

**95 GHZ SILICON GERMANIUM LOW NOISE AMPLIFIER AS FRONT-END  
RECEIVER FOR SPARSE APERTURE MILLIMETER WAVE IMAGING**

by

Andrew Alexander Wright

A thesis submitted to the Faculty of the University of Delaware in partial fulfillment of the requirements for the degree of Master of Science in Electrical and Computer Engineering

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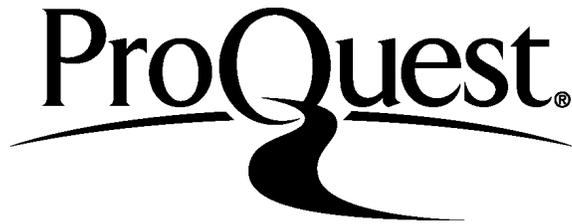
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## ABSTRACT

Demand for the ability to navigate in degraded visual environments (DVE) such as dust, smoke, and fog, has led to the development of millimeter wave (mm-wave) real-time imaging systems. Millimeter wavelength radiation has shown that the wavelengths are long enough to penetrate the obscuring agents while also allowing sufficient resolution. A low attenuation atmospheric window in the 95 GHz region has pushed for these systems to operate at these millimeter wavelength frequencies. Due to low signal levels at these frequencies, the system requires high gain in the front-end to boost the signals of mm-wave frequencies. This involves collecting the electromagnetic waves with a horn antenna and then amplifying the signal with a low noise amplifier (LNA) to maximize the signal to noise ratio (SNR). In photonics-based imaging systems, the mm-wave signal is then up-converted to optical domain, where it then propagates through optical fibers to an infrared camera for further processing. The horn, LNA and up-converter comprise a single module. A large distributed array of modules, around 200, are required for a real-time mm-wave imaging system capable of peering through DVE. As a result, pushing this technology to higher frequencies can be very costly, due to the high prices of individual high frequency components. Therefore, an alternative technology is required to keep the costs to a minimum.

One approach to controlling costs of components operating at higher frequencies is to adopt an alternative amplifier technology. Conventionally, commercially available GaAs and InP LNAs are used to obtain high gain at the high frequencies, but at 95 GHz, each amplifier used to be thousands of dollars. Since then, costs for each amplifier decreased to \$100. With each module requiring three or more amplifiers, costs become prohibitively high for many applications. Therefore, this thesis focuses on the

development of a 95 GHz amplifier using silicon germanium (SiGe) technology to obtain the required high gain while maintaining low costs. To date, extensive efforts have been made in the development of SiGe amplifier technology and high gain was demonstrated at the W-band. However, existing amplifier technology does not meet the requirements of the mm-wave imager. In particular, major limitation is the 3-dB bandwidth of the gain curve. A distributed aperture system with a wide field of view and broadband response will experience a phenomenon known as fringe-washing if an off-axis signal arrives with significant delay between the receivers on the opposite ends of the longest baseline. Severe fringe-washing occurs when this delay of the projected baseline is comparable to the correlation time of the signal, i.e. the inverse bandwidth of the system. To mitigate fringe-washing, each module must limit the bandwidth of operation, which can be accomplished either with a filter or an amplifier. Since filters can be lossy, ideally a narrow-band amplifier is preferred.

In this thesis, using the basic principle of amplifier design, an LNA is developed based on advanced SiGe-foundry processes to operate in the 95 GHz regime. The advantage of a custom SiGe amplifier is the ability to design it to meet the imager's specific demands, including gain, noise figure, bandwidth, and power consumption in a single low cost device. This thesis details such design, and includes the discussion of tradeoffs and limitations imposed by the commercial SiGe-foundry processes employed.

## Chapter 1

### INTRODUCTION TO MILLIMETER WAVE TECHNOLOGY

Amplifiers have been in development since the first amplifying device in 1907 by Lee De Forest with his triode vacuum tubes, which he called the “Audion”. Since then tubes have been replaced by solid-state semiconductor transistors, such as metal oxide semiconductor field effect transistors (MOSFETs) and bipolar junction transistors (BJTs). As semiconductor processes are enhanced, operating frequencies of transistors have been increased to the millimeter-wave (mm-wave) region, i.e., 30 to 300 GHz and beyond. With this development of transistor technology, mm-wave amplifiers are also being developed and are a critical device for many applications such as automotive radars, communication systems, and RF imaging systems.

#### 1.1 Atmospheric Attenuation and Millimeter Wave Imaging System

One major characteristic of electromagnetic waves, specifically in the mm-wave spectrum, is the atmospheric attenuation as a function of frequency. Figure 1.1 shows a plot of the atmospheric attenuation for different levels of humidity and fog. [1] As seen from Figure 1.1, electromagnetic waves can transmit within several frequency regions with low attenuation. These frequency regions are known as atmospheric transmission windows, which allow for maximum penetration of fog, dust, smoke, as well as other obscurants. It is evident that W-band (75-110 GHz) frequencies will have the capabilities of maximum penetration in degraded visual environments (DVE). The military is interested in fielding high resolution millimeter wave imaging systems capable of providing covert, stand-off screening at checkpoints and as navigational aids in DVE. One particular area of interest is in achieving a real-time imaging system that

allows helicopters to navigate in DVE, specifically, “brown-out” conditions which occur when landing rotary craft in unimproved, dusty landing zones.

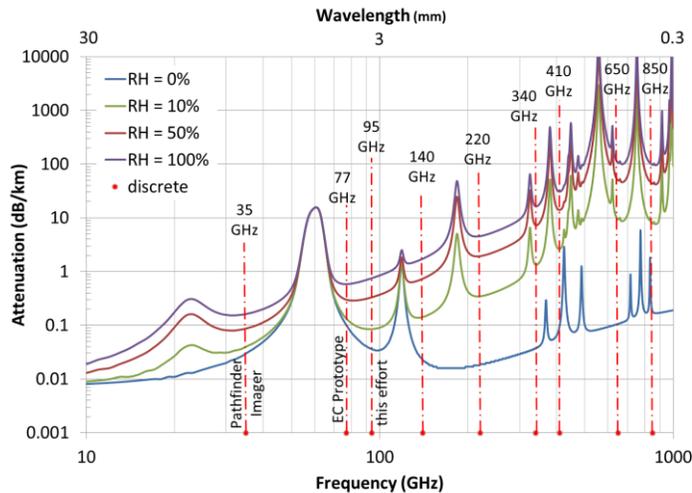


Figure 1.1: Plot of the atmospheric attenuation [1] in dB/km for moist air and fog using codes developed by mmW Concepts LLC. The surface air temperature is 15 °C and the atmospheric pressure is 1013 mbar.

The government requires the ability to see through DVE due to major threats to rotary wing aircrafts operating in areas of brownout. According to the *Aviation Safety Technologies Report*:

“Degraded Visual Environments (DVEs) caused by brownout and whiteout account for almost half of the Air Force rotorcraft airframe losses, and are the leading cause of airframe losses for the Army. In addition to the safety impact, DVEs create impediments to operations where these conditions occur.” [2]

To counter the DVE threat to today's pilots, the US armed forces and Defense Advanced Research Projects Agency (DARPA) are all working on brownout and

whiteout solutions. One of the solutions is to exploit mm-wave radiation to achieve real-time environment imaging at video rates with high resolution.

## **1.2 Millimeter Wave Front-End Module and Imaging System Description**

For the past several years, the University of Delaware (UD) and Phase Sensitive Innovations (PSI) Inc. have been working together on the development of a real-time mm-wave imaging system. UD and PSI Inc. has developed a photonics based front-end receiver module that was specifically designed to collect electromagnetics signal at 77 GHz. The module consists a horn that collects the electromagnetic waves where the RF signal is then amplified with three or more low noise amplifiers (LNA) to maximize the signal to noise ratio (SNR). This being a photonics-based module, the mm-wave signal is up-converted to the optical domain using an optical phase modulator. Typically with W-band frequencies, the signal would be down converted to a lower frequency with a downconverting mixer instead of being optically up-converted. There are several benefits to working in the optical domain, such benefits include the routing of signals with low loss and light weight fiber optic cables instead of bulky and lossy RF cables, removal of complex correlation circuitry, simplified optical filtering, and etc. With the use of a photonics-based front-end receiver module and the benefits it holds, a W-band single pixel radiometer was constructed, also known as the W-band scanning cart. Two sets of images captured by this single pixel radiometer are as shown in Figures 1.2 and 1.3. Figure 1.2 consists of a visible light image of a building near a body of water. The following images show the same building on a foggy day and the corresponding mm-wave image. In visible light, the building is no longer perceived, but through mm-waves, the building is visually imaged. Similarly, Figure 1.3 compares the image of a motorcycle with and without a cover to equivalent mm-wave image with the cover on.

The cover is relatively transparent at millimeter wave frequencies, making it possible to see the motorcycle.



Figure 1.2: Visible image of a building on a clear day (top) and the same building on a foggy day (middle) and a millimeter wave image of the building in the same fog (bottom).



Figure 1.3: Imager of (left) a motorcycle in the visible light spectrum and (middle) a motorcycle with a cover in the visible light spectrum and (right) a millimeter wave image of motorcycle with a cover.

With the two examples taken with the W-band scanning cart, it is feasible to create a photonics-based imaging system capable of operating in the mm-wave spectrum and that enables the ability to peer through DVE. Using this same optical upconversion concept in a distributed aperture imager, a real-time imaging system is then comprised of an array of the front-end receiver module technology. As the name suggests, mm-wave images can now be taken instantaneously and video rates (~30 fps), unlike the scanning cart that requires several minutes to capture a single image. UD and PSI have also created and proven a 77 GHz, 220 channel distributed aperture imaging system capable of taking real-time video.

With the completion of the real-time imaging system, the next goal of this project is to improve the resolution of the captured image. To improve resolution, the imaging system will be required to operate at a higher frequency. Next higher frequency with a low atmospheric attenuation is 95 GHz as shown in Figure 1.1. Issue that comes along with moving from 77 GHz to 95 GHz is the size, weight, power, and cost (SWaP-C). Not only is it desired to improve the imager's resolution, it is also important to keep SWaP-C to a minimum. Considering a real-time imaging system requires a large number of front-end modules and each module requires at least three LNAs, each commercial LNA at 95 GHz is not cost effective. This leads to the next section discussing the research and commercially available LNA technology that is capable of operating at 95 GHz.

### **1.3 Existing Millimeter Wave Amplifier Technology**

There are several existing LNAs that can operate at 95 GHz, as shown in Table 1.1. Mostly developed as research efforts, these amplifiers are not commercially available and those that are available, cost as much as \$90 each. The LNA needs to be

both inexpensive and meet specific requirement, which are defined in Chapter 2. These reasons lead to the research described in this thesis, i.e., development of a 95 GHz LNA using SiGe BiCMOS technology. The SiGe platform is chosen for its cost-effectiveness in addition to the capability of operating at 95 GHz. Likewise, as shown in references [11-17], it is possible of achieving the range of gain for this objective with SiGe technology at 95 GHz.

Table 1.1: Existing high frequency amplifiers

Ref.	Frequency [Peak] (GHz)	Gain (dB)	Noise figure (dB)	Fabrication process	OP1dB (dBm)	Power dissipation (mW)	Chip size (mm <sup>2</sup> )
[3]	80-100 [94]	13	2.3	0.07 um InAlAs/In GaAs	-	-	1.00
[4]	[95]	20	2.5	InP	-	-	-
[5]	85-110 [94]	16	3.2	InP	-	30.8	3.00
[6]	75-101 [94]	11.5	3.3	InGaAs/In AlAs InP	-	-	2.55
[7]	67-102 [94]	19.4	2.5	0.1 um InGaAs InAlAs/InP	-	18	-
[8]	75-120 [110]	25	7	65 nm CMOS	-3	48	0.25
[9]	89-107 [95]	10.7	6	45 nm SOI CMOS	5.2	52	0.32
[10]	100-120 [110]	20	4	0.13 um SiGe	-5	17	0.41
[11]	110-130 [121]	25	7	0.13 um SiGe	5 *	54	0.33
[12]	82-100 [95]	27	8 *	0.12 um SiGe	-	27.6	0.20
[13]	110-135 [130]	17.5	7.7	0.13 um SiGe	-	31.5	0.36

[14]	83-91 [90]	22	7	0.13um SiGe	-	56	-
[15]	77-101 [92]	45	7	0.13um SiGe	0.2 *	19.2	0.77

\*Simulated

#### 1.4 Outline of this Work

Introduced above is the purpose towards the development of a SiGe LNA that operates at 95 GHz. The remainder of this document details the primary requirements, designs, and performance characterization of the fabricated 95 GHz LNA. Chapter 2 discusses with further details of the imager and the requirements defined for the LNA in order to be used for the front-end receiver module. Available SiGe foundries and processes are also discussed and analyzed as to which is best to develop the LNA technology. Chapter 3 covers gain, noise figure, bandwidth, interstage matching, and output power and the necessary ways to obtain these figure of merits. Chapter 4 details the characterization of a fabricated passive device that is compared with HFSS™ simulations as well the modeling of the passive components used in the LNA design, which includes coplanar waveguide, microstrips, capacitors, RF probes and wire bonds. Chapter 5 presents the fabricated LNA designs along with the measured results. The general design of each amplifier and significance of the fabricated device is explained, alongside the challenges concerning each of those designs. The designs reviewed include those of a single stage, a four stage, and a six stage LNA. Chapter 6 entails the measurement setups e.g., vector network analyzer to measure the s-parameters, noise figure setup using the Y-factor technique, and 1-dB compression point measurement set. Finally, Chapter 7 summarizes this thesis and provide insight into future research.

## Chapter 2

### REQUIREMENTS FOR 95 GHZ AMPLIFIER

Millimeter wave imaging has many variables that define the overall quality and resolution of the captured image. The amplifier must meet certain requirements to have it satisfy the variables for the imager. Figures of merit for the SiGe amplifier design are gain, noise figure, power dissipation, output power, and 3-dB bandwidth. In this chapter, in-depth analyses of the goals for a successful RF front-end 95 GHz SiGe low noise amplifier are detailed.

#### 2.1 Amplifier Bandwidth Considerations for an Up-Conversion Receiver Module

The radiometric power received at each front-end receiver module of the imager is given by the well-known formula

$$P = k_B T B$$

$$P_{dB} = 10 \log(k_B T B) \quad (2.1)$$

where  $k_B$  is Boltzmann's constant ( $1.3806505 \times 10^{-23}$  J/K),  $T$  is the object temperature in Kelvin, and  $B$  is the system bandwidth in Hz. Received power is independent of the operating frequency, antenna gain and source distance, but simply proportional to the device's black body temperature and system bandwidth. Terrestrial emissive objects (300 K) yield a received power of around 4 pW per GHz of bandwidth. The power at the antenna in dBm for a terrestrial source, yield greater received power levels for larger bandwidths. This system bandwidth can be set by the cutoff frequencies of the antennas, waveguides, filters within the system or by the amplifiers that are used to amplify the signal.

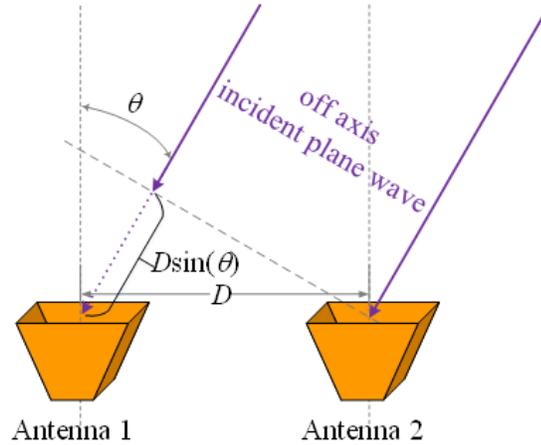


Figure 2.1: Diagram showing the geometric time delay induced by an off axis signal to two antennas separated by baseline distance  $D$  in a distributed aperture system.

The distributed aperture configuration, however, places further bandwidth limitations to the system. A distributed aperture system with a wide field of view will experience a phenomenon known as fringe-washing. This occurs when an off-axis signal arrives at receivers on opposite ends of the longest baseline with a significant delay between them. As shown in Figure 2.1, a geometrical time delay,  $\tau = D\sin(\theta)/c$ , is created when an off axis signal arrives at two different antennas separated by a distance  $D$ . Fringe washing can occur when this delay of the projected baseline is comparable to the correlation time of the signal and hence the inverse bandwidth of the system. To circumvent this effect we require that

$$\frac{D\sin(\theta)}{c} < \frac{1}{B},$$

or equivalently

$$B < \frac{c}{D\sin(\theta)} [\text{Hz}], \quad (2.2)$$

where  $D$  is the longest baseline (i.e. width/height of the imaging aperture),  $\theta$  is the maximum incident angle (i.e. one-half the instantaneous field of view of the imager),  $c$  is the speed of light, and  $B$  is the system bandwidth in cycles/sec (Hz). It should be noted that the maximum baseline, and hence the imager overall aperture size also determine the angular resolution of the system as given by

$$\Delta\theta \approx 1.22 \frac{\lambda}{D} = 1.22 \frac{c}{\nu D}, \quad (2.3)$$

where  $\lambda$  is the free-space wavelength of the signal, and  $\nu$  is the frequency of the signal. Reasonable resolution can be achieved at around a 95 GHz operating frequency with aperture sizes ( $D$ ) on the order of one-half ( $\Delta\theta \approx 0.44^\circ$ ) to 1 meter ( $\Delta\theta \approx 0.22^\circ$ ) in size. Systems with smaller aperture sizes suffer lower angular resolution while larger systems are difficult to deploy due to SWaP limitations.

The optical upconversion module's function is to linearly convert the incident millimeter wave radiation into optical sidebands on a telecom wavelength laser carrier while preserving the relative phase information. More energy in the sideband results in more infrared optical power incident on the SWIR camera to reconstruct the millimeter wave scene. This power can be increased by 1) increasing the bandwidth of the captured millimeter wave energy spectrum or 2) by increasing the level (i.e. power) of the signal with more gain and a higher output power.

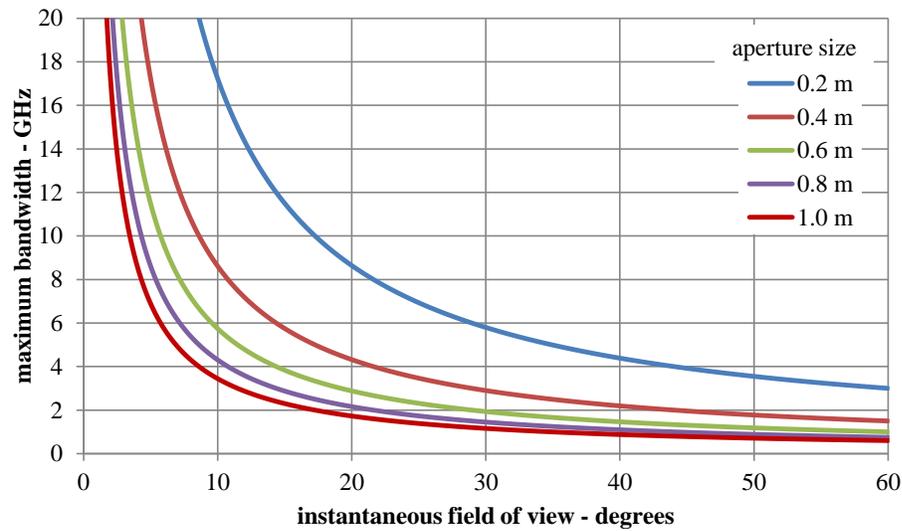


Figure 2.2: Bandwidth limitations due to fringe washing in a distributed aperture imaging system with aperture sizes of 200 mm to 1 meter as a function of the instantaneous field of view of the imager.

Figure 2.2 shows the bandwidth limitations inherent in a distributed aperture system due to fringe washing as a function of the imager's instantaneous field of view for imagers with aperture sizes of 200 mm to 1 m. It is evident that a larger field of views for a given aperture size places a more stringent restriction on the bandwidth of the imaging system. While reducing the system bandwidth will allow for greater field of views, it has the effect of reducing the incident power. The current 220 channel imaging system has an aperture size of close to 600 mm and an instantaneous field of view of  $\pm 10^\circ$ , which stipulates a maximum operating bandwidth of 2.9 GHz. The second way to increase the level of the up-converted millimeter wave signal in the optical sidebands is to increase the absolute power level of the mm-wave signal coupled into the lithium niobate electro-optical modulator within a given bandwidth. The power delivered to the modulator is limited by the gain of the amplifier chain as well as

saturated output power of the overall amplifier chain. This is ideally set by the last stage and is often characterized by a parameter known as P1dB that specifies the input referred power that results in a 1 dB gain compression at the output. An additional factor is the coupling efficiency from the last amplifier to the modulator within the package. It should be noted that most off the shelf amplifiers have a wide bandwidth, but those that have a narrow bandwidth have power requirements on the order of 1 watt, which is undesirable for a multi-channel imager.

## 2.2 Amplifier Requirements

The focus of this work was designing an amplifier with a bandwidth less than 5 GHz. This would allow for a 30° instantaneous field of view from a 0.4 m (~ 16”) aperture imager. The amplifier stage not only must have a narrow bandwidth, but it must couple well with the 50 Ω lithium niobate modulator load. The power delivered to a load is given as the rms voltage squared over the impedance of the load:

$$P_{load} = \frac{v_{rms}^2}{Z_{load}} = \frac{(\hat{V}/\sqrt{2})^2}{Z_{load}} = \frac{\hat{V}^2}{2Z_{load}}, \quad (2.4)$$

The peak to peak signal voltage,  $V_{pp}$ , is then simply twice the peak voltage amplitude,  $\hat{V}$ . The peak-to-peak signal voltage as a function of power level in dBm is plotted in Figure 2.3 for load impedances of 25, 50, and 100 Ω. Obviously, higher output powers and higher load impedances require larger voltage swings. Typical supply voltages are on the order of 1.6 to 2.5 volts for this SiGe process which makes achieving the larger peak to peak voltages a challenge. The optical up-conversion module requires an input power of +3 to +6 dBm (2 to 4 mW), so it is evident from Figure 2.3, for a 50 Ω load a voltage swings of 900 mV to 1.25 V peak to peak is required.

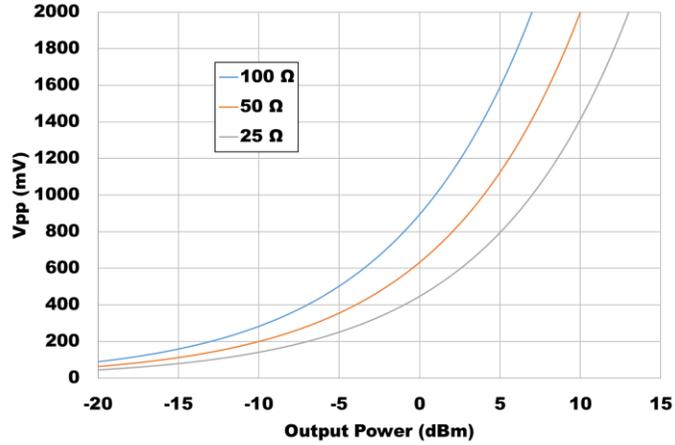


Figure 2.3: Peak to peak voltage swing,  $V_{pp}$ , in millivolts versus output power in dBm for loads with impedances of 25, 50, and 100  $\Omega$ .

The incident radiometric power ( $k_B T B$ ) of a terrestrial emitter within a 2 GHz bandwidth is -80.818 dBm, so the overall gain of the module will need to be roughly 87 dB to achieve these output power levels. If we assume 10 dB of internal packaging and transmission line losses, the total gain from the three or more amplifiers will need to supply close to 100 dB. First stage to increase the mm-wave signal will be an InP LNA [16] that provides 30 dB of gain and a noise figure equal to 3 dB, so with two cascaded SiGe amplifiers will be designed to have a readily tunable gain of 35 dB. Demonstrated work of an amplifier with over 40 dB of gain has been displayed in a single IC at these high frequencies, showing it is possible to obtain high gain from a single IC and remain stable [15].

Final consideration is the noise introduced by the amplifier. Overall noise factor of an  $n$  stage amplifier chain is given by the Friis formula for noise factor

$$F = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \frac{F_4 - 1}{G_1 G_2 G_3} + \dots + \frac{F_n - 1}{G_1 G_2 G_3 \dots G_{n-1}} \quad (2.5)$$

where  $F_n$  is the noise factor and  $G_n$  is the power gain of the  $n^{\text{th}}$  stage. The noise of the first stage,  $F_1$ , is the dominant factor in the overall noise figure ( $NF = 10\log(F)$ ) of the amplifier chain. The noise of subsequent amplifiers is reduced by the gain of previous stages. The best W-band noise figures in SiGe measured directly at the die level on research and development devices are around 4 dB [11], but the SiGe foundry process decided to fabricate the amplifiers, commonly have a noise figure of 7-8 dB at 95 GHz, hence the utilization of commercially available InP low noise amplifier (LNA) [16], with about 3 dB NF, for the first stage.

### 2.3 Foundry Decision

Recent advances in SiGe:BiCMOS foundry technology has enabled low cost, high volume production of hetero-junction bipolar transistors (HBTs) with transition frequencies,  $f_T$ , of well over 200 GHz. Foundry decision was focused on state-of-the-art in silicon processes available in the United States. TowerJazz at the time released the SBC18H3 process with a 240/270 GHz  $f_T / f_{MAX}$  and their roadmap has plans for higher performance 180 nm designs as well as 130 nm designs. The new and future design technologies provide lower power consumption and lower noise as well as higher operating frequencies. IBM 8HP SiGe:BiCMOS process using 130 nm technology achieves a 200/265 GHz  $f_T / f_{MAX}$  and also has the capability of adding bumps for flip-chip packaging. Both TowerJazz and IBM (through MOSIS) offer multi-project wafer shuttle runs for the fabrication of test die.

TowerJazz has created accurate models and design kits for each technology for use in the Cadence® Design Tools that enable the extraction of parasitic elements from the circuit layout, which allows for accurate modeling of the physical die's performance. SBC18H3 processes is similar in architecture to previous generations of SBC18

processes, but has been scaled modestly in the lateral dimensions in order to reduce parasitic capacitances and resistances and thus improve  $F_{MAX}$  and  $NF_{MIN}$ . Furthermore, the noise and power consumption of circuitry is greatly reduced in the SBC18H3 technology. TowerJazz specifies a minimum noise figure of less than 1 dB at 20 GHz and 2 dB at 40 GHz. Proprietary documentation suggests that the minimum noise figure at 100 GHz is around 7 dB which rival that of much more expensive III-V technologies. TowerJazz also offers SBC18H3 technology design submission at a monthly basic, with a three month lead time. With a high  $f_T$ , decent noise figure at 95 GHz, and quick lead times, TowerJazz technology was the choice for fabricating the low noise amplifier.

#### **2.4 Summary**

In summary, the amplifier needs to meet the following goals  $\geq 35$  dB of gain at 95 GHz,  $\leq 5$  GHz; 3 – 6 dBm of output power to a 50  $\Omega$  load, and power dissipation less than 100 mW; and a small packaged footprint of 1mm x 0.5mm. Currently there are no commercially available amplifiers that meets these requirements. It was decided to use TowerJazz's SBC18H3 SiGe:BiCMOS process to obtain the goals defined based on their monthly tape outs, fast lead times, decent noise figure, and low power consumptions.

## Chapter 3

### TECHNOLOGY CHALLENGES AND SOLUTIONS

As described in the previous chapter, amplifier design introduces a lot of technology challenges that are difficult to overcome in order to achieve high gain, low noise, narrow bandwidth, low power dissipation, and medium output power. This chapter will discuss the design challenges and technology considerations made to achieve a 95 GHz low noise amplifier design capable of acting as a front-end module for a passive mm-wave imaging system.

#### 3.1 Available Gain

Achieving high gain within the frequency range of 75-110 GHz, W-band range, will be the first step to developing the low noise amplifier. Two amplifier topologies were studied to achieve the gain bandwidth (GBW) needed from the NPN transistors in the TowerJazz SiGe technology. The high frequency model of the NPN transistor are shown in Figure 3.1 [17]. The common emitter amplifier suffers from the Miller Effect where the  $C_{\mu}$  (collector-base junction capacitance) of the device is effectively multiplied by the gain of the transistor. This significantly lowers the frequency of the pole that determines the high frequency cut-off of the amplifier. It is possible to eliminate the Miller Effect by using a common emitter amplifier in conjunction with a common base amplifier in what is known as a “cascode” configuration. Cascode was chosen as the amplifying stages in the design since it does not suffer from the Miller effect, which reduces the operating bandwidth of the circuit. The cascode design uses the common base configuration to serve as a current buffer and thereby eliminates the effect of the base to collector capacitance of the common emitter transistor. This also results in higher isolation from the output to the input, which is important in high gain designs.

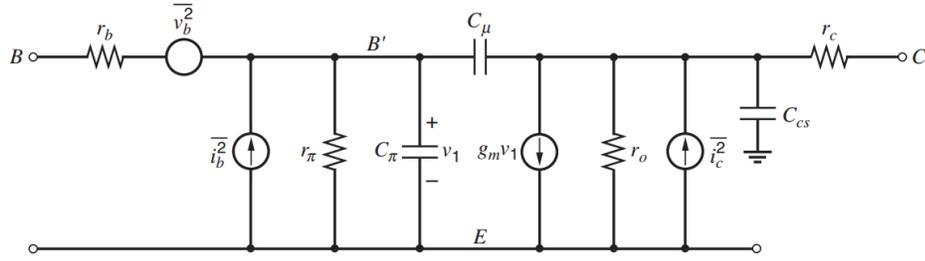


Figure 3.1: Diagram of a capacitively coupled common emitter amplifier (top) and the high frequency model of the BJT (bottom). [17]

To ensure stable operation, the isolation of the circuit must be significantly lower than the gain of the circuit. The feedback can occur through the circuit, the substrate, power and control lines, and free space. One of the advantages of the cascode design is that the common base transistor used in the cascode makes the amplifier unilateral in performance by isolating the output from the input. This enables much higher gains to be realized in a cascode amplifier over that of the more ubiquitous common emitter designs. This circuit design has additional features that are designed to increase isolation and allow for more gain in a single integrated circuit.

When using a cascode typology, the transition frequency has an impact and must be considered for several aspects that include gain and noise figure. The collector-base junction capacitance  $C_\mu$  is given by

$$C_\mu = \frac{C_{\mu 0}}{\left(1 + \frac{V_{CB}}{V_{0c}}\right)^m}, \quad (3.1)$$

where  $C_{\mu 0}$  is the value of  $C_\mu$  at zero voltage;  $V_{CB}$  is the magnitude of the collector-base junction reverse-bias voltage,  $V_{0c}$  is the collector-base junction built-in voltage (typically, 0.75 V), and  $m$  is its grading coefficient (typically, 0.2–0.5). The emitter-

base capacitance,  $C_\pi$ , is comprised of the small-signal diffusion capacitance  $C_{de}$  and the base–emitter junction capacitance  $C_{je}$

$$C_\pi = C_{de} + C_{je}, \quad (3.2)$$

where diffusion and junction capacitance are given by

$$C_{de} = \tau_F g_m = \tau_F \frac{I_C}{dV_{BE}} \quad (3.3)$$

$$C_{je} = 2C_{je0}. \quad (3.4)$$

The factor  $\tau_F$  is a device constant with the dimension of time known as the forward base-transit time. Typically, the emitter-base capacitance is on the order of a few pF to tens of pF while the collector-base capacitance is a fraction of a pF to a few fF, so it can be considered as negligible. It can be shown that the transition frequency,  $f_T$ , of the transistor is related to the device capacitance by the following relationship:

$$f_T = \frac{g_m}{2\pi(C_\pi + C_\mu)} \cong \frac{g_m}{2\pi C_\pi}. \quad (3.5)$$

TowerJazz offers three different high speed NPN transistor designs:

1. 121 – one emitter, two bases, and one collector,
2. 122 – one emitter, two bases, and two collectors,
3. 232 – two emitters, three bases, and two collectors.

The transistor used to do the simulation is a 122, with an emitter length of 3  $\mu\text{m}$ . With this and the simulation from the Cadence®, the common emitter transition frequency is shown in Figure 3.2a. As described by TowerJazz, the peak  $f_T$  is around 250 GHz, this simulation is ideal, so parasitics are not being considered. Now considering equation 3.6,  $C_\pi$  is doubled in a cascode typology with the same transistor, making,

$$f_T \cong \frac{g_m}{4\pi C_\pi}. \quad (3.6)$$

The simulation transition frequency ( $f_T$ ) of the cascode is as shown in Figure 3.4b. It can be seen that  $f_T$  drops more than 100 GHz, but it is still within reason to obtain decent gain at 95 GHz.

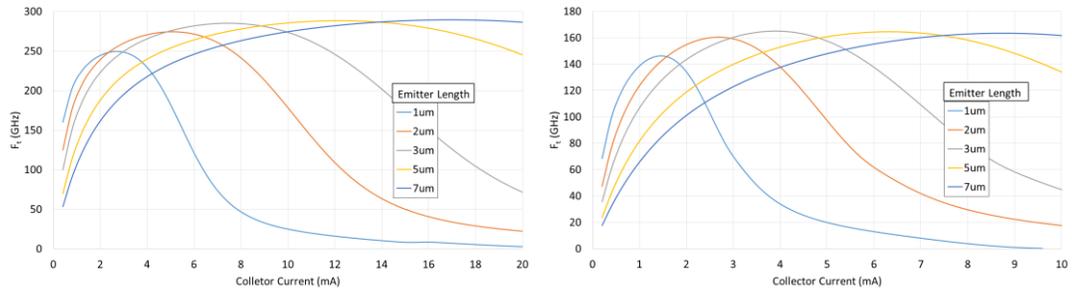


Figure 3.2: a) Simulated transition frequency of a common emitter typology with various emitter lengths, b) Simulated transition frequency of a cascode typology with various emitter lengths.

There are three solutions to improving the gain of an amplifier. First, a well-known technique is used that can compensate for the cut-off frequency by “peaking” the gain. This is accomplished by adding an inductive load, which is known as inductive peaking. The inductive element is in-parallel with the internal capacitance of the transistor or a capacitor. An LC circuit is created, with the proper parameters will cause a resonance at a specific frequency, known as a single tuned amplifier. [18] The quality factor,  $Q$  of the circuit can be calculated with Equation 3.7.

$$Q = R\sqrt{C/L}. \quad (3.7)$$

The resonance alters the frequency response of circuit as shown in Figure 3.3a. Gain increase as a function of  $Q$ . With increasing  $Q$ , increases the magnitude as seen in Figure 3.3b. [19]

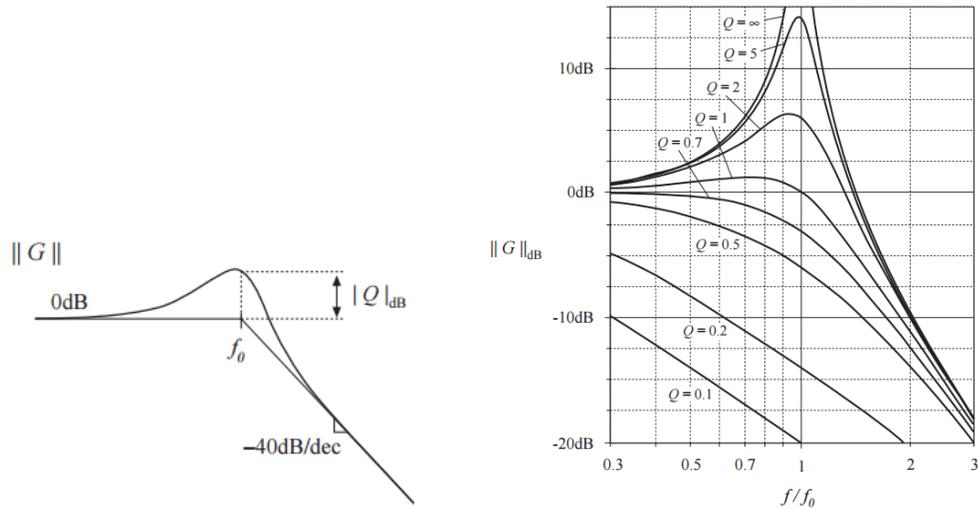


Figure 3.3: a) Bode plot of the magnitude asymptotes for the two-pole transfer function with and without the resonant circuit, b) Two-pole response for several values of  $Q$ . [19]

The second technique considered to increase the gain of a single stage cascode is inductive boosting. Inductance is added between the base of the common base and the positive supply rail. As stated in [20], "The real part of the look-in impedance in the common base transistor decrease with the increasing inductance. This impedance acts as the load impedance of the common emitter stage. Hence the voltage gain of the common emitter stage increases and simultaneously gain is also increased." As the inductance increases there is a specific point where the gain decreases due to the reduction in gain of the common base stage. The trade off to this technique, is the reduction in the overall stability factor. There is a reduction in stability because of the reduced load resistance of the common emitter stage. If done correctly, there is an obtainable point where maximum gain is achieved and also remain unconditionally stable. Inductive boosting also increases the noise figure of the stage because of the

alteration in impedance. This technique has been used by a group [15] that designed a low power, high gain amplifier at 95 GHz, by adding inductive boosting to each of the four stages in the amplifier. They measured and proved that it is possible to obtain a gain of 45 dB in a single integrated circuit. Considering we will be designing an amplifier with high gain and a low noise figure, inductive boosting should not be used at the first stage.

Third and final technique and the most simple, is a multistage design. Total gain is summed by the gain of each individual stage as describe in the following equation, with  $G_n$  representing the gain of the  $n^{\text{th}}$  stage,

$$G_T = G_1 + G_2 + \dots + G_n. \quad (3.8)$$

Issue with multiple stages, increases the amount of power consumption by a single IC. As mention before, we want to achieve high gain, but with a power consumption of 100 mW. The tradeoff for higher gain by increasing number stages to power dissipation needs to be determined for the amplifier design. Increase in gain is achieved by inductive peaking, inductive boosting, and multiple amplifier stages.

### 3.2 Noise

In the world of electronics, one difficulty in developing a front-end amplifier is noise. Noise is a random fluctuation of an electrical signal that exists in all conductors. “Statistical fluctuation of electric charge exists in all conductors, producing random variation of potential between the ends of the conductor. The electric charges in a conductor are found to be in a state of thermal agitation, in thermodynamic equilibrium with the heat motion of the atoms of the conductor. The manifestation of the phenomenon is a fluctuation of potential difference between the terminals of the conductor” [21], as quoted by J.B. Johnson. In this section, a discussion of noise and

noise figure of a low noise amplifier and the techniques used to keep the noise figure at a minimum are detailed. The noise factor,  $F$ , is the difference between the noise output of the actual receiver to the noise output of an “ideal” receiver with the same overall gain and bandwidth when the receivers are connected to a matched source. The noise figure, in dB, is then  $10 \log (F)$ .

### 3.2.1 Types of Noise

There are four types of noise sources that must be considered during amplifier design: thermal noise (Johnson-Nyquist noise), shot noise, flicker noise, and burst noise. First, thermal noise results from the random (Brownian) motion of transporting electrons, which causes random current flow even if there is no external bias of electric field. Thermal noise is directly seen with the base resistance of the heterojunction transistor (HBT). Random current flow leads to random voltage fluctuation across the base resistance. Noise increases with increasing temperature, due to higher fluctuation of transporting electrons. The basic equation for thermal noise is given as,

$$v_n = \sqrt{4k_B TRB}, \quad (3.9)$$

where  $k_B$  is Boltzmann’s constant,  $T$  is the resistor’s temperature,  $R$  is the resistance, and  $B$  is the bandwidth.

Next, shot noise (Poisson noise), which refers to the fluctuations associated with DC current flow across a potential barrier. Specifically for a transistor, shot noise is the thermal fluctuation of minority carriers in the p-n junction. Disturbance of the minority carriers, causes the current to fluctuate randomly, so for the HBT, this occurs from the base and collector current. Basic equation for shot noise is given as,

$$i_n = \sqrt{2IqB}, \quad (3.10)$$

where  $I$  is the DC current,  $q$  is the elementary charge, and  $B$  is the bandwidth.

Third, flicker noise (pink noise) is caused by resistance in the path of the current, which causes a fluctuation of number of carriers. Flicker noise is simply seen as generation-recombination noise and  $1/f$  noise,  $f$  representing the frequency. At high frequency, it can be seen as almost negligible.

Finally, burst noise (RTS noise) is caused by random trapping and release of charge carriers to the Fermi level. Source of the noise can occur from imperfection of the crystal lattice structure of the transistor. “Kleinpenning [22] showed that RTS noise exists with devices with small number of carriers, where a single electron can be captured by a single trapping center.” [23] As shown in Figure 3.4 is a complete small-signal equivalent schematic of a bipolar transistor with noise sources taken from the Meyer and Gray [17], Analysis and Design of Analog Integrated Circuits book.

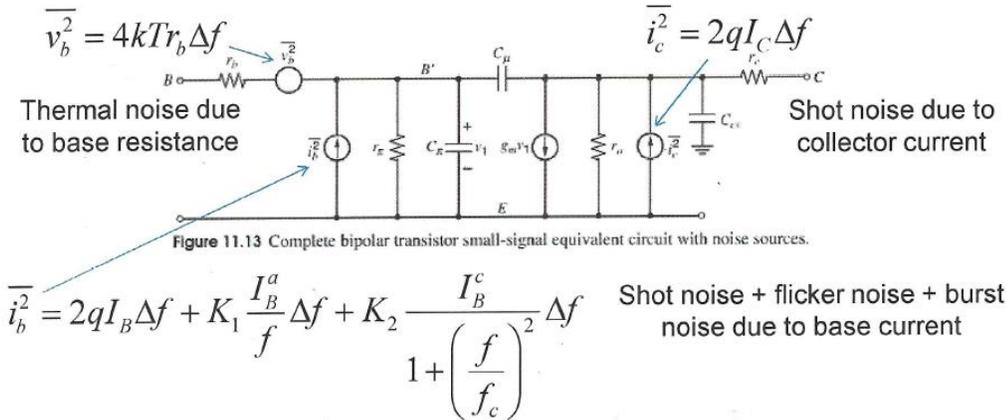


Figure 3.4: Complete bipolar transistor small-signal equivalent circuit with noise sources. [17]

### 3.2.2 Impact of Parasitics to Noise Figure

Layout parasitics will also have a large contribution to noise figure (NF) of the amplifier. Major source of parasitics form by substrate coupling, ESD protection, input RF signal pad, and wire bonds. First off, substrate coupling is as it sounds, it is the RF signal coupling with the silicon substrate. Coupling with the semiconductor causes loss and noise, which is not caused by the capacitor itself, but by the thermodynamic equilibrium of the amount of charge on the capacitor. Once the capacitor is disconnected from a conducting circuit, the thermodynamic fluctuation is frozen at a random value with standard deviation as given above. Transmission of a signal over a balanced line reduces the influence of noise or interference due to external stray electric fields. Any external signal sources tend to induce only a common mode signal on the line and the balanced impedances to ground minimizes differential pickup due to stray electric fields.

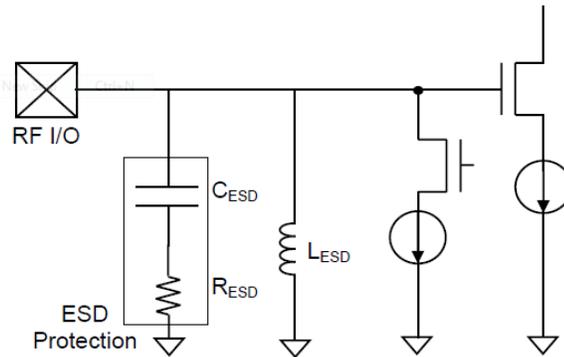


Figure 3.5: Schematic of the ESD diode between RF input and the gate of a MOSFET.

Second source of noise is the ESD protection diodes, TowerJazz fabrication process requires a reverse bias diode shunted with the RF signal path for ESD protection. The diode has a small impact to the noise as depicted in Figure 3.5 and Equation 3.11,

$$NF = 1 + \omega^2 C_{ESD}^2 R_S R_{ESD}. \quad (3.11)$$

Third source of parasitic noise is the RF signal pad. In order to propagate a signal to the amplifying circuit, a ground signal ground (GSG) port is required. It is essential there is plenty of pad space for the RF probe and wire bonds. Similar to the ESD protection diode, the signal pad is acting as shunt capacitor with the signal path. Capacitance of the pad can be calculated with Equation 3.12,

$$C_{pad} = \frac{\epsilon_{SiO_2} A_{pad}}{h}. \quad (3.12)$$

With  $\epsilon_{SiO_2}$  representing the permittivity of the dielectric, in our case silicon dioxide,  $A_{pad}$  representing the pad area, and  $h$  representing the height from the return path. It is preferable to keep the size of the pad as small as possible, but large enough to do wire bonding when packaging the device, which lead to the final source of noise, wire bonds. The wire bond acts as a series inductor with the signal path. A precise inductance can be derived from

$$L_{wb} = 5.08 \times 10^{-3} l \left( \ln \left( \frac{4l}{d} \right) - 1 \right) [nH], \quad (3.13)$$

where  $l$  is the length of the wire bond and  $d$  is the diameter, both given in mils (thousands of an inch). A plot of inductance and reactance versus wire bond length is shown in Figure 3.6 for a standard 1 mil diameter wire. From this graph a more accurate inductance for a 1 mm long wire bond is 0.81 nH for a reactance of 485  $\Omega$ . Series inductance will cause a severe impedance mismatch causing loss to the signal, degrading the NF.

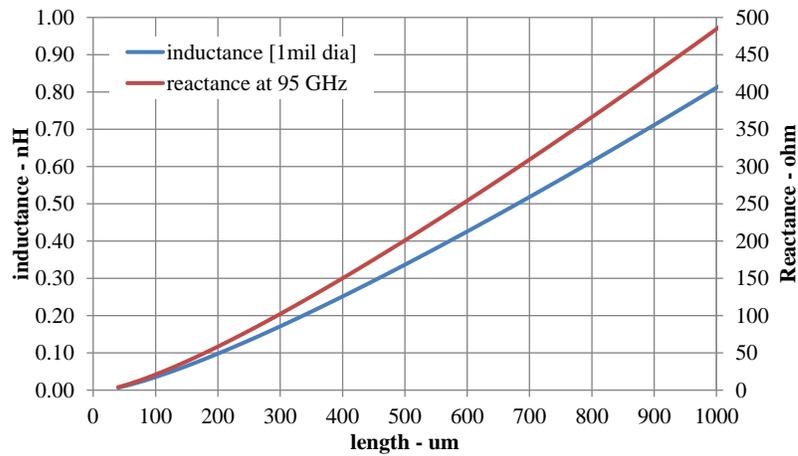


Figure 3.6: Plot of the inductance in nanohenries and reactance on ohms at 95 GHz of a 1 mil diameter wire bond as a function of the length of the wire bond.

To mitigate some of the parasitics from the RF signal pad, ESD diode, and wire bonds is a circuit technique known as inductive degeneration, commonly used in low noise amplifiers at high frequencies. This technique improves the matching network between the amplifying stage and the external source. As shown in Figure 3.7,  $L_{wb}$  is the inductance of the bond wire used to couple in the RF signal and  $C_{pad1}$  and  $C_{pad2}$  are the capacitances of the bond pad on the external transmission line and on the SiGe chip respectively, and the emitter and base inductors,  $L_E$  and  $L_B$ , respectively, are used to match the amplifier input impedance to the complex conjugate of the source impedance, which is known as inductive degeneration.

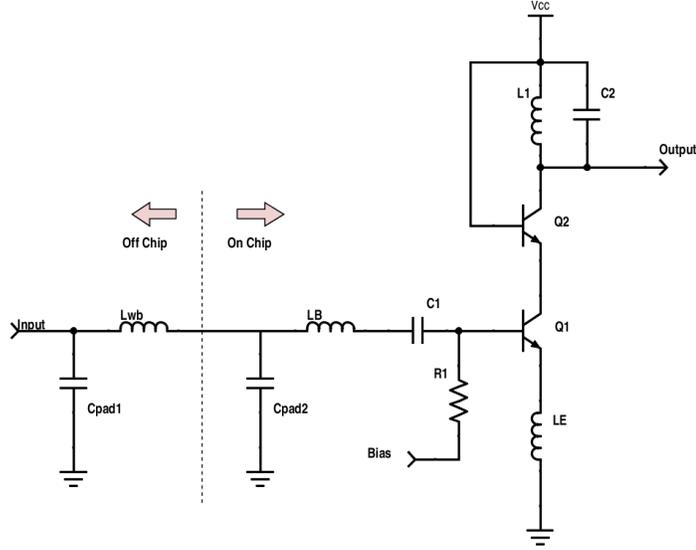


Figure 3.7: Schematic of an amplifier including the packaging parasitic components and inductive degeneration.

Looking into the base inductor of the cascode amplifier the impedance of the inductively degenerated common emitter is:

$$\begin{aligned}
 Z_{in}(s) &= r_X + r_n + sL_B + sL_E + \frac{1}{sC_\pi} + \frac{g_m}{C_\pi} L_E \\
 &\cong r_X + r_\pi + 2\pi f_T L_E + sL_B + sL_E + \frac{2\pi f_T}{sg_m}.
 \end{aligned} \tag{3.14}$$

Using  $s = j\omega = j2\pi f$ , the input impedance as a function of frequency is

$$Z_{in}(jf) \cong r_X + r_\pi + 2\pi f_T L_E + j \left( 2\pi f L_B + 2\pi f L_E - \frac{f_T}{f g_m} \right). \tag{3.15}$$

If we ignore the pad capacitance and the wire bond inductance the source impedance,  $Z_0$ , is simply a real 50 ohm impedance. Therefore, to match real and imaginary parts of  $Z_{in}$  to the complex conjugate of the source impedance,  $Z_0$ , we have the following equations:

$$r_X + r_\pi + 2\pi f_T L_E = Z_0 = 50\Omega, \tag{3.16}$$

$$2\pi f L_B + 2\pi f L_E - \frac{f_T}{f g_m} = 0. \quad (3.17)$$

Using equation 3.16 we can see that the emitter inductance should be

$$L_E = \frac{Z_0 - (r_X + r_\pi)}{2\pi f_T}. \quad (3.18)$$

The base inductance is then given by solving Equation 3.17 to arrive at the following

$$L_B = \frac{\frac{f_T}{f g_m} - 2\pi f L_E}{2\pi f} = \frac{f_T}{2\pi f^2 g_m} - L_E. \quad (3.19)$$

If we add the bond pad capacitance and the wire bond inductance brought on by packaging the circuit as shown in Figure 3.15 to the source impedance we get the following for  $Z_S$ :

$$Z_S(s) = Z_0 \chi_{C_{pad}} + s L_{wb} = \frac{Z_0}{1 + s Z_0 C_{pad}} + s L_{wb} = \frac{Z_0 - s^2 Z_0^2 C_{pad}^2}{1 - s^2 Z_0^2 C_{pad}^2} + s L_{wb}. \quad (3.20)$$

The real and imaginary components of the source impedance as a function of frequency can then be derived by multiplying the numerator and denominator of Equation 3.20 by the complex conjugate of the denominator to achieve

$$Z_S(jf) = \frac{Z_0}{1 + (2\pi f)^2 Z_0^2 C_{pad}^2} + j \left[ \frac{(2\pi f)^2 Z_0^2 C_{pad}^2}{1 + (2\pi f)^2 Z_0^2 C_{pad}^2} + 2\pi f L_{wb} \right]. \quad (3.21)$$

Equating the input impedance to the conjugate of this new source impedance results in the following two equations:

$$r_X + r_\pi + 2\pi f_T L_E = \frac{Z_0}{1 + (2\pi f)^2 Z_0^2 C_{pad}^2}, \quad (3.22)$$

$$2\pi f L_B + 2\pi f L_E - \frac{f_T}{f g_m} = \frac{(2\pi f)^2 Z_0^2 C_{pad}^2}{1 + (2\pi f)^2 Z_0^2 C_{pad}^2} + 2\pi f L_{wb}. \quad (3.23)$$

Rearranging equation 3.22 we find that the emitter inductance is now given by

$$L_E = \frac{\frac{Z_0}{1 + (2\pi f)^2 Z_0^2 C_{pad}^2} - (r_X + r_\pi)}{2\pi f_T} = \frac{Z_0}{2\pi f_T (1 + (2\pi f)^2 Z_0^2 C_{pad}^2)} - \frac{(r_X + r_\pi)}{2\pi f_T} \quad (3.24)$$

and the new base inductance becomes

$$\begin{aligned}
L_B &= \frac{\frac{(2\pi f)^2 Z_0^2 C_{pad}^2}{1+(2\pi f)^2 Z_0^2 C_{pad}^2} + 2\pi f L_{wb} - 2\pi f L_E + \frac{f_T}{f g_m}}{2\pi f}, \\
&= \frac{2\pi f Z_0^2 C_{pad}^2}{1+(2\pi f)^2 Z_0^2 C_{pad}^2} + L_{wb} - L_E + \frac{f_T}{2\pi f^2 g_m}. \tag{3.25}
\end{aligned}$$

It is obvious that packaging and the wire bond inductance plays a significant role in the performance of a millimeter wave amplifier. For this reason, ribbon bonds or multiple wire bonds in parallel are often used.

Now, to view noise figure as a whole for the full multistage amplifier. For a multistage amplifier, the noise figure is contributed most by the front end and the first gain stage. Equation 3.26, is a representation of noise factor of multiple amplifying stages:

$$F = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \frac{F_4 - 1}{G_1 G_2 G_3} + \dots + \frac{F_n - 1}{G_1 G_2 G_3 \dots G_{n-1}}. \tag{3.26}$$

$F_n$  is the noise factor and  $G_n$  is the power gain for the  $n^{\text{th}}$  device. This relationship is known as Friis' Formula and it is evident that the noise of the first stage is most important as the effect of subsequent stages is reduced by the gain of the previous stages. For the amplifier, the first stage will be optimized to achieve noise figure minimum ( $NF_{\min}$ ).

### 3.3 Bandwidth

As defined in Chapter 2, 5 GHz or less of bandwidth is required for the imaging system. To achieve is relatively straight forward compared to obtaining low noise or high output power. The basic typology used in the design is a single-tuned amplifier, which defines the circuit to peak at specific frequency. Reduced bandwidth is conveniently achieved with the inductive load used for inductive peaking, as well from the single frequency tuned impedance matching networks.

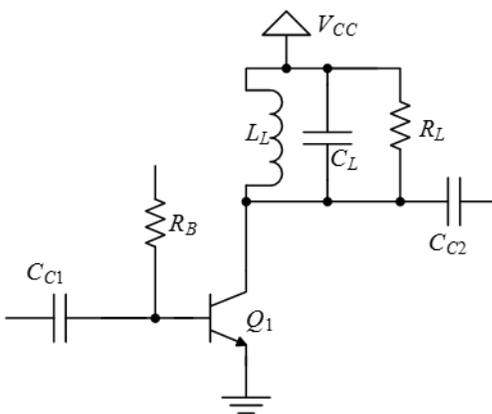


Figure 3.8: Schematic of a simple tuned amplifier design.

As shown in Figure 3.8 is a simple circuit single-tuned circuit represented by  $L_L$ ,  $C_L$ , and  $R_L$ . The parallel RLC circuit at the load is known as a tank circuit and sets the operating frequency, gain, and bandwidth of the amplifier. The voltage gain,  $A_v(s)$  is therefore a second order band pass function with a resonant frequency of

$$f_0 = \frac{\omega_0}{2\pi} = \frac{1}{2\pi\sqrt{L_L C_L}} [\text{Hz}] \quad (3.27)$$

and a bandwidth of

$$BW = \frac{1}{2\pi C_L R_L} [\text{Hz}]. \quad (3.28)$$

The  $Q$  factor of the amplifier is defined as the resonant frequency divided by the bandwidth and is therefore,

$$Q \equiv \frac{f_0}{BW} = 2\pi f_0 C_L R_L. \quad (3.29)$$

At resonance the reactive components cancel, i.e.,  $\chi_C = -\chi_L$  so that  $R_{oeff}$  is equal to  $R_L$  and the gain is equal to  $-g_m R_L$ . It should be noted that effective  $R_L$  is made up of the parallel combination of the load resistor and the output resistance,  $r_o$ , of the transistor and that  $C_L$  also includes the  $C_\mu$  of the transistor and/or a separate capacitor. From this

analysis to increase the high  $Q$ , narrowing the bandwidth of the amplifier, the effective load capacitance needs to be increased. Once we have selected the capacitance we can then choose the proper load inductance to make the circuit resonate at 95 GHz. Another benefit of a large  $C_L$  is that the resonating frequency is not significantly dependent on  $C_\mu$ .  $C_\mu$  can easily be altered during the fabrication process, and with difference in capacitance can detune the circuit to a lower or higher frequency from 95 GHz.

A second solution to reduce the bandwidth of the amplifier can be achieved by cascading multiple amplifying stages. If  $N$  identical stages are used, the overall amplifier bandwidth is given by:

$$BW_{overall} = \frac{2\pi f_0}{Q_{stage}} \sqrt{2^{1/N} - 1}. \quad (3.30)$$

The first term in this equation is the bandwidth of the individual amplifier and the square root multiplication factor is known as the bandwidth shrinkage factor. Figure 3.9 is a plot of the bandwidth-shrinkage factor for up to 10 cascaded stages.

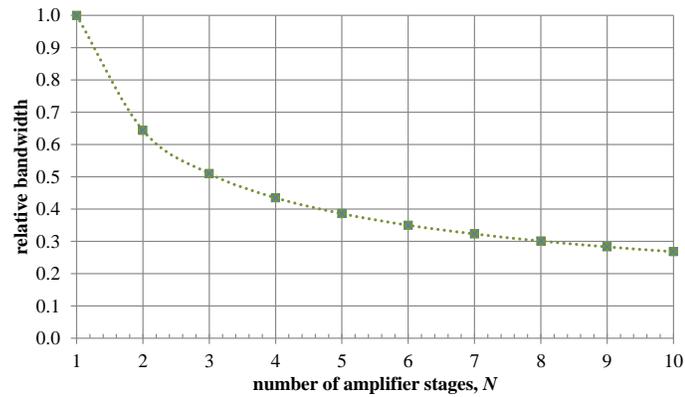


Figure 3.9: Plot of the bandwidth-shrinkage factor as a function of the number of identical amplifier stages.

It is evident that a three stage amplifier will have approximately half of the 3 dB bandwidth as a single stage design. Figure 3.10 is a plot of the normalized transfer function for one to five stages of tuned 95 GHz amplifiers. In this simulation the load resistance,  $R_L$ , is  $1000 \Omega$ , the capacitance  $C_L$  is 32 fF, and the inductance  $L_L$  is 87.7 pH. It should be noted that the load resistance plays a role in the  $Q$ /bandwidth of the stage and that this in turn may be limited by the output resistance of the transistor.

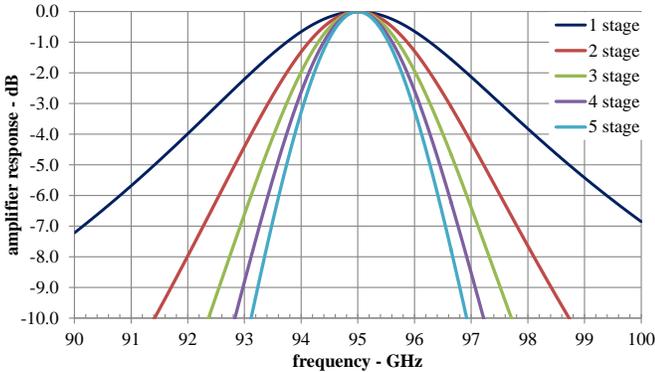


Figure 3.10: Plot showing the overall normalized response of a multistage amplifier with the bandwidth-shrinking factor.

Another effect of cascading multiple amplifier stages is that the out of band energy is more heavily attenuated. The second order response will have a roll off of 20 dB/decade or 6 dB/octave. A two stage amplifier will roll off at 40 dB/decade and each additional stage will add another 20 dB/decade of roll off. Both the RLC circuit and multiple stages amplifiers can be used to reduce the bandwidth of the LNA.

### 3.4 Interstage Matching

For a multi-stage amplifier design, to transmit the RF signal from each stage requires a matching network between stages, else the signal will be reflected back, causing loss with a decrease in gain and potentially, instability. A few steps are taken to do interstage matching: first step is to simulate the impedance at both the input and output of the amplifier typology. For this example, a cascode typology as shown in Figure 3.11a, simulated with  $V_{cc}$  set to 1.8 V, the bias at 0.95 V, with an  $L1$  set to 1 mH, and  $C1$  set to 1  $\mu$ F is used.  $L1$  and  $C1$  are large, so that they do not affect the simulated impedance at the input and output, while supplying a source to the transistor to make them active. The HBT transistor have emitter length of 3  $\mu$ m, and 2 emitter fingers, 3 base fingers, and 2 collector fingers. Simulated impedance at the input is  $0.3010 - j0.2603$  and the output is  $0.5460 - j1.5047$ .

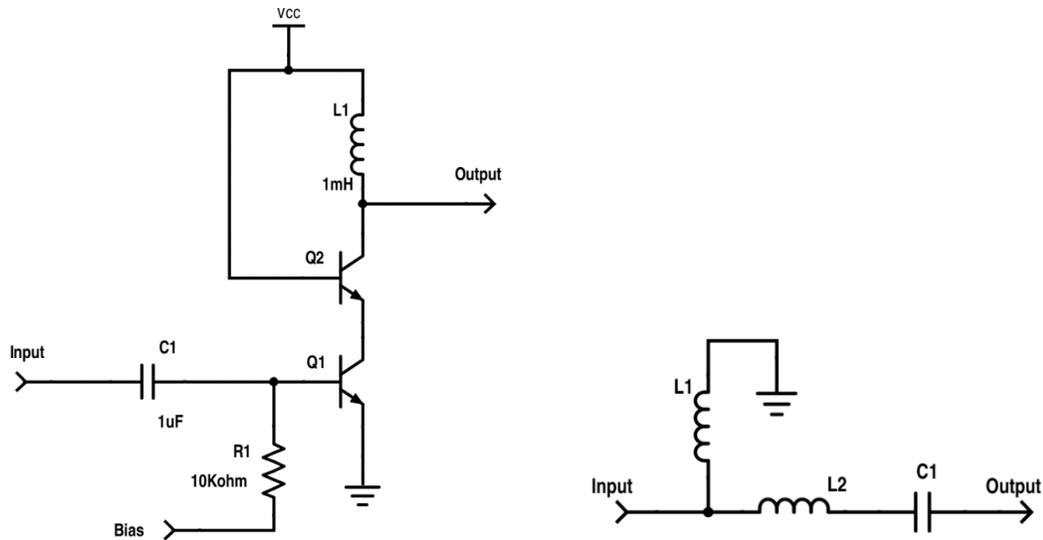


Figure 3.11: a) Basic schematic to obtain impedance at the input and output at 95 GHz, b) Simplified schematic of an interstage matching network.

Network shown in Figure 3.11b is used to demonstrate how to match the impedance between stages. This structure will be used to match the output of the amplifier, the source, to the input of the next stage, the load. An open source code that uses Mathcad®, is used to perform the impedance matching calculations. Code is supplied from circuitsage.com. [25] This software helped to find the parameters needed to match the source impedance with the conjugate of the load impedance, as shown in Figure 3.12. L1 was found to be 59.5 pH, L2 to be 68 pH, and C1 to be 20 fF. For the actual matching networks, microstrips will be used instead of inductors, but the code is capable of doing transmission lines as well. This is the technique used to impedance match between the amplifying stages for reduced loss and reflection.

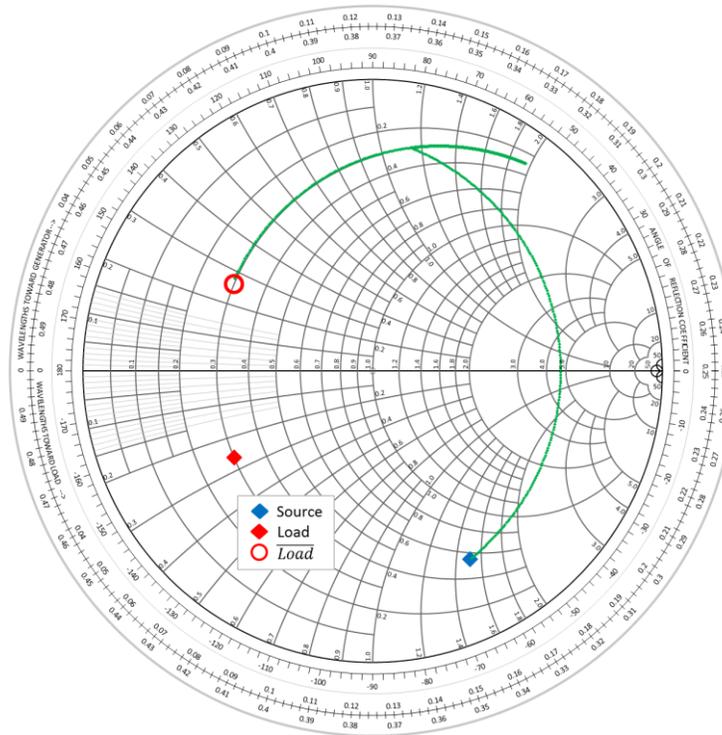


Figure 3.12. Matching network perform on a smith chart. [27-28]

### 3.5 Output Power

Mentioned in Chapter 2, greater than 3 dBm of output power is required from the LNA, a cascode topology are great for achieving high gain, but with a low supply voltage of 1.8 V to collector of the cascode, makes it impossible to have a voltage swing large enough to obtain the higher output power. In contrast, the common emitter configuration has a larger voltage swing compared to the cascode. A simple schematic of the common emitter that will be used as the output stage is as shown in Figure 3.13. The common emitter has a larger voltage swing ratio compared to the cascode because the common base of the cascode has the same base voltage as the collector voltage, which limits the output voltage swing to about half to that of a common emitter circuit. One of the negatives to the common emitter is that it supplies less gain, so this topology will only be used as the final stage of a multistage amplifier.

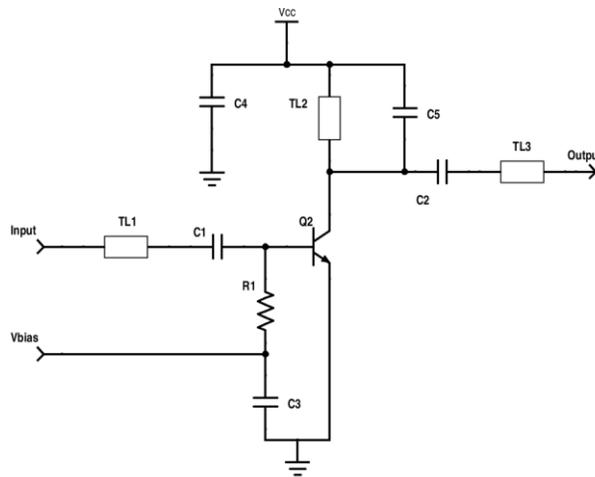


Figure 3.13: Simplified schematic of the output stage.

Obviously, not only a high voltage swing is needed, high current is also required to have high output power. To increase the output current, the emitter length of the transistor needs to increase. With a higher collector current, means a higher power dissipation, so again, only the last stage will have a larger emitter compared to the amplifying stages that come before it to keep the power consumption of the LNA to a minimum.

### **3.6 Summary**

In summary, in accordance with the requirements of the amplifier mentioned in Chapter 2, the techniques mentioned will be utilized in the amplifier design. Multiple stages utilizing the cascode typology with LC load for inductive peaking will be used for high gain and narrow bandwidth, alongside inductive degeneration in the first stage to minimize noise figure. Lastly, a common emitter stage with a larger transistor and an LC load will act as the final stage for higher output power.

## Chapter 4

### PASSIVE STRUCTURE DESIGN AND MODELING

One of the difficulties with designing a high frequency amplifier is properly designing transmission lines to traverse the microwave signal within multiple circuit applications. Along with Cadence®, Calibre® (an external software by Mentor Graphic®), used to extract parasitics of the layout can only extract resistance and capacitance parasitic, not inductance, making transmission lines difficult to be simulated. ANSYS® HFSS™ was used to solve this problem. HFSS™ is a 3-D full-wave electromagnetic field solver and was used to model many types of transmission lines for this project, which includes microstrips, coplanar waveguides, RF probes, and even capacitors.

#### 4.1 Characterization of Measured Transmission Line vs. HFSS™ Simulations

First step to characterize the transmission line was to repeat the simulated HFSS™ results with measured results of a fabricated transmission line. In one of the SiGe MPW runs, a conductor back CPW (CBCPW) that is 1,268  $\mu\text{m}$  long was fabricated and shown in Figure 4.1. The measured and simulated results show a respectable agreement, as shown with the s-parameter in Figure 4.2.

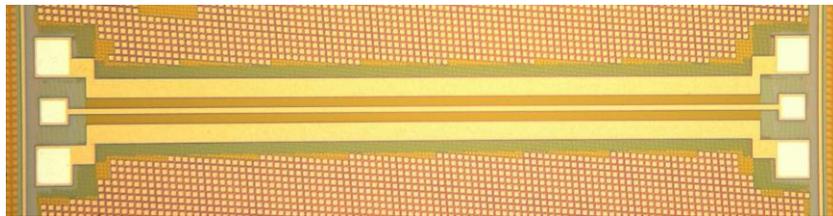


Figure 4.1: Fabricated conductor backed CPW.

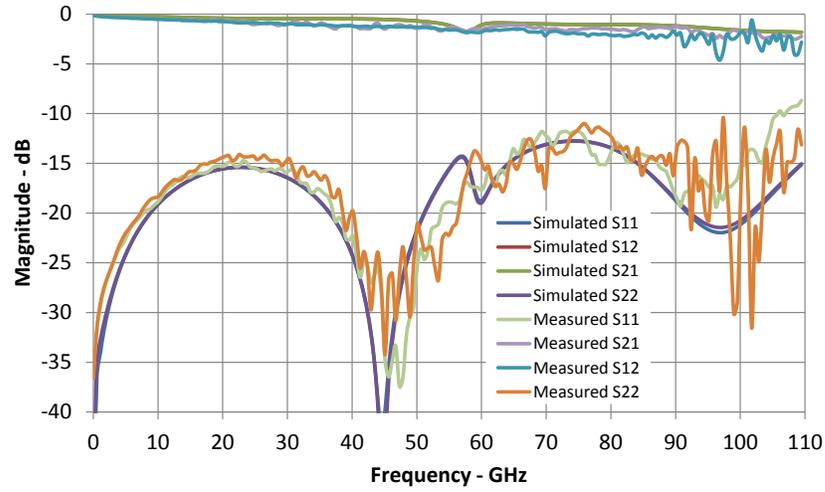


Figure 4.2: Comparison of the simulated HFSS™ model and measured data of the fabricated device.

With the measured the s-parameters, the impedance of the device can be calculated.

Impedance is calculated with the following equations:

$$Z_{in} = Z_{11} - \frac{Z_{12}Z_{21}}{Z_{22}+Z_L}, \quad (4.1)$$

$$Z_{out} = Z_{22} - \frac{Z_{12}Z_{21}}{Z_{22}+Z_S}, \quad (4.2)$$

$$Z_{11} = \frac{((1+S_{11})(1-S_{22})+S_{12}S_{21})}{\Delta_S} Z_0, \quad (4.3)$$

$$Z_{12} = \frac{2S_{12}}{\Delta_S} Z_0, \quad (4.4)$$

$$Z_{21} = \frac{2S_{21}}{\Delta_S} Z_0, \quad (4.5)$$

$$Z_{22} = \frac{((1+S_{11})(1+S_{22})+S_{12}S_{21})}{\Delta_S} Z_0, \text{ and} \quad (4.6)$$

$$\Delta_S = (1 - S_{11})(1 - S_{22}) - S_{12}S_{21}, \quad (4.7)$$

where  $Z_S$ ,  $Z_L$ , and  $Z_0$  are the source, load, and characteristic impedances, respectively, all of which are 50 ohms. Using these relationships we can plot the impedance of the

transmission lines as a function of frequency as shown in Figure 4.3. It is evident that the transmission line is close to 50 ohms throughout the entire measurement range, similar to the simulated port impedance.

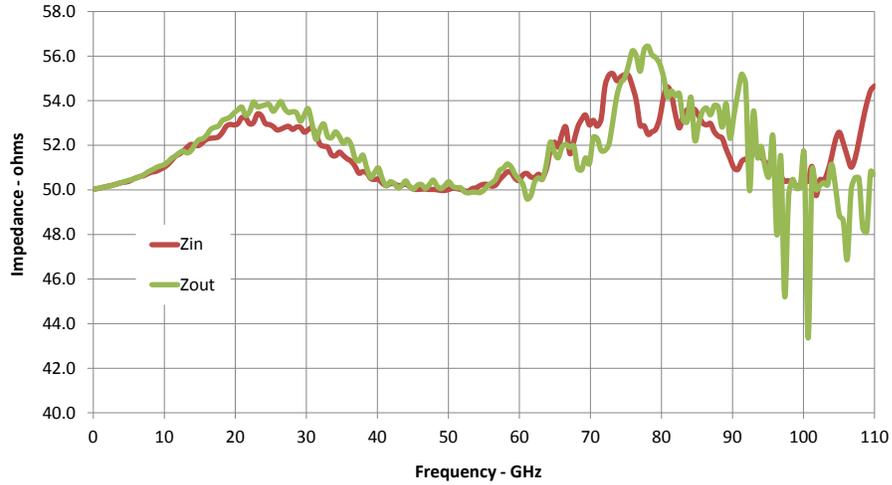


Figure 4.3: Measured impedance of the CB-CPW structure in SiGe.

## 4.2 Electromagnetic Components

### 4.2.1 Microstrip and Inductive Element

One key improvement is the inclusion of transmission line effects by modeling them in HFSS™ and then including the 2-port measurements into Cadence®. For a lossless transmission line, the impedance along the transmission line is given by:

$$Z_{in}(\theta) = Z_0 \frac{Z_L + jZ_0 \tan(\theta)}{Z_0 + jZ_L \tan(\theta)}, \quad (4.8)$$

where once again  $Z_0$  and  $Z_L$  are the characteristic and load impedances. Theta ( $\theta$ ) is the electrical length in radians and can be found as:

$$\theta = \beta l = \frac{2\pi}{\lambda} l = \frac{2\pi\sqrt{\epsilon_r}}{\lambda_0} l = \frac{2\pi f\sqrt{\epsilon_r}}{c} l, \quad (4.9)$$

where  $\lambda_0$  is the wavenumber,  $l$  is the position within the transmission line,  $\epsilon_r$  is the relative dielectric constant,  $\lambda$  is the wavelength in the medium, and  $f$  is the frequency.

If the transmission line is shorted, i.e.  $Z_L = 0 \Omega$ , equation (4.8) becomes:

$$Z_{in} = jZ_0 \tan(\theta) = jZ_0 \tan\left(\frac{2\pi f\sqrt{\epsilon_r}}{c} l\right). \quad (4.10)$$

The inductance can then be calculated with the following equation

$$L = \frac{Z_{in}}{2\pi f}. \quad (4.11)$$

It can be noted that the impedance is purely imaginary (reactance) and is a function of position and wavelength/frequency. This allows shorted transmission lines to behave as inductors at a specific frequency.

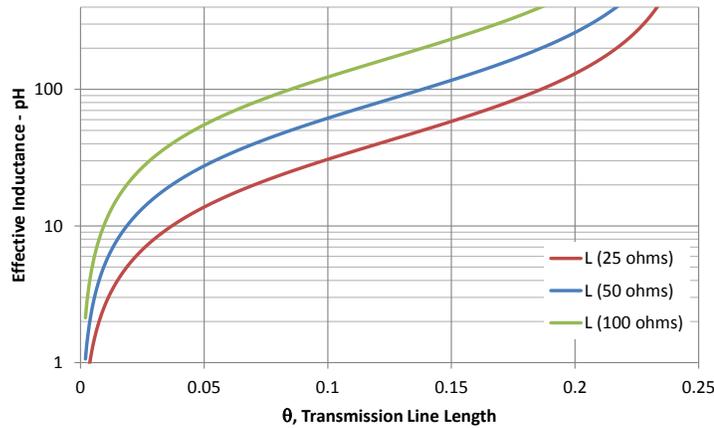


Figure 4.4: Inductance vs electrical length,  $\theta$ , for a 25  $\Omega$ , 50  $\Omega$ , and 100  $\Omega$  shorted transmission line.

Figure 4.4 is a plot of the inductance in pH of three different impedance transmission lines as a function of electrical length. In order to obtain a proper

inductance from specified length, the microstrip must be well terminated. As shown in the HFSS™ models in Figure 4.5, two microstrips were modeled with different terminations. The left model has a very small metal short between the signal and return path. The right model has a large short to terminal the microstrip. Simulating the Z-parameters of the device with HFSS™, the inductance can be calculated with  $L = \text{im}[Z_{11}]/(2\pi f)$ . As shown in Figure 4.6, is an inductance comparison of the two termination types and two different lengths and as shown as a function of frequency. It can be seen in Figure 4.6, that it is important how the microstrip is terminated, else extra inductance may be seen or other unwanted parasitics as the frequency increases. In this example, extra inductance is from the small short because it has its own inductance in series with the microstrip. At 100 GHz, there is approximately a 3-4 pH difference between the terminations types, this may not seem like much, but with a narrow band amplifier can detune the circuit to a frequency not originally simulated.

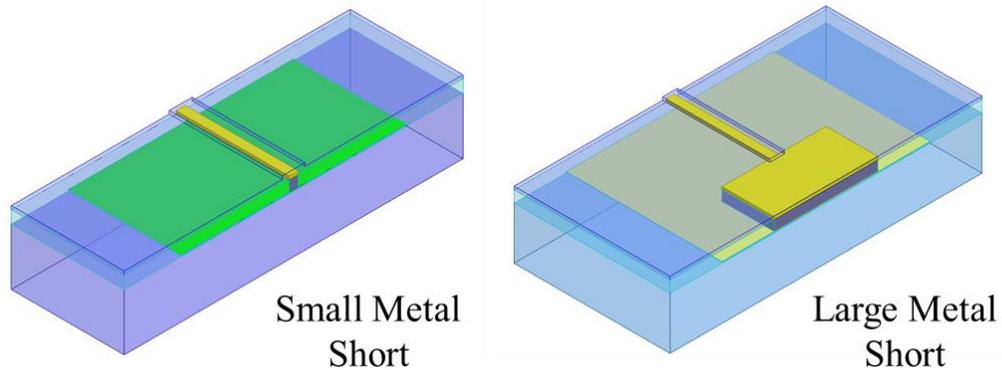


Figure 4.5: Terminated microstrip with a small metal short (left) and a large metal short (right).

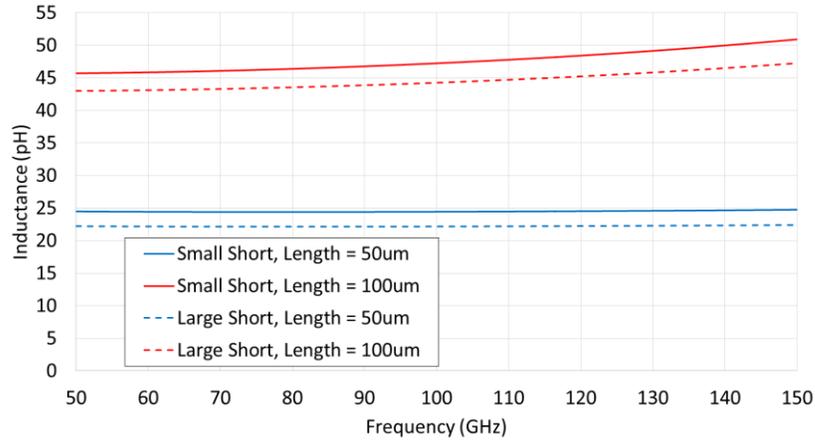


Figure 4.6: Microstrip inductance comparison of a small short vs a large short, simulation done at 95 GHz.

Unfortunately, not all the microstrips can be terminated with a metal short because a positive DC supply voltage must reach the transistors. More specifically, the load of the cascode between the supply rail and the collector. To solve this issue, a shunt capacitor can be used to block the AC signal and still allow the flow of DC current to the collector. Two HFSS™ models are shown in Figure 4.7, a large metal short on the left, and a large shunt capacitor on the right for comparing the inductance of the microstrip. A large capacitor must be used to have a low reactance at 95 GHz. Reactance of the capacitor can be calculated with  $\chi_C = 1/(2\pi fC)$  and it is desired to have it as close to  $0 \Omega$  as possible at 95 GHz. Shown in Figure 4.8, is a simulated inductance comparison of the two termination types and two different lengths as shown as a function of frequency. It can be seen there is a slight variation between the two, with a 1-2 pH difference, but still relatively close to say the microstrip is well terminated.

Variation seen in the inductance can be compensated by changing the length of the microstrip.

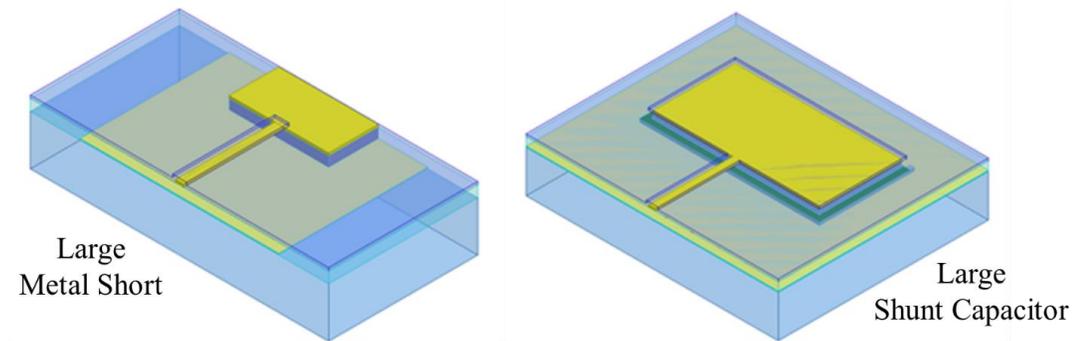


Figure 4.7: Terminated microstrip with a large metal short (left) and a large shunt capacitor (right).

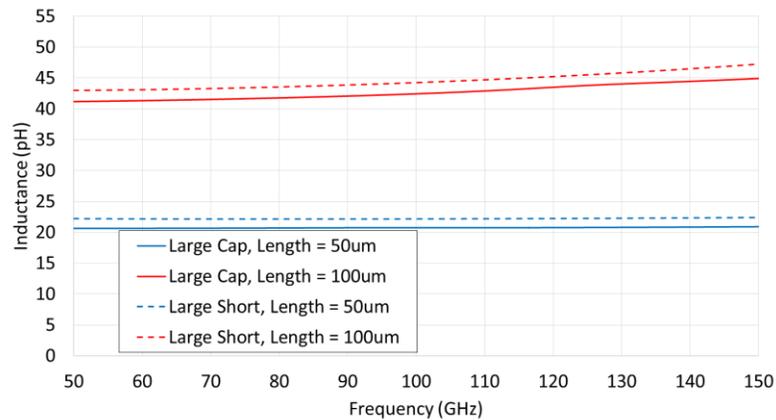


Figure 4.8: Microstrip inductance comparison of a large short vs. a large shunt capacitor, simulation done at 95 GHz.

#### 4.2.2 RF Port, RF Probe, and Wire Bond Modeling

Another important model needed is the RF signal pads, which is a CBCPW transmission line, commonly known as a ground signal ground (GSG) port. As shown

in Figure 4.9, is an HFSS™ model of the primary GSG port used in the amplifier designs. It consists a signal pad of 60 x 60  $\mu\text{m}$ , depending on the amplifier designed. Wire bonds used are 1 mil and it can increase in width when pressed against the pad surface, hence the importance of having a large pad. Spacing of the return pad and signal pad is 22  $\mu\text{m}$ . The GSG has pitch of 100  $\mu\text{m}$  for the RF probes used to measure the devices.

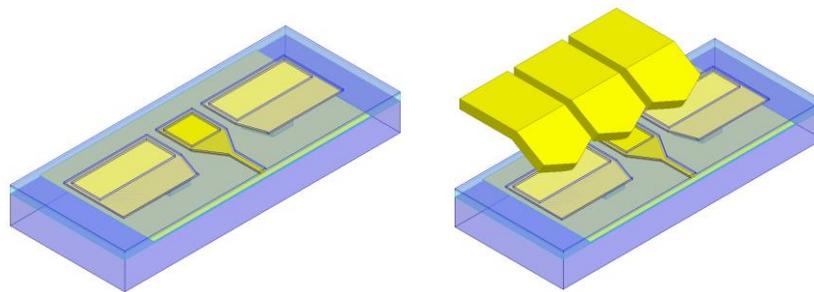


Figure 4.9: GSG port to microstrip transition without probe (a) with probe (b).

These models are used for both the input and output ports of the amplifier, but with the variation in microstrip width, depending on the impedance matching effort done for the specific amplifier. Unfortunately, due to the limitation of the width of the pad and the height between the signal pad and return path underneath, the port impedance is around 25  $\Omega$ , where we desire an impedance of 50  $\Omega$ . At 95 GHz, the GSG is fairly lossy, but it is relatively short and within reason considering the amplifier has to be packaged in order to couple in the signal to the amplifier. For the model with the RF probe, Figure 4.9b, the loss is around 1 dB at 100 GHz and is shown in the s-parameters in Figure 4.10.

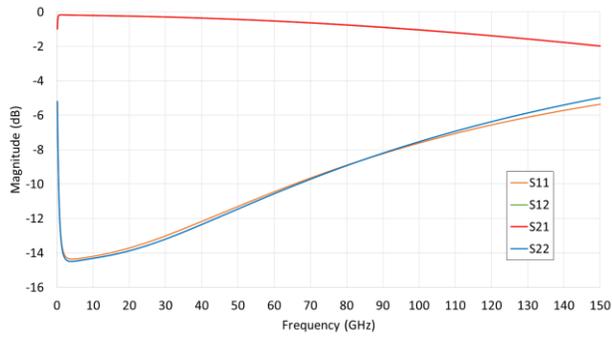


Figure 4.10: S-parameters for the model with the RF probe to GSG to microstrip transition.

Expanding from the probe model, modeled in this effort is the same GSG port, but with wire bonds to a CPW and with the RF probes on the opposite end, as shown in Figure 4.11a. The CPW is on an alumina substrate and has a characteristic impedance of  $50 \Omega$  and a length of 1 mm. S-parameters of the model is as shown in Figure 4.11b. The full structure has a loss of 1.5 dB at 100 GHz. Majority of the loss seen is from the wire bonds transitioning from the CPW to the IC. In Figure 4.11b, a standing wave can be seen, indicating reflection maybe occurring at the wire bond.

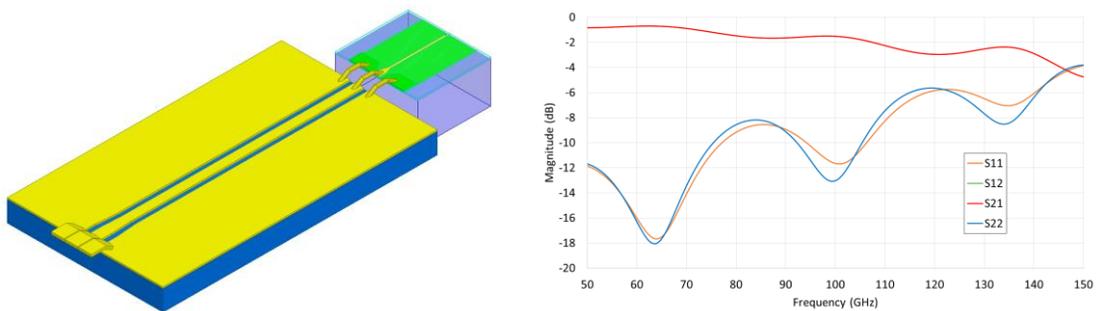


Figure 4.11: a) RF probe to CPW to wire bond to GSG to microstrip transition model, b) S-parameters of the wire bonded GSG to CPW.

### **4.3 Summary**

At the mm-wave frequency range, the electromagnetic components must be well modeled compared to the layout in order to obtain accurate results from the fabricated results. HFSS™ was a major tool to properly simulate the amplifier, without HFSS™ the circuit can easily be detuned by parasitics. As seen in Chapter 3, parasitics can effect, operating frequency, gain, noise figure and matching networks. For the discussed amplifier designs, RF ports, microstrip, probes, etc. were used to accurately simulate the LNA designs.

## Chapter 5

### FABRICATED DEVICES AND ANALYSES

#### 5.1 Single Stage Amplifier

##### 5.1.1 Purpose

The first step to designing a multistage amplifier was to develop a single stage amplifier. It is required to assure that a successful design can be created with the modeling tools available. Starting this amplifier project and throughout the development of the amplifier, Cadence® was used to design and simulate the LNA, but the simulations do not include inductance in the parasitic extraction nor did the TowerJazz kit include transmission line cells. So with the review above, HFSS™ was necessary to create accurate simulations of the amplifiers. Both Cadence® and HFSS™ are well-defined tools and have been used in many applications, but there is a higher difficulty mixing the two together. Thus, the importance to start the project with a simple single stage amplifier design and compare the measured results with the simulations was vital for accuracy.

##### 5.1.2 Circuit Description

The first submission for a single stage LNA fabricated had four amplifier configurations. One single stage amplifier was a cascode with an inductor load. Second amplifier was also a cascode, but with a microstrip load. Third amplifier was a common emitter with an inductor load. And finally the fourth amplifier was a common emitter with a microstrip load. Inductor and microstrip loads are used for inductive peaking mentioned in Chapter 3. The amplifiers, not including the inductor load, only required two transmission lines, the input and output CPW transmission line. The amplifiers with

the microstrip load obviously required three transmission lines, i.e., the input and output CPW and the microstrip load. Since the simplest way to propagate an RF signal into an IC device is through a GSG (Ground Signal Ground) port structure, it was simple to just continue the GSG port with a CPW to the base of transistor. As shown in Figure 5.1, an HFSS™ model of the transition from the GSG to the transistor, consists a taper of the signal and return path. The taper helps to improve the impedance matching to the transistor and reduce the reflection because of the slow impedance shift along the RF path. The CPW has a loss of 0.73 dB at 95 GHz from 50 ohm source and 50 ohm load.

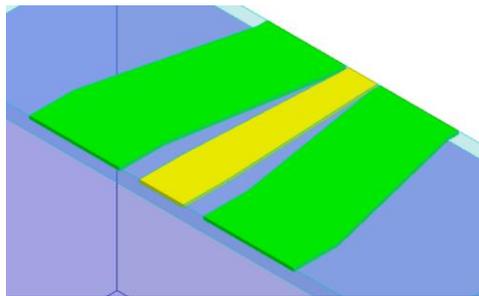


Figure 5.1: CPW input or output port modeled in HFSS™.

Microstrips were also modeled in HFSS™, but the length first needs to be determined in order to obtain a specific resonance to achieve high gain at 95 GHz. In order to determine the length of the transmission line is to first determine the inductance required at L1, as shown in Figure 5.2, to obtain the peak gain at 95 GHz. A simulation sweep of the inductance was then performed in Cadence® until a gain peak formed at 95 GHz.

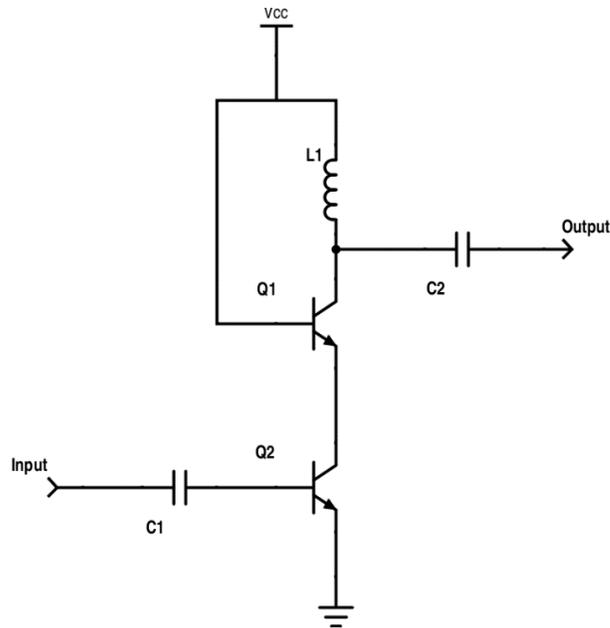


Figure 5.2: Simple schematic of a cascode with inductive peaking.

Using the equations described in Chapter 4, the microstrip length can be calculated after determining the required inductance. With the determined length, the model was created in HFSS™ and the S-parameters were transferred to Cadence®. As for the two amplifiers with an inductor, the smallest TowerJazz inductor available in the kit was used to obtain the high gain. For the four amplifier design, a current mirror was used to bias current to the base of the amplifier as well as used for isolation.

### 5.1.3 Simulated and Measured Results

The set of amplifiers were labeled AFR0713. Simulated data is shown in Figure 5.3 with collected data shown in Table 5.1.  $S_{12}$  (reverse isolation) for all of the designs is below -100 dB, so it has been removed to not over crowd the plot.

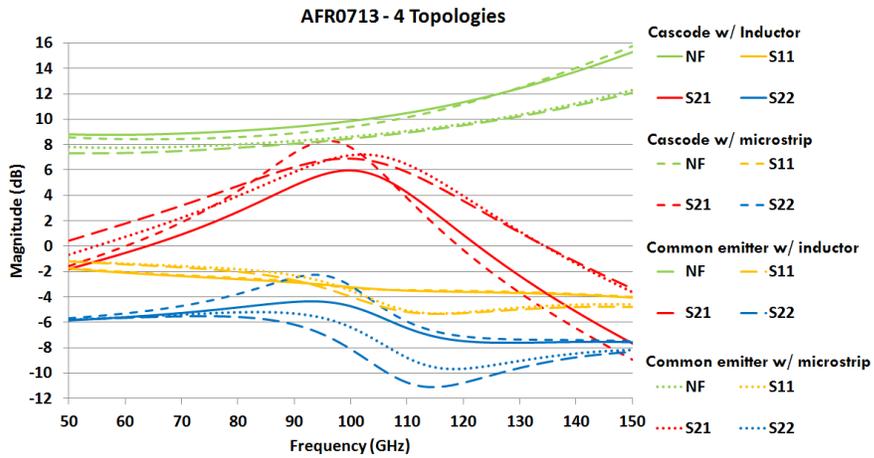


Figure 5.3: Simulated data for AFR0713.

The cascode with the microstrip line load had the highest gain of the four, but has a higher noise figure. The common emitter with the inductor had the lowest noise figure. Although the common emitter with the microstrip had a higher noise figure to the one with the inductor, it only has 0.2 dB higher noise figure while the gain is 0.3 dB higher.

Table 5.1: Performance characteristics of the SiGe LNA set.

Topology	Peak frequency (GHz)	Gain (dB)	Noise figure (dB)	3-dB BW (GHz)	Power dissipation (mW)
Cascode w/ inductor	100	5.9	9.8	32.7	17.0
Cascode w/ microstrip	96	8.4	9.2	23	16.3
Common emitter w/ inductor	99	6.9	8.5	44.0	20.7
Common emitter w/ microstrip	102	7.2	8.7	38.0	20.6

AFR0713 was personally received at the TowerJazz foundry in Irvine, California. The amplifiers went through various forms of analyzes and it was found the cascode with microstrip load had the best performance of the batch, while the amplifier with the inductors significantly detuned and was oscillating and the common emitter with the microstrip load had low gain, so only the cascode with microstrip load is discussed in this section. The measured vs. simulated results for the cascode with microstrip load are shown in Figure 5.4 and with collected results listed in Table 5.2 show a resembling match except for S12, because of the limitation of the PNA calibration noise floor.

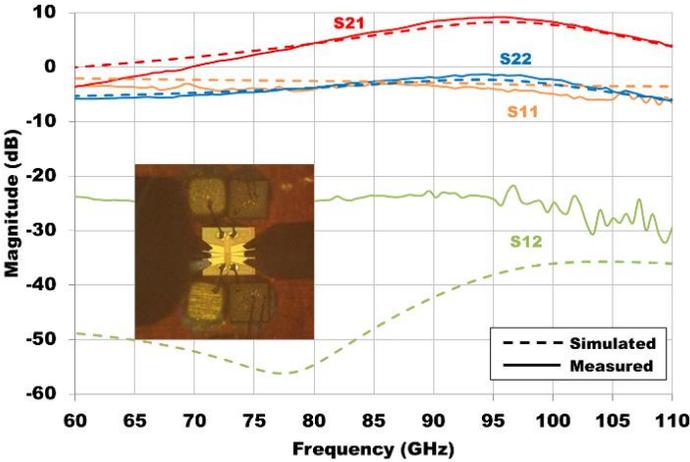


Figure 5.4: Simulated and measured S-parameters for the cascode with microstrip load.

Table 5.2: Comparison of measured and simulated parameters.

	Peak frequency (GHz)	Gain (dB)	3-dB BW (GHz)	Power Dissipation (mW)
Simulated	96.0	8.40	22.40	16.98
Measured	95.7	9.18	20.85	16.39

S11 and S22, have a poor impedance matching at both the input and output ports of the amplifier. The GSG transition is not optimal in this design for max transfer of the energy in and out of the amplifier. This will be improved in the upcoming designs.

The stability can be calculated from the s-parameter results using the K-factor, or Rollett's Stability Factor from a 1962 IRE paper by John Rollett. The K-factor can be derived from the s-parameter data using the following equations:

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{21}S_{12}|}, \quad (5.1)$$

$$\Delta = S_{11}S_{22} - S_{21}S_{12}. \quad (5.2)$$

An alternative stability factor, used in the Cadence® environment, is B1f where

$$B1f = 1 + |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2. \quad (5.3)$$

For an amplifier to be unconditionally stable,  $K > 1$ ,  $|\Delta| < 1$ , and/or  $B1f > 0$ . Using equations 5.1 and 5.2, a plot of the stability curve is as shown in Figure 5.5. The amplifier is well stable from 10 GHz to 110 GHz.

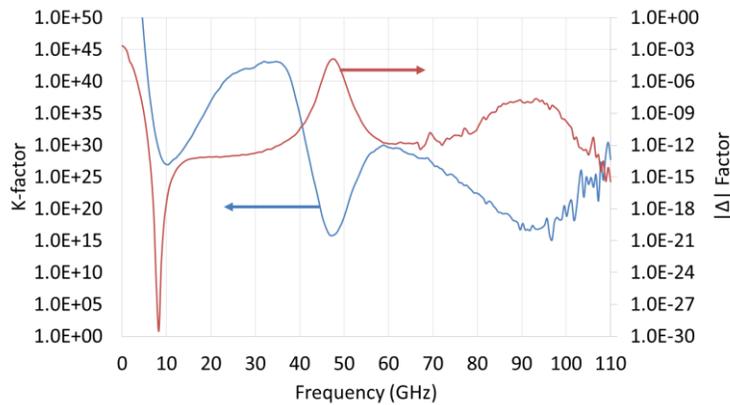


Figure 5.5: Stability curve for the single stage amplifier with microstrip load.

A temperature sweep was taken as well for the amplifier. Using a TEC to cool or heat the device, a set of data was collected as shown in Figure 5.6 and Table 5.3. The performance of the device improves as the temperature decreases as can be seen with the increase in gain. Noise figure should theoretically decrease with the decrease in temperature, but noise figure analysis was not conducted with these amplifiers because the simulated gain was less than the noise figure, so it would be difficult to obtain accurate data.

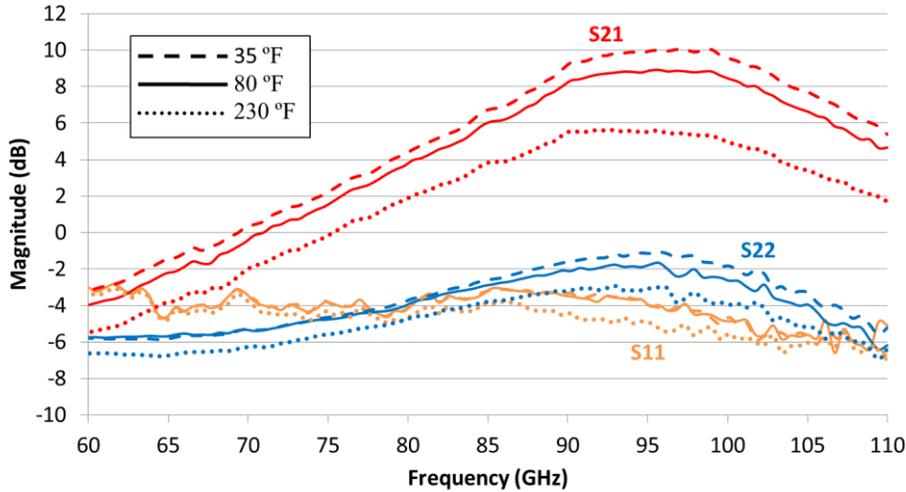


Figure 5.6: S-parameter of the amplifier through a temperature sweep.

Table 5.3 Collected performance of the amplifier under varies temperatures

Temperature (°F)	Peak frequency (GHz)	Gain (dB)	3-dB BW (GHz)
35	95.7	10	20.35
80	95.7	8.9	21.80
230	95.7	5.6	25.55

Next, analysis conducted on the amplifier was at a packaging point of view with a CPW on alumina and wire bonded to the input and output of the amplifier. This is

important to know the impact of the wire bonds. Shown in Figure 5.7 is the collected S21 data through a base bias current sweep as well as an image of the package single stage amplifier.

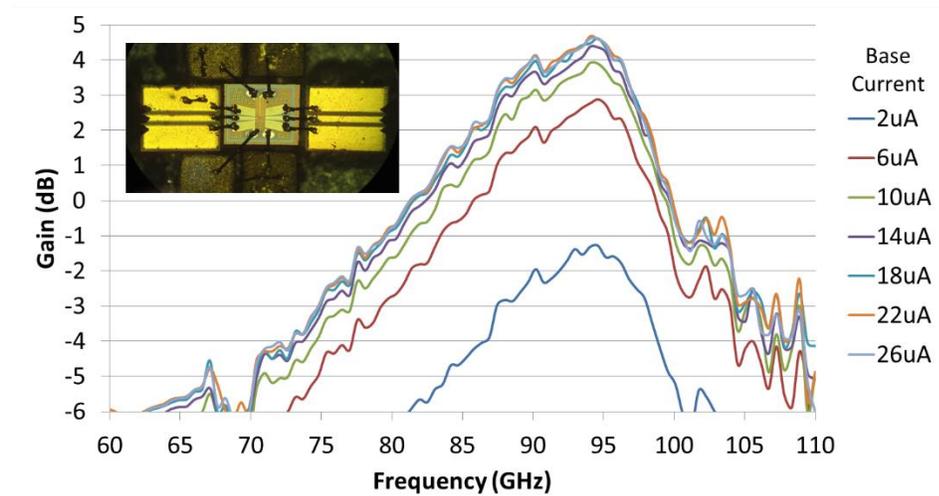


Figure 5.7: Measured S21 of the amplifier with an Alumina CPW at the input and output with wire bonds.

The gain was significantly impacted from the wire bonds. Wire bonds act as a series inductor in the RF path causing poor impedance matching and reflection of energy back to the source. Peak gain seen was 4.7 dB at 95 GHz with a 13.2 GHz 3-dB bandwidth. This suggests an approximate loss of 2.0 – 2.2 dB across each wire bond.

Using Cadence®, Calibre®, HFSS™, and the TowerJazz SBC18H3 SiGe BiCMOS kit we have demonstrated a single stage cascode amplifying a gain of 9 dB at 95 GHz. Results obtained from the single stage amplifier played a significant role in the development of the amplifiers following this design. With a good correlation between

the simulated and measured results, we will continue with the following designs and address the difficulties seen with them.

## 5.2 Four Stage Amplifier

Another set of amplifiers were submitted to TowerJazz for fabrication, the IC set is labeled AFR0614. This set was submitted before the return and analysis of an amplifier set labeled AFR0314, which had an error with the termination of the microstrip load. As mentioned in Chapter 4, the microstrip load must be terminated with a large capacitor, but the design had a small capacitor adding and effective length to the microstrip, causing the circuit to detune. Nonetheless, the primary design submitted in AFR0614 is a four stage LNA with the layout shown in Figure 5.8 and has given interesting results seen further in this section.

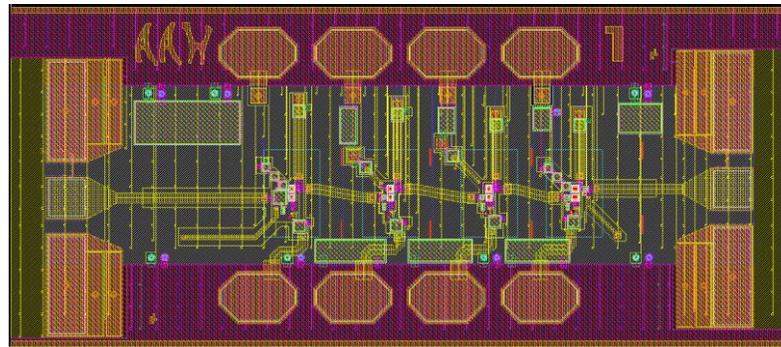


Figure 5.8: Four stage cascode amplifier with inductive peaking, degeneration, and boosting.

Difference between the four stage amplifier and the single stage amplifier is that emitter followers were not used to do impedance matching, cutting the power consumption by half. By removing the emitter follower, impedance matching between the collector of

the cascode to the base of succeeding cascode stage became difficult. As mentioned in Chapter 3, the microstrip used for inductive peaking then becomes part of the interstage matching network when the emitter follower is removed, causing additional difficulty when defining the peak frequency and interstage matching. A simplified schematic of the series-shunt network used for interstage matching is as shown in Figure 5.9. TL2 represents the microstrip load. This new matching network becomes more sensitive to any error in the layout and fabrication of the device, but it is possible to get a matched network with careful modeling.

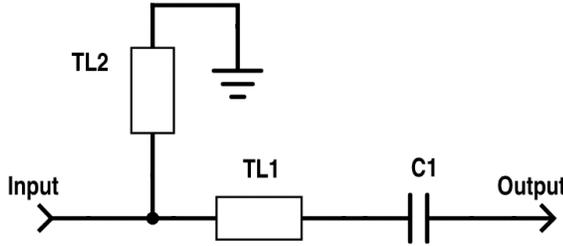


Figure 5.9: Simplified schematic of interstage matching network.

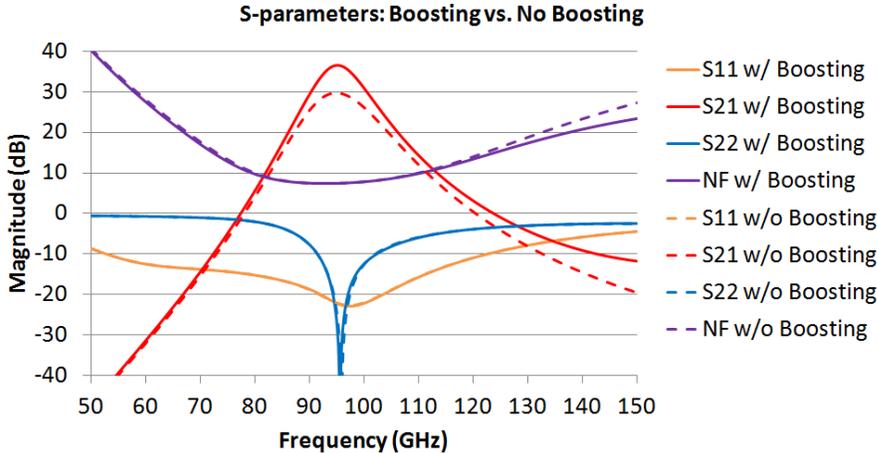


Figure 5.10: Comparison with and without inductive boosting.

Table 5.4: Simulated data comparing with and without inductive boosting.

	Peak frequency (GHz)	Gain (dB)	P1dB (dBm)	OP1dB (dBm)	Power dissipation (mW)
w/ Boosting	95.0	36.59	-36.18	-0.50	65.09
w/o Boosting	95.0	29.82	-31.09	-2.04	65.09

Another issue seen with removing the emitter follower is the reduction of gain. To compensate for the reduction in gain, inductive boosting was used in this design. Mentioned in Chapter 3, inductive boosting has the effect of causing instability, so this is a potential risk for the full design and the instability may not be seen in simulation, since Cadence® cannot accurately simulate air or semiconductor coupling. As shown in Figure 5.10 and collected data listed in Table 5.4 is a comparison of the four stage amplifier with and without inductive boosting on the two inner stages. Inductive boosting pushes the amplifier to obtain 6 dB more gain.

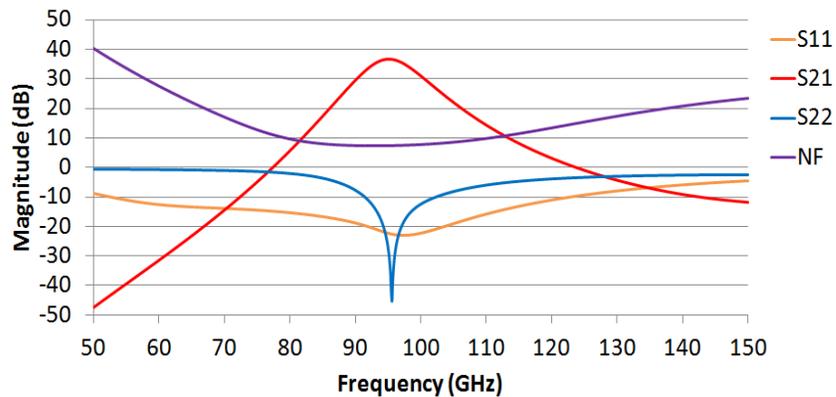


Figure 5.11: S-parameters of the simulated four stage amplifier.

Using inductive peaking, inductive degeneration, and inductive boosting, Figure 5.11 and collected in Table 5.5 shows the simulated results of the amplifier. These simulations include parasitics, and HFSS™ models for the transmission lines and RF probe to the GSG ports.

Table 5.5: Simulated data for the four stage amplifier.

Peak frequency (GHz)	Gain (dB)	Noise figure (dB)	IP1dB (dBm)	OP1dB (dBm)	3-dB BW (GHz)	Power dissipation (mW)
95.00	36.59	7.45	-36.18	-0.50	6.50	65.09

Parameters of each stage are as shown in Table 5.6. Stage one does not use inductive boosting because it degraded the noise figure at the first stage. Similar for the fourth stage, with inductive boosting, the output power degraded, so it also doesn't have the extra inductance. One of the benefits of not having the emitter follower is the increase of output power, because the emitter follower would limit this.

Table 5.6: Parameters of the amplifying stages.

	Stage 1	Stage 2	Stage 3	Stage 4
Emitter length (um)	2.9	2.9	3.0	6.0
Collector current (mA)	6.0	7.6	7.7	12.9
Collector current density (mA/um <sup>2</sup> )	15.9	20.2	19.7	16.5
Load inductance (pH)	33.6	31.8	26.5	26.5
Base inductance (pH)	None	9.7	17.9	None

As shown in Figure 5.12 is an image of the fabricated four stage amplifier, AFR0614. As mentioned above this amplifier will have a similar issue because of the capacitor size used for terminating the microstrip load. Figure 5.13 displays the measured results of the amplifier.

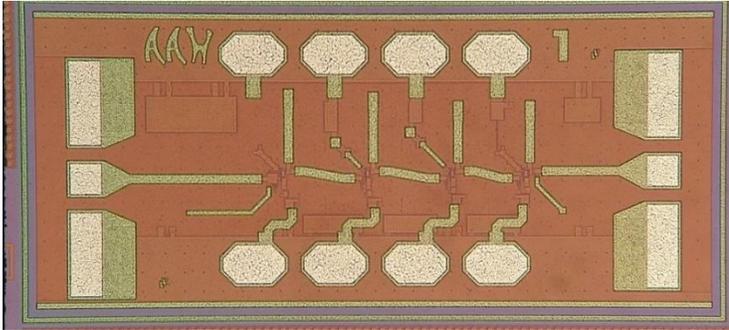


Figure 5.12: Fabricated four stage amplifier submitted in the AFR0614 set.

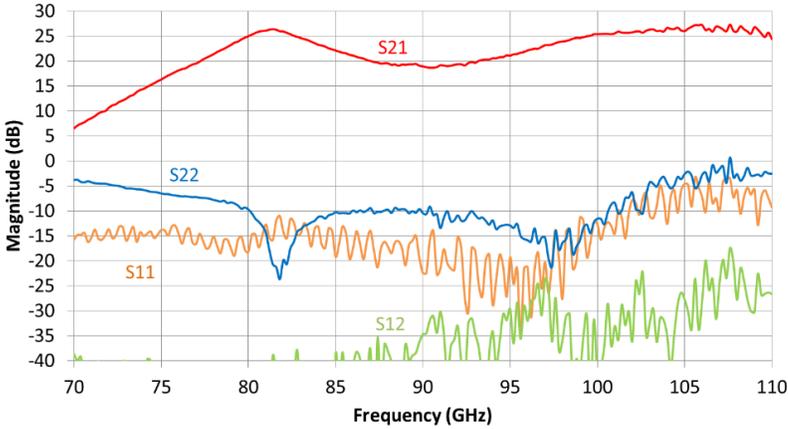


Figure 5.13: Measured S-parameter for the four stage amplifier by direct probing.

Instead of narrow-band amplification, the amplifier has a wide bandwidth, if considering a 7 dB BW. The amplifier has a gain of 20 dB at 95 GHz and about 25 dB

at both 82 and 105 GHz. There is also a wide bandwidth of impedance matching at the input and output of the amplifier. The gain peak seen at 100 GHz was considered to oscillating, but as shown in Figure 5.14, the amplifier is stable according to the K-factor and  $|\Delta|$  factor through the gain bandwidth.

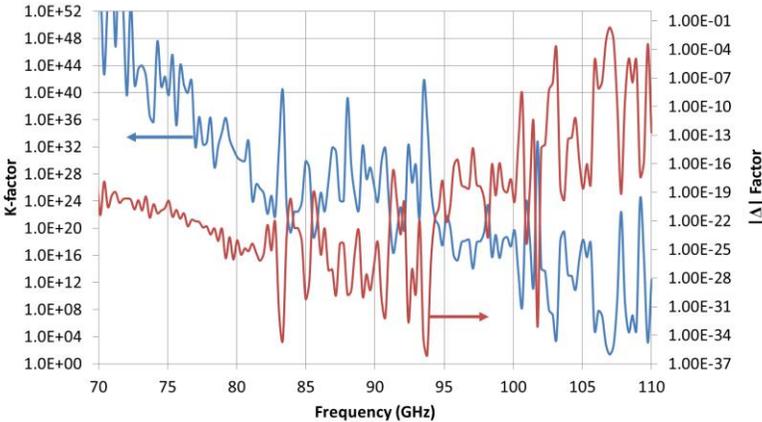


Figure 5.14: Measured stability of the four stage amplifier.

Although the amplifier did not work as expected, the amplifier has given gain through a wide bandwidth along with good S11 and S22 matching. It was decided to package this amplifier to measure the effects to the S-parameters and to be able to measure the noise figure using Y-factor technique and the 1-dB compression point. S-parameter results and images of the packaged LNA are shown in Figure 5.15. Similar to the direct RF probe results, two peaks appear on the gain curve. A few differences can be seen in the results. First, the gain is 5 dB lower, some loss is due to the adapters that transition from the standard WR-10 connector and the housing WR-10 connection,

called WR-10 flange adapters. To note, WR-10 is a rectangular wave guide that operates at 75 – 110 GHz.

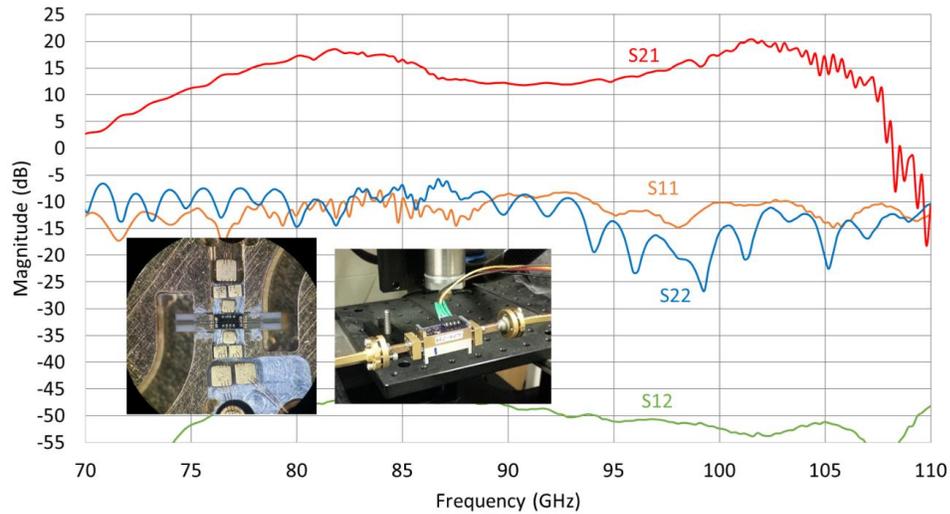


Figure 5.15: Measured S-parameter of the four stage amplifier.

Two adapters are needed, each with 0.5 dB of loss, so this adds a total loss of 1 dB. It was noted earlier in this Chapter, a single stage amplifier was wire bonded to an alumina CPW at the input and output. A loss of 2 dB from each RF wire bond transition was observed, totaling 4 dB of loss from the wire bonds. It can be said the same amount of loss from the wire bonds are seen with the packaged four stage LNA.

Next, noise figure was measured using the setup described in Chapter 6. Noise figure measurement with s-parameter data of the four stage amplifier are as shown in Figure 5.16. It can be seen that an average packaged NF of 9 dB from 72 – 100 GHz is observed. Calculating, at the front end of the packaged amplifier is 2.5 dB of loss, which

will have a direct impact to the noise figure, so with this knowledge, the noise figure will be an average of ~7 dB without packaging from 72 – 100 GHz.

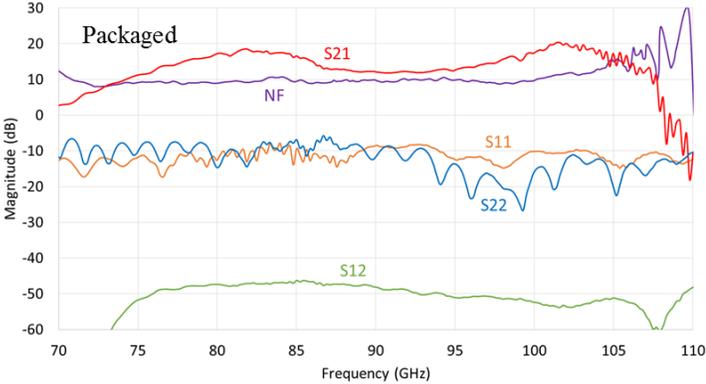


Figure 5.16: Plot of the S-parameter and NF for the packaged LNA.

Next measurement, with the setup discussed in Chapter 6, is the 1-dB compression point of the packaged four stage LNA. Output power vs. input power measurements of the packaged LNA taken at three different frequencies are shown in Figure 5.17. The input power 1-dB compression point (IP1dB) at 95 GHz was determined to be -23.9 dBm, so the output power 1-dB compression point (OP1dB) is -10.2 dBm. At both 80 and 100 GHz had higher OP1dB compared at the frequency point of 95 GHz. It is observed the max output power  $P_{max}$  at 80 GHz is higher compared to the points at the higher frequencies, this is an indication that the output amplifying stage of the LNA detuned to a lower frequency compared to the other three stages, considering the output stage was designed to produce higher output power.

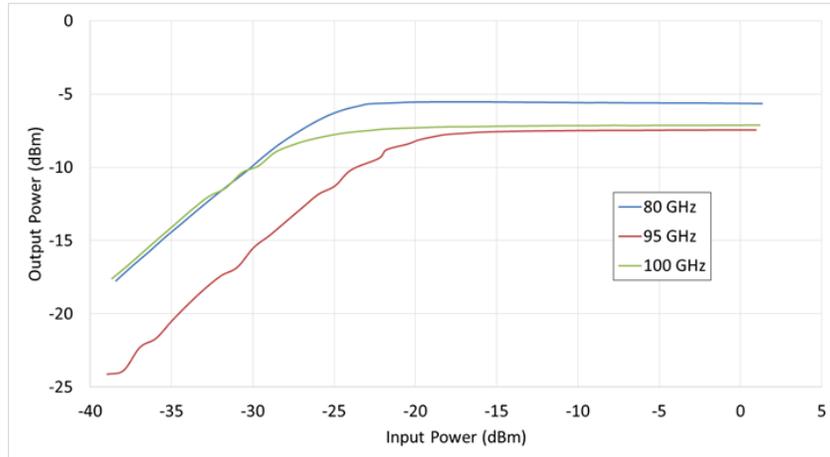


Figure 5.17: Measured output power vs. input power for the package LNA.

The four stage amplifier has given interesting results and may be useful to a user that requires a wide band or a double peak gain LNA at these frequencies. Noise figure measurement results have shown good correlation to the noise figure seen in simulations indicating accuracy of the simulation. With the knowledge collected from this design and the other design before it, was taken to the final design discussed in the next section.

### 5.3 Six Stage Amplifier

With the knowledge collected from the single stage cascode design and with succeeding multistage designs that TowerJazz fabricated, we have finalized what would be necessary to meet the requirements we have defined for this project. The final amplifier design consists of six amplifying stages, with a heterojunction bipolar transistor cascode architecture as the first five stages and with a common emitter architecture as the final stage. Layout of the amplifier is as shown in Figure 5.18.

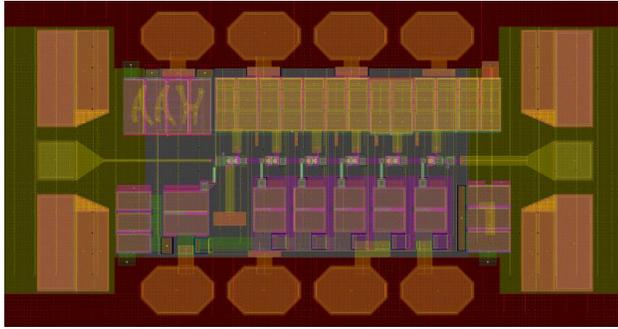


Figure 5.18: Layout of the six stage amplifier.

Cascode amplifier typology used for the first five stages is as shown in Figure 5.19, but stages 2 – 5 do not have TL1 and TL4 since they were used for inductive degeneration. As mentioned in Chapter 3, inductive degeneration is used to improve the impedance matching network at the input, while not increasing the noise figure of the first stage.

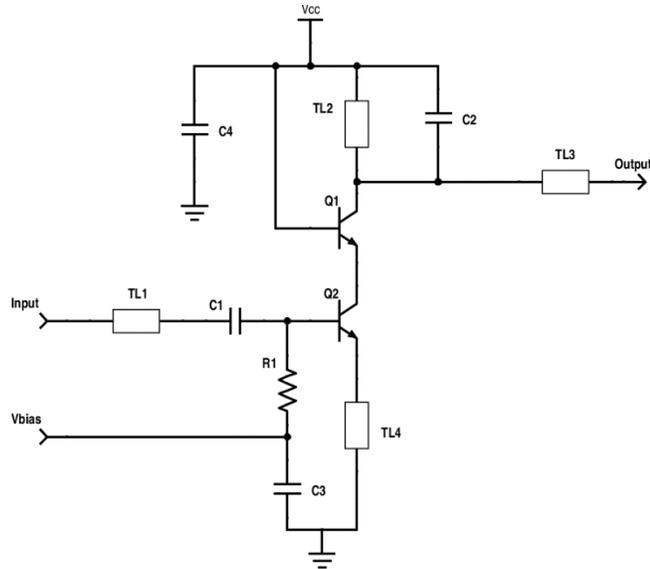


Figure 5.19: Simplified schematic of the first stage and stages 2 – 5, but without TL1 and TL4.

For stages 1 – 4, the transistors have an emitter length of 3  $\mu\text{m}$ , the fifth stage has an emitter length of 4  $\mu\text{m}$ , and the sixth stage has a length of 6  $\mu\text{m}$ , with all stages using a 232 type (described in Chapter 3) transistor. The common emitter output stage, stage 6, is shown in Figure 5.20, to obtain high output power. A voltage swing greater than 900 mV is required to get at least 3 dBm output power to a 50  $\Omega$  load. A common emitter has a larger voltage swing ratio compared to a cascode, because the common base of the cascode has the same base voltage as the collector voltage which limits the voltage swing, this is also explained in Chapter 3. The common emitter does not produce as much gain as a cascode, hence the reason it is only used as the final stage of the LNA.

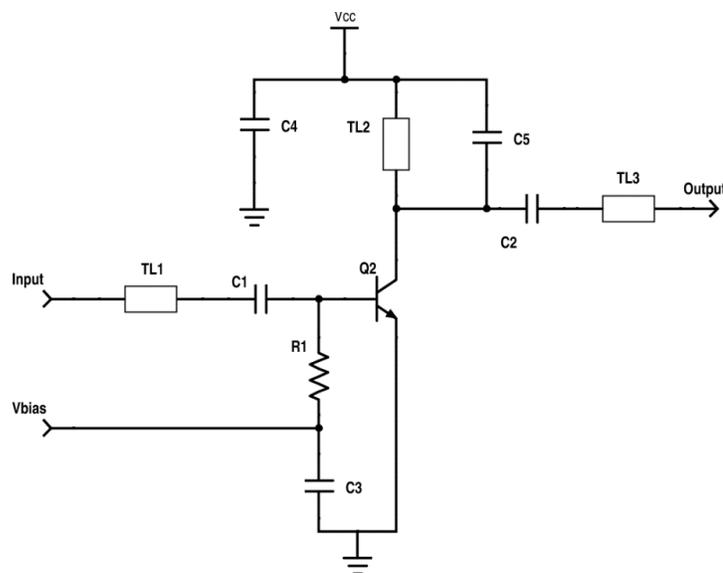


Figure 5.20: Simplified schematic of the output stage.

Similar to the previous design, the amplifier does not have emitter followers for the same reason to reduce power dissipation, so an L-network interstage matching

network was used in this design as well, but with the addition of a capacitor, C2. As mentioned in Chapter 3, one way to reduce the bandwidth is to add a capacitor in parallel with the microstrip load. The capacitor, C2, then becomes part of the matching network as shown in Figure 5.21. Additionally, the capacitance of the transistor becomes less significant to the Q of the circuit, so fabrication error should be less prominent to drift of the peak frequency.

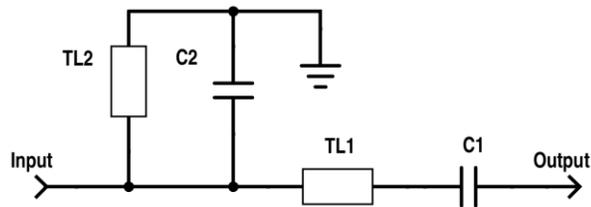


Figure 5.21: Interstage matching network with microstrip load.

The length of the microstrip load, TL2, for stages 1 – 4 and 6 is 42  $\mu\text{m}$  and stage 5 is 38  $\mu\text{m}$ . All microstrip loads have a width of 14  $\mu\text{m}$  and a height of 9.66  $\mu\text{m}$ . C2 has a capacitance of 134 fF for all the stages. To note, a simple addition to the amplifier layout, is the larger capacitors used to terminate the microstrip loads. This should prevent the onset of an additional effective length of the transmission line that would detune the circuit as seen from previous fabricated LNAs. Shown in Figure 5.22, is an ideal simulation of the described design. Simulated gain of the amplifier is 36 dB at 95 GHz, with a 3-dB bandwidth of 3.7 GHz. The noise figure is 9 dB with a good input matching network. The OP1dB was simulated to obtain +3 dBm.

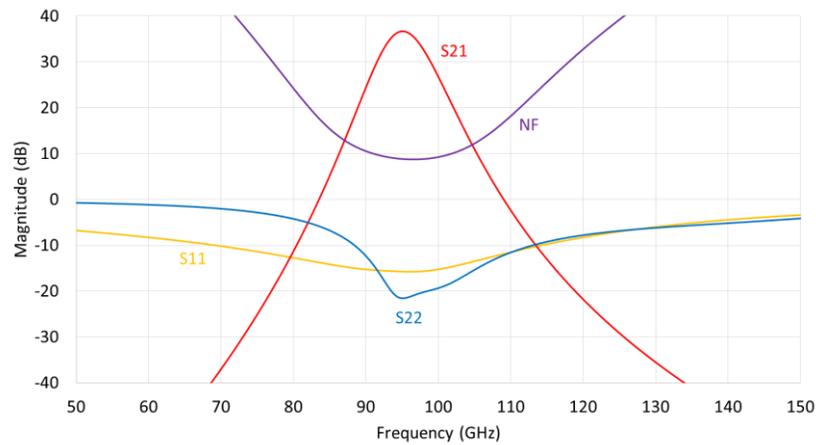


Figure 5.22: Simulation results for a five stage amplifier.

From past experience, it was best to create additional amplifiers that operated at higher frequencies in case of any drift of the peak frequency. Additionally, two amplifiers that peaks at 100 GHz and 105 GHz were created. The designs are almost identical except for the reduced length of the microstrip. Amplifier peaking at 100 GHz has a gain of 30 dB with an OP1dB of 1 dBm, and the 105 GHz amplifier has a gain of 27 dB with OP1dB of 0.8 dBm.

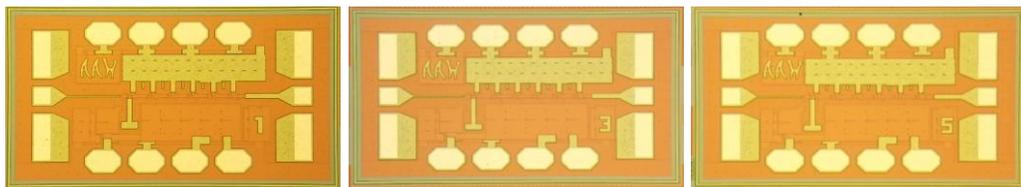


Figure 5.23: Three SiGe six stage LNAs peaking at three different frequencies.

As shown in Figure 5.23 is the three fabricated six stage LNAs that have simulated gain peaks of 95, 100, and 105 GHz. S-parameters, noise figure and 1-dB

compression results were measured for each of the amplifiers. NF in the following Figures is calculated from the measured packaged NF by subtracting 2.5 dB from 70 – 110 GHz, because of the loss measured from wire bonds and the WR-10 flange adapter described previously. Measured results for the amplifier originally simulated to peak at 95 GHz is plotted in Figures 5.24 and 5.25. As seen in the data, the peak shifted from 95 to 93 GHz. All the devices have the collector voltage set at 2 V, consuming ~ 60 mA.

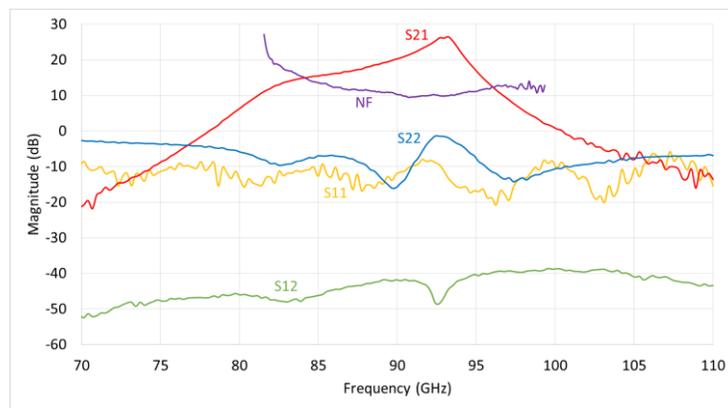


Figure 5.24: S-parameters and noise figure of directly probed ‘95 GHz’ amplifier. 2.5 dB is subtracted from packaged noise figure from calculated loss from the packaging at the input.

Maximum gain obtained from the directly probed amplifier is 26 dB, 10 dB lower than simulated, but the 3-dB bandwidth is 2.2 dB. It is seen that S22 is peaking along with the gain curve, but is still below 0 dB. This was found to be air coupling, s-parameter data from the packaged amplifier shown S22 and S11 measuring close to -10 dB, S22 was no longer peaking, and additionally gain was reduced by 9 dB, 4 dB more than expected. These are clear indications that air coupling was occurring. Noise figure is

measured and calculated to be 11 dB at 93 GHz for the stand alone device, fairly close to the simulated 9 dB noise figure. Measured IP1dB is -29.4 dBm with an OP1dB of -15.5 dBm. Measured OP1dB is much lower than the simulated +3 dBm.

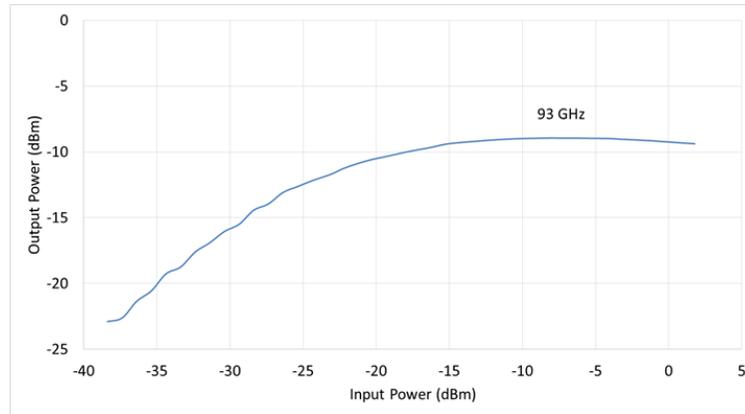


Figure 5.25: Measured output power vs. input power of the ‘95 GHz’ amplifier.

Since the peak frequency has detuned by 2 GHz, this indicates the Q of the amplifying circuit has altered. One explanation of the detuning, is the capacitance of the transistor,  $C_{\mu}$ , may have increased in fabrication compared to the models. First four stages of the LNA uses the exact size transistor, but the fifth and sixth stage transistors are larger for higher output power. The assumption, is  $C_{\mu}$  in the fifth and sixth stages had a larger impact from fabrication, causing a larger shift of the peak frequency for the individual stages. From theory, we expect stages 1 – 4 peak frequency shifted from 95 to 93 GHz and the sixth stage has detuned from 95 GHz to 85 GHz, hence the visible hump of the gain curve at 85 GHz. This also explains the reduction of OP1dB, with the increase of  $C_{\mu}$ , the matching network will detune, degrading the impedance matching, causing loss of the signal, hence reduced output power.

Continuing, shown in Figures 5.26 and 5.27, similar symptoms occurred for the 100 GHz amplifiers. The 100 GHz LNA gain peaks at 95 GHz, directly at the frequency we desire. 22 dB of gain is seen from the direct probe measurement with a 2.75 GHz bandwidth with an OP1dB of -13 dBm. Noise figure is measured and calculated to be 12.5 dB for the LNA. This LNA also consumes 120 mW of power. For third design, the 105 GHz LNA, it has shifted to 98 GHz with a gain of 13.6 dB, a measured and calculated noise figure of 12.4 dB and an OP1dB of -13.0 dBm.

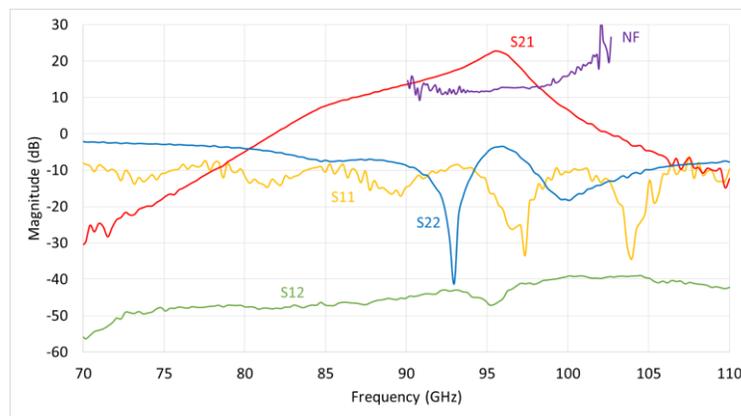


Figure 5.26: S-parameters and noise figure of directly probed ‘100 GHz’ amplifier. 2.5 dB is subtracted from packaged noise figure from calculated loss from the packaging at the input.

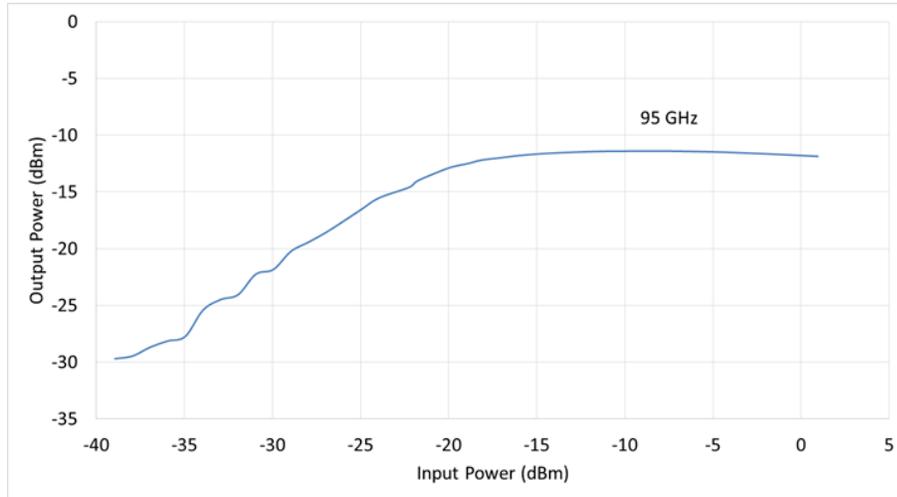


Figure 5.27: Measured output power vs. input power of the ‘100 GHz’ amplifier.

#### 5.4 Summary

A 95 GHz SiGe low noise amplifier is proposed and a fabricated device is demonstrated. The final amplifier device, after a few iterations, has achieved a 3.8 GHz narrow bandwidth at 95 GHz with a gain of 22 dB, a noise figure of 12.5 dB, and a 1-dB compression output power of -13 dBm. Some of the requirements for the amplifier were not met with the final design, the primary requirement not met being the OP1dB, but the amplifier has high gain at 95 GHz with a narrow bandwidth. Commercially available is a wideband InP amplifier with high gain at 95 GHz with an OP1dB of close to 3 dBm. As mentioned in Chapter 2, there is no commercially available narrow-band amplifiers, making the SiGe amplifier highly desirable solution for the front-end receiver module. Also mentioned in Chapter 2, three LNAs will be used to obtain enough gain, the SiGe will be used as the second LNA to narrow the bandwidth, while the InP is used as the first stage and third stage for noise figure and output power, respectively.

## Chapter 6

### MEASUREMENT SETUPS

In order to properly test and characterize the designed low noise amplifiers, measurement setup were required to measure the s-parameters, noise figure, and 1-dB compression of each LNA. To determine the s-parameters, a vector network analyzer with the addition of some new techniques to DC probe the custom IC's were used. Considering that the device is a low noise amplifier, a need to measure noise is necessary even though the SiGe will not be the first stage of the front-end receiver module, as mentioned in Chapter 2. Using an optical upconversion module and the Y-factor technique, noise figure can be measured. Final setup using a power meter, the 1-dB compression point can be determined. Remainder of this Chapter is a description of the three setups.

#### 6.1 S-parameters

The first tests necessary for an amplifier is direct DC and RF probing to measure the s-parameters. As shown in Figure 6.1, is the direct probing setup (left) and a zoomed in image of the fabricated amplifier being DC and AC probed (right). A custom probe card is fabricated from a company named Accuprobe, which is used to make contact with only the DC pads and Agilent Keithley® 2401 source meters are used to bias the LNA. To couple the RF signal in and out of the amplifier, two Picoprobe® RF probes were used to sweep from DC to 110 GHz. The RF probes are then connected with Agilent's E8361C power network analyzer and N5260A and N5260-60003 millimeter head controller to measure the s-parameters of the device. This setup allows to quickly measure the DC beta of the transistor and measure s-parameters from the device without the need of dicing the individual amplifiers.

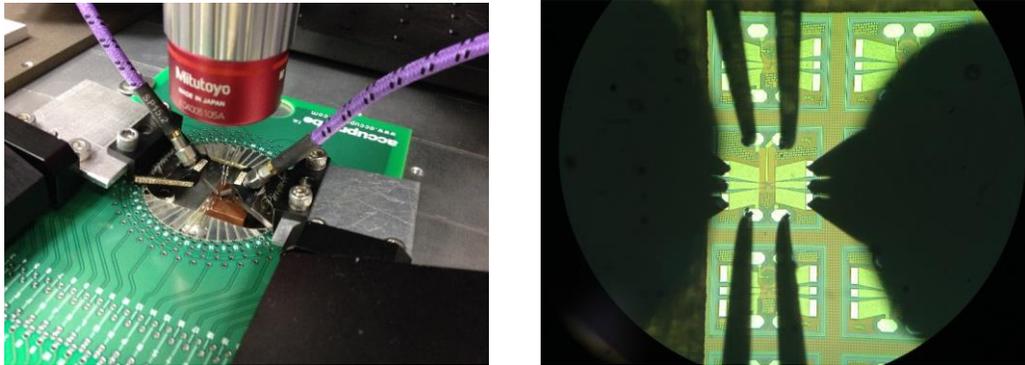


Figure 6.1: Probe card and RF probes directly contacting amplifier.

Next step for the amplifier is to package the device with wire bonds to see the effects of extra inductance either on the DC or RF path. As shown in Figure 6.2, the amplifier was diced with a Disco DAD3220 dicing saw, and wire bonded with an F&K Delvotec 56xx wire bonder with 1 mil gold ribbon wire. DC pads are wire bonded to vertical capacitors or gold bond pads, and then wire bonded to a surfboard to run 24 AWG wire to the Keithley® source meter. After this, CPWs on alumina are added at the front and back end of the amplifier, as shown in Figure 6.2. This allows us to see the impact of the series inductance across the RF signal.

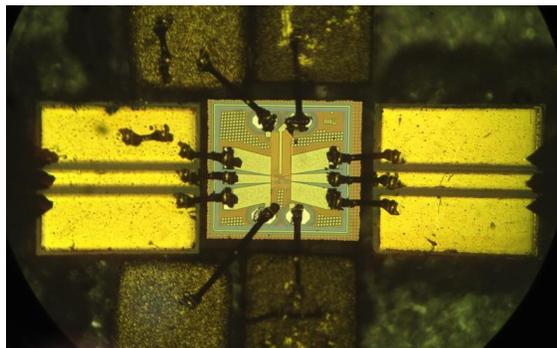


Figure 6.2: LNA DC pads wire bonded to capacitor and gold bond pad, and RF pads wire bonded to a CPW on alumina.

Next, setup involves measuring the noise figure and 1-dB compression point. In order to measure this data, UD and PSI developed a technique to gather the two measurements, but it requires to package the LNAs into an aluminum housing, that have a WR-10 input and output waveguides. An image of the packaged device is as shown in Figure 6.3. From the waveguide, the propagating mm-wave transitions into a probe, then transitions to a CPW where it is then wire bonded to the amplifier. The same steps are followed at the output, but in reverse. An aluminum top is then added to seal the device completing a packaged device, as shown in Figure 6.4. Also as shown in the Figure 6.4 is the packaged device connected to WR-10 waveguides at the input and output and then connected to the Agilent millimeter head controller to measure the s-parameters to ensure packaging was successful. To note, WR-10 flange adapter were used to connect the custom housing with the standard flange of a WR-10 rectangular wave guide. The adapter is about 1 inch long with a loss of 0.5 dB at W-band frequencies.

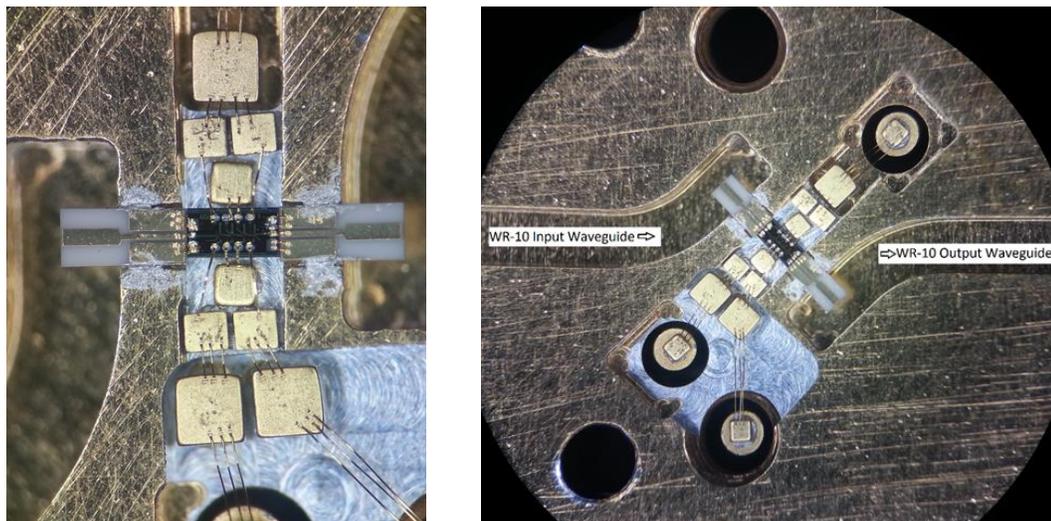


Figure 6.3: Packaged SiGe amplifier into an aluminum housing.

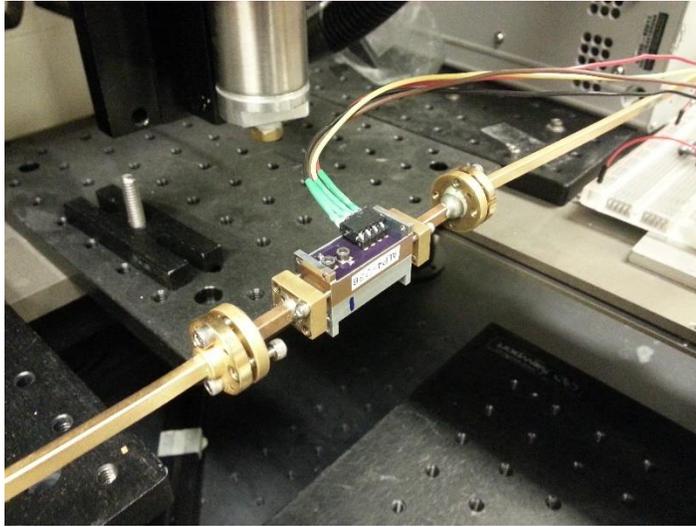


Figure 6.4: Packaged amplifier connected to a WR-10 waveguide.

## 6.2 Noise Figure

To measure the noise figure and gain of the finished packaged amplifier, a process was developed by Dr. Richard Martin that is capable of measuring the noise figure based on the optical output of an up conversion module. This measurement can be accomplished by measurement of the optical spectra of the device output as shown in Figure 6.5. The noise figure of an RF device is a measurement of the degradation of signal-to-noise-ratio (SNR) imposed by the device over an “ideal” gain device. In devices where thermal noise is the dominant contribution, which is a reasonable assumption for the radiometric devices being tested herein, a device of gain,  $G$ , can be approximated as a chain of an RF loss with a loss equivalent to the noise factor of the device,  $F$ , followed by an ideal gain stage of gain,  $G'$ . In such a case, the total gain,  $G$ , of the electronics chain is then simply  $G = G' * F = G' - NF$ , where the effective noise figure of the device is simply the decibel equivalent of the noise factor  $NF = 10\log_{10}(F)$ . Using this setup, the noise figure and the gained conversion efficiency,  $G_o$ , can be

determined, where the gained conversion efficiency is the product of the total electronic gain,  $G$ , and the conversion efficiency of the optical modulator,  $\eta$ , through a simple ratio test of the output optical power with a noise diode in the on and off states.

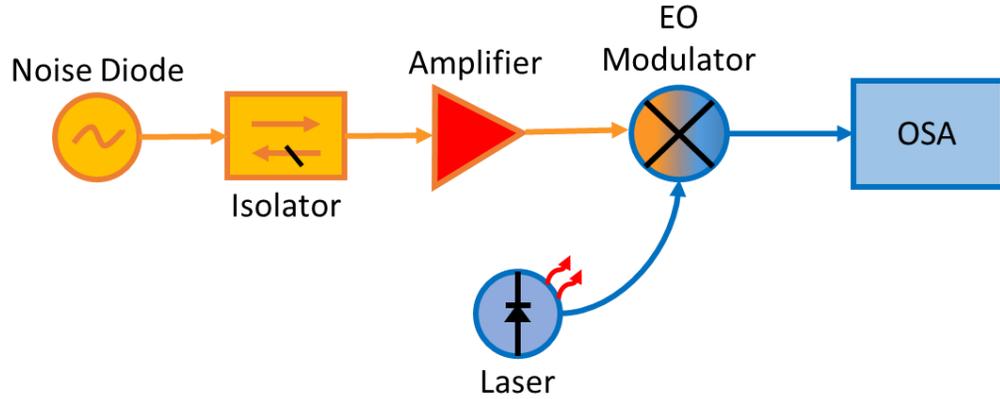


Figure 6.5: Schematic layout of Noise Figure module testing setup.

In the following section, we derive the relationships necessary to back out noise figure and gain from these tests. The method described herein is a simple adaptation of the Y-factor method commonly used to test all electrical devices on an electrical spectrum analyzer (ESA), but testing instead in the optical space using an optical spectrum analyzer (OSA). At the input plane of the amplifier, with noise diode connected to the input, the radiometric power received by the input is:

$$P_A^{off} = kT_p B \text{ and } P_A^{on} = k(ENR)T_p B, \quad (6.1)$$

where  $P_A^{off}$  and  $P_A^{on}$  represent the on and off states of the noise diode, respectively,  $k$  is the Boltzmann constant ( $1.38 \cdot 10^{-23}$  W/(K\*Hz)),  $T_p$  is the physical temperature of the device setup,  $B$  is the bandwidth over which the measurement is made, and  $ENR$  is the

equivalent noise ratio of the noise diode being used adjusted for loss in the feed setup. Assuming the noise diode is in the off state and the internal electronics of the amplifier are at roughly the same temperature, the values in (6.1) will yield

$$P_B^{off} = kT_p B \quad (6.2)$$

and

$$P_B^{on} = F * (k ENR T_p B) + (1 - F) * (k T_p B). \quad (6.3)$$

After gain and upconversion, (6.2) and (6.3) further become

$$P_D^{off} = kT_p B G' \eta P_{opt} \quad (6.4)$$

and

$$P_D^{on} = [F * (k ENR T_p B) + (1 - F) * (k T_p B)] G' \eta P_{opt}, \quad (6.5)$$

where  $P_{opt}$  is the carrier power out of the modulator. These powers can be measured directly using an OSA. The effective bandwidth of the OSA is dependent on the resolution set point of the instrument. For the highest spectral resolution, the OSA is set to 0.01 nm resolution, which corresponds to a bandwidth of approximately 1.25 GHz at a carrier wavelength of ~1550nm. Solving (6.4) and (6.5) for  $F$  and  $G_o$ , the following relationships are derived to be

$$F = \frac{\frac{P_D^{on}}{P_D^{off}} - 1}{ENR - 1} \quad (6.6)$$

and

$$G_o = \frac{P_D^{off} F}{kT_p B P_{opt}} [\text{W}^{-1}]. \quad (6.7)$$

For comparison,  $G_o$  can also be measured by switching to a narrowband output from the VNA and the output power measured on the OSA can be compared to the input power for a known input. The ratio of these two measurements, assuming that the input power

is much greater than  $kT_pB$ , is a direct measurement of  $G_o$ . To create a test setup for automated testing of noise figure and gained conversion efficiency, a LabVIEW program was designed to capture the spectra from the optical spectrum analyzer and calculate the gain and NF. As shown in Figure 6.6 is the NF setup starting with the noise diode on the right. The signal propagated through the isolator, so that no signal propagates back to the diode. Then the signal is amplified and outputted to the optical upconversion module. A laser feeds an optical signal to the input of the optical modulator and the output of the modulator is fed to the Yokogawa AQ6319 OSA.

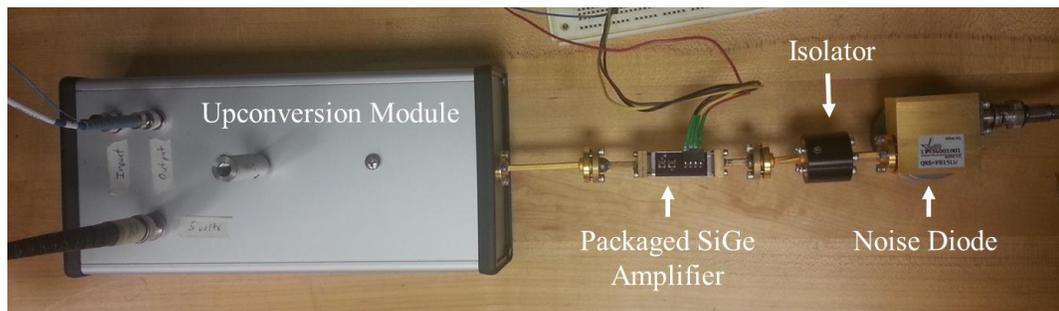


Figure 6.6: Noise figure measurement setup.

### 6.3 1-dB Compression Point

Next and final measurement setup to discuss is the 1-dB compression point measurement setup, a process also developed by Dr. Richard Martin. Schematic of the setup is as shown in Figure 6.7 and an image of the setup in Figure 6.8. Used as the mm-wave source is an Agilent 8703B Lightwave Component Analyzer along with an Agilent W85104A frequency multiplier. Following the source is an electronically controlled Millitech variable attenuator to sweep the input power to the amplifier. Following the

amplifier is an Agilent W8486A Power Sensor to an Agilent E4418B Series Power Meter to measure the output power of the amplifier.

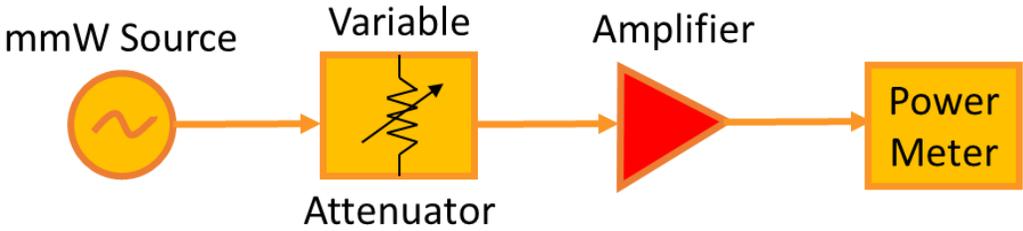


Figure 6.7: Schematic of the 1-dB compression point setup.

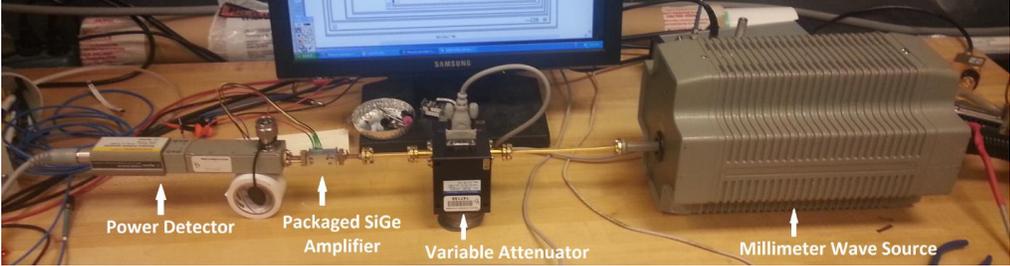


Figure 6.8: 1-dB compression point measurement setup.

LabVIEW controls and collects the data from the equipment. Output power and input power is then plotted in LabVIEW, where gain can be simply calculated with the following equation:

$$A_V = (P_{out} [dBm] - P_{in} [dBm]) [dB]. \tag{6.8}$$

With the calculated gain, when the gain drops by 1 dB after consistent gain, that is the input power 1 dB compression point (IP1dB). With IP1dB and referring to the output

power vs. input power data, the output power 1 dB compression point (OP1dB) can be determined.

#### **6.4 Summary**

In summary, this section presented the primary equipment and setups used to assist in analyzing the performance of the fabricated LNAs as well as the equipment used to package the devices. The technique used to measure noise figure and 1-dB compression is not desirable, because it requires to package the devices leading to inaccuracy to the results, but allows us to obtain a reasonable estimate to the results. In the future, it would be desirable to measure noise and compression without the need of packaging the device in an aluminum housing.

## Chapter 7

### CONCLUSIONS

In conclusion, the research efforts to fabricate and package a functional amplifier have met majority of the specified requirements. In accomplishing this task, the skills required to design, package, and properly characterize an amplifier have been learned and utilized. After a few iterations of amplifier designs using different typologies and layouts, the latest six stage SiGe low noise amplifier has the ability to be used as a front-end active component. The amplifier achieved high gain while maintaining a decent noise figure. Major benefit achieved from the SiGe LNA is the narrow bandwidth that is essential for a multi-channel mm-wave imaging applications to remove fringe washing, as described in Chapter 1. Designed to be only 1.0 x 0.5 mm in size, this amplifier has demonstrated low power consumption of around 120 mW. This is important as a multi-channel application experiences a power consumption increase of  $N$  times the power consumption of each amplifier, where  $N$  is the number of amplifiers. These devices have been packaged into usable waveguide housings for use in various applications where the key figures of merit are met with this amplifier, but current technique for packaging is not a viable solution for high quantities of front-end receiver modules. Improvements of the front-end receiver module can make the upcoming 95 GHz mm-wave imaging system a greater success.

#### 7.1 Results and Future Work

##### 7.1.1 Comparison of Expected Results

Described in Chapter 1, a 77 GHz real-time mm-wave imaging system was developed that creates images with relatively good resolution while penetrating

obscurants. By upgrading the front-end module technology to 95 GHz through the designed low noise amplifiers, the scene images will become more defined with the improvements in resolution. As shown in Figure 7.1, is an image captured by the 77 GHz imaging system. It is evident that some of the features of the object are unclear or visible, such as the rim or side mirror. It is expected with the increase in the received frequency to 95 GHz that there will be obvious improvements to the resolution of the images, making those features more distinguishable. The path forward to the new imaging system front-end module design is focused on the implementation and packaging of the SiGe LNA technology onto liquid crystal polymer that will precede an electro-optic modulator to upconversion purposes as described in earlier Chapters.



Figure 7.1: (a) Visible image of a car, (b) 77 GHz image of the same car.

### 7.1.2 95 GHz Front-End Receiver Module

Currently, ceramic substrates for the RF path and a multi-layer FR-4 PCB with the biasing and control electronics are used to package with the amplifier, which is found to be difficult and expensive. Alternate solution is a multi-layer liquid crystal

polymer substrate (LCP) that will include all of the associated circuitry. LCP is a fairly new and promising thermoplastic organic material. It can be used to fabricate high performance circuits at low cost. There is nearly a constant dielectric constant of 3.1 over the entire RF range up to 110 GHz and has a very low loss tangent of only 0.002, which increases to only 0.0045 at 110 GHz, thereby making LCP very suitable in designing mm-wave applications. This new technology will reduce weight and complexity of the packaging which directly reduces costs. With LCP and SiGe LNA technology together reduces all the parameter of SWaP-C desired and described in Chapter 1.

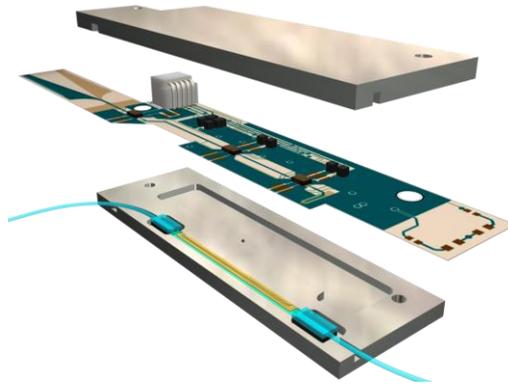


Figure 7.2: Blender model of proposed 95 GHz receiver module.

Looking at the front-end receiver as a whole, it will have a horn to collect the mm-waves where the signal then couples into the waveguide probe fabricated onto the LCP. The signal will then be amplified by an InP LNA then the SiGe LNA and finally another InP LNA where all three LNAs are wire bonded onto the LCP. To note, the SiGe LNA is still an important component for the module, because it is the only

amplifier available that peaks at 95 GHz with a narrow bandwidth with low power consumption. A narrow bandwidth is essential in order to remove fringed-washing in the captured mm-wave image. To continue, the amplified mm-wave signal then propagated from the LCP to the optical upconversion module to be up-converted to optical domain, where it then propagates through optical fibers to an infrared camera for further processing. Proposed is a 95 GHz front-end receiver module as shown in the Blender image in Figure 7.2. This is the next step for the SiGe LNA technology.

### **7.1.3 Integrated Circuit Additions**

Several additional integrated circuit ideas can be created and designed within the current SiGe amplifiers to make them more appealing to various projects of interest. Beneficial additions to upscale the performance of these low noise amplifiers would be to include a voltage regulator, temperature sensor, and frequency tunability. A voltage regulator can be added internal with the LNA, with each amplifying stage having its own voltage regulator, this will isolate each stage from one another, removing the possibility of noise propagating through the collector of the transistor of each stage or noise from the power supplies. Second additional feature that can be added is an internal temperature sensor. The 77 GHz real-time imaging system described in Chapter 1, will get hot, with an increase in temperature will change the performance of the imaging system, with a temperature sensor in each front-end receiver module, the degradation can be compensated with the additional information of temperature. A final additional feature that can be included into the amplifier design is the capability to frequency tune the gain peak. Mentioned in Chapter 1, there is multiple atmospheric transmission windows, with frequency tunability would give the capability to peer through other

atmospheric windows. These additional features can be highly desirable for the imaging systems and can be a consideration for future efforts.

## **7.2 Final Remarks**

Research efforts to design and analyze a SiGe low noise amplifier have been achieved at 95 GHz with a 3-dB bandwidth of 2.8 GHz, a gain of 22 dB, 12 dB noise figure, -13 dBm output power, and 120 mW of power dissipation. These results satisfy the necessary requirements for a viable amplifier for a 95 GHz optically addressed imaging system. Paths forward with this SiGe technology include packaging onto a front-end receiver modules and creating a large of array of the modules creating part of a real-time 95 GHz imaging system that will be capable of high resolution and low noise distortion.

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## Appendix A

### LIST OF PUBLICATIONS

#### Conference Publications

**A. Wright**, R. Martin, F. Kiamilev, J. Bai, K. Shreve, A. Mercante, Y. Zhang, C. Harrity, S. Shi, and D. W. Prather, “95 GHz SiGe LNA for Sparse Aperture mmW Imaging,” in Government Microcircuit Applications & Critical Technology Conference, 2015 GOMACTech.

R. Martin, C. Schuetz, T. Dillon, D. Mackrides, P. Yao, K. Shreve, C Harrity, A. Zablocki, B. Overmiller, P. Curt, J. Bonnett, **A. Wright**, J. Wilson, S. Shi, and D. W. Prather, “Optical up-conversion enables capture of millimeter-wave video with an IR camera,” in Defense & Security, 2012 SPIE Newsroom.

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Figure 1

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