GROWTH AND ANALYSIS OF GALLIUM PHOSPHIDE ON SILICON FOR VERY HIGH EFFICIENCY SOLAR CELLS

by

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TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

ABSTRACT

Photovoltaics research and development is marked by a continual effort to reach higher efficiencies. The highest efficiencies are achievable through the use of multijunction solar cells - devices designed to utilize the solar spectrum to its fullest potential. State-of-the-art multijunction devices are comprised of III-V materials both for the substrates and the junction layers. While these materials provide the high efficiency sought, they are also very expensive. On the other hand, other high efficiency devices utilize silicon (Si) - a material that is highly abundant and inexpensive with a well-developed technological base. The goal of this body of work is the integration of Si and III-V materials in a multijunction system for the realization of high efficiency and increased affordability.

This work is comprised of two portions. The first section is the experimental implementation of the growth of gallium phosphide (GaP) on Si through liquid phase epitaxy (LPE) based on previous foundational work. This approach provides unique challenges for the further growth of GaP or other III-V devices on a Si substrate. This body of work addresses the effects of substrate orientation, growth time, temperature, rate, and area, and principles of supersaturation. The second section is a theoretical analysis of two potential dual-junction devices: a GaP solar cell on a Si solar cell and a GaAsP solar cell on a Si solar cell.

The results of this work show promise for the future of these devices. The experimental results of this study demonstrate marked improvements in GaP buffer layer quality for subsequent layer growths. Growth procedure optimization steps

have led to a reduction of Si concentration from 20% to 3-10%. Additionally, theoretical modeling from a first principles approach shows relative efficiency gain of 20-71% and absolute efficiency gains of 3-13% for devices adding either a GaP junction or a GaAsP junction above a representative Si device. Both the experimental and the theoretical analysis shows that, while there is still work to be done to realize the goal of a high efficiency multijunction device utilizing a Si solar cell as the substrate, there is significant potential for these structures.

Chapter 1

INTRODUCTION

1.1 Purpose

The purpose of this work is the enhancement of very high efficiency silicon (Si) solar cells through the epitaxial growth of gallium phosphide (GaP) on a Si substrate and subsequent analysis of the structure. The importance of this work to the field of photovoltaics includes, but is not limited to, a pathway to the improvement of the efficiency of already high performing Si devices and a reduction in the cost of high efficiency multijunction solar cells by a replacement of expensive III-V substrates with Si.

1.2 Background

1.2.1 Efficiency as the Driving Force

Photovoltaic applications strive for the most efficient use of the sun's spectrum. Understanding why this is the case is key to envisioning further pathways for improvement upon existing photovoltaic technologies.

The future of photovoltaic energy production will be constrained by one major factor - real estate. The availability of real estate for development is dwindling, and this decrease in available space on which to install photovoltaic modules reduces the overall area covered by the modules. Solar insolation - measured in power per unit area, or $\frac{W}{m^2}$ - is a measure of how much total power is delivered by the sun that is available for capture over a given area. When the area covered by the modules is

reduced, the result is a decrease in the amount of total power that is available for capture by the system.

As an illustration of the area challenge, consider an area-constrained application such as, simply, the roof of a house. A finite number of modules will be able to fit onto the roof, and they will only be able to utilize the solar insolation that falls within the area covered by the panels. No modules can be added, and no extra solar insolation can be tapped into, resulting in a finite supply of power within the area constraints. The only way to increase the power output of the system, therefore, is to increase the conversion efficiency so that more of the input power is manifested as generated power. As energy requirements to sustain technology-driven lifestyles, and/or reduce the reliance upon energy generated from fossil fuels, grow in demand, the ability of photovoltaic systems to utilize more of the available solar insolation will also grow in importance. In order to make photovoltaic energy production in today's world feasible, therefore, the photovoltaic systems must have an increased conversion efficiency, making efficiency the driving force for photovoltaic development.

1.2.2 Pathway to High Efficiency

The development of a pathway to high efficiency involves first analyzing present photovoltaic device structures. To date, the frontrunners for efficiency are III-V Multijunction devices, followed by crystalline III-V and crystalline Si devices, with Si being the dominant market force. These three device families each have characteristics that can be combined for the advancement of photovoltaics and device efficiency.

Silicon solar cells have clear advantages over other material systems. These advantages have led to Si being the dominant presence in the photovoltaic market. Si technology is extremely well developed - and continuously improving. The Si material is abundant, robust, and inexpensive. Very high efficiency Si solar cell

devices have reached 25% [6] for laboratory devices and over 20% for individual cells at the manufacturing scale. Despite these achievements for efficient energy conversion, however, there is one downside to a single-junction crystalline Si solar cell. With a bandgap (E_g) of 1.12eV, photons with energy higher than the bandgap are not converted to electricity at their full potential.

III-V materials have higher bandgaps than Si, which allow for more efficient conversion of the high energy photons. Including the loss of lower energy photons due to transparency, laboratory single-junction crystalline III-V solar cells have reached 26.4% efficiency [6]. In addition to more effective conversion of high energy photons, III-V materials have a predictable, high open circuit voltage (V_{oc}) and high fill factor (FF). High V_{oc} and FF are essential components for very high efficiency solar cells. It has been experimentally well-documented that III-V materials have a predictable V_{oc} of E_g-0.4eV. The higher bandgap of III-V materials, therefore, ensures a high Voc for a device. Also, high Voc, due to a lateral shifting of the I-V curve, results in higher FF for devices. These three characteristics - high bandgap for more efficient conversion of high energy photons, high V_{oc}, and high FF - make III-V materials excellent candidates for use in very high efficiency solar cells. The drawback, again, is having only one bandgap available for photon conversion, as all of the lower energy photons are lost due to transparency.

Multijunction solar cells are designed with the intent to better use the higher energy photons without losing the lower energy photons. Multiple materials are layered from lowest bandgap closest to the substrate to highest bandgap at the surface of the device. The theory is that the photons will enter the device, first encountering the highest bandgap material. The photons with energy greater than, or equal to, the highest bandgap will be absorbed and generate carriers. All other photons will pass through the layer to the next bandgap material, which will absorb all photons of energy greater than, or equal to, its bandgap. Lower energy photons

pass through the layer, and the process continues until the remaining photons have passed through all device layers. This process allows for the most efficient use of the spectrum. Each range of photons is absorbed and used to generate carriers at levels comparable to the energies of the photons themselves, rather than having a single lower bangap that loses excess energy from high energy photons, or a single high bandgap that loses contributions from lower energy photons due to transparency.

Multijunction solar cells are not without their own drawbacks, however, with the main issue being cost. III-V multijunction solar cells are monolithically grown on expensive III-V substrates. While very highly efficient, the structures are cost-prohibitive for significant market penetration as long as expensive substrates are used.

The ideal device, therefore, is a combination of crystalline Si, III-V, and multijunction solar cell technologies. To this end, the proposed structure is a monolithically grown dual-junction solar cell utilizing crystalline Si as the substrate and low bandgap material, and a crystalline III-V material for the high bandgap contribution. The device would, ultimately, benefit from the technological maturity of Si, the high bandgap, V_{oc}, and FF of III-Vs, the spectrum utilization of a multijunction structure, and the cost effective replacement of a III-V substrate with Si.

The challenge, then, is to grow a III-V material directly on Si and have this layer develop into a full III-V device.

1.2.3 Why a III-V Material

There are many material options available for the cell that would be grown on Si. The decision for using a III-V material, as opposed to another, is based on an analysis of the parameters that determine efficiency - the driving force for development.

Efficiency is defined as the following:

$$\eta = \frac{V_{oc} I_{sc} FF}{P_{in}} \tag{1.1}$$

As shown in Equation 1.1, the four parameters are V_{oc}, short circuit current (I_{sc}), FF, and input power (P_{in}). The first parameter that can be eliminated from this analysis is P_{in}, as the sun is the input power source and solar insolation can be assumed to be a constant variable independent of the material chosen. The second parameter that can be eliminated is I_{sc}. In a standard multijunction solar cell, the separate active cells are connected in series, which means that the device has one shared current - the lowest current of the devices in question. There are device designs that allow us to circumvent this challenge, however, that eliminate I_{sc} as a parameter based on fundamental material properties. Only such parameters should be considered when determining which material to use. The remaining two parameters are V_{oc} and FF, which are both determined by inherent material properties, and with FF being dependent upon V_{oc}.

The V_{oc} and FF are proportional to η, which indicates that the higher the V_{oc}, the higher the efficiency of the device. The same is true of FF. There is an additional component, however, and one of great importance. The V_{oc} and FF are multiplied by each other, indicating that having both a high V_{oc} and high FF will yield even higher efficiency than having a high value in only one of the parameters. The material used above Si in this cell, then, must have both a high V_{oc} and a high FF.

The three main material systems - based upon performance - that could be a top cell over Si are CIGS, II-VIs, and III-Vs. The first of these has bandgaps that range from 1.0eV to 1.65eV, dependent upon doping. Having a bandgap near to - or lower than - the Si device beneath it would defeat the purpose of the multijunction structure. The material also does not guarantee the required high V_{oc}, as the record CIGS cell has only 0.01V higher V_{oc} than the record Si cell [6]. II-VIs have a leading

material composition in CdTe, which has a bandgap of 1.5eV. As with CIGS, the bandgap does not reach levels that are high enough to promote a high V_{oc}. The record CdTe cell has a higher V_{oc} than the CIGS cell, but it is still E_g-0.655eV, in addition to a FF below 80% [6]. Neither of these material systems display a reliably high V_{oc} coupled with a high FF, which is a requirement of this device system.

The III-V materials, however, show both high V_{oc} and high FF. As mentioned previously, III-V materials have a V_{oc} that is reliably E_g-0.4eV. This means that, with a bandgap of 2.26eV we can expect a V_{oc} of 1.86V, or a bandgap of 1.8eV to produce a V_{oc} of 1.4V. A high V_{oc} is guaranteed. In addition, the high V_{oc} also produces a high FF due to lateral shifting of the IV curve. Both conditions are satisfied.

Based upon an analysis of the parameters that determine efficiency, therefore, the III-V materials are shown to have the most controllable - and reliable - high V_{oc} and high FF when compared to rival material systems. It is for this reason that the material chosen to be grown on Si will be from this material system.

1.2.4 Why Gallium Phosphide (GaP) on Si

First, an appropriate III-V material must be chosen for epitaxial growth onto a Si substrate. There are two main characteristics that must be taken into account when deciding upon a material:

1) limited lattice mismatch with Si and

2) an appropriate bandgap for further device development.

Low lattice mismatch is a crucial requirement for any epitaxial growth process. Without low mismatching, the frequency of dislocations caused by lattice strain will be too high, destroying the efficacy of any epitaxial layer for further device development. In order to satisfy the first condition, therefore, lattice constants of III-V semiconductors were reviewed for their similarity to Si. GaP has a lattice constant of 5.4505 Å, which is a 0.36% mismatch from Si at 5.431 Å. Such a low

lattice mismatch makes GaP a good candidate for low dislocation-density epitaxial growth on Si.

For a Si bottom junction at a bandgap of 1.12eV, the bandgap required to reach the maximum efficiency for a dual-junction cell has been analyzed for different device structures, and under different spectra. There are three electrical terminal configurations that are possible for a dual-junction device, which provide varying levels of freedom for top bandgap choice when trying to reach the highest possible efficiency. These options are two-, three-, and four-terminal structures.

For a two-terminal device, the performance of the two cells is restricted by the current - shared terminals require current matching - although the device current is dominated by the lowest current of the two cells if the two are not properly matched. For this two-terminal case, using the AM1 spectrum, the calculated top bandgap to achieve an efficiency of 36.2% is 1.75eV [5]. This calculation is not realistic enough for our purposes, however, as the AM1 spectrum denotes perfect conditions on Earth - nearly impossible to achieve. Other work, using both AM1.5 direct and global, is more applicable to this analysis, and shows some variation from the AM1 calculation [14]. While the bottom junction bandgap remains close to the Si bandgap at an optimized 1.19eV for AM1.5 global and 1.00eV for direct, the optimized top junction varies from 1.80eV under global and 1.59eV under direct irradiance. These bandgap pairings yield maximum theoretical efficiencies of 38.2% and 36.2%, respectively. Both of these bangaps are much lower than the GaP bandgap of 2.26eV, and the GaP-Si pairing reaches neither the 32% nor 30% efficiency marks - the lowest demarcations on the respective calculated reference set of curves. This indicates that GaP is not adequate under two-terminal conditions as the end goal for a top junction, but this changes under the three- or four-terminal conditions.

For the three- or four-terminal device, the limitation of current matching is

removed as each cell has its own separate terminals to connect to the load. Under these conditions, the AM1 calculation shows a maximum efficiency of 36.6% with a top bandgap of 1.8eV - very close to the two-terminal system, but still much lower than the GaP bandgap. The use of a 2.26eV top bandgap, however, is shown to have a theoretical efficiency greater than 34% - a marked improvement over the theoretical efficiency with a two-terminal structure [5]. In turning again to the AM1.5 calculations for comparison, the global calculation shows a maximum efficiency of 39.1% with a top bandgap of 1.91eV and a bottom bandgap of 1.16eV. The direct irradiance calculation shows a maximum efficiency of 36.8% with a top bandgap of 1.85eV and a bottom bandgap of 1.16eV. In both cases, the GaP-Si pairing shows theoretical efficiencies of greater than 36% and 32%, respectively [14].

GaP, with a bandgap of 2.26eV, does not match the optimization criteria for either two- or four-terminal structures. Utilizing a four-terminal structure, however, has the potential to produce devices with efficiencies greater than 32%. This calculation indicates that, while GaP might not have the optimized bandgap for the top junction in the dual-junction structure with Si, there is still the potential to develop a high efficiency device utilizing this material. The ultimate benefit of utilizing GaP epitaxially grown on Si, however, does not end with the top junction of a dual-junction structure.

The greatest benefit of the GaP material is most likely its potential as a platform for further device development. GaP, with its low lattice mismatch to Si, will provide a good nucleation surface, with minimal Si interaction, upon which to grow a III-V layer that has been optimized for very high efficiency. In addition, the 2.26eV bandgap will not interfere with the transmittance of photons from the top junction to the bottom junction. If the top junction is approximately 1.81eV, it will have already absorbed any photons with energy greater than, or equal to, the bandgap - including photons of greater than or equal to 2.26eV, which the GaP

layer would absorb - transmitting all remaining photons to the Si bottom junction. The conclusion, therefore, is that the bandgap of GaP - while not optimized for a top junction in and of itself - is appropriate for further device development, thereby satisfying the second condition for material selection.

1.3 Thesis Objectives

The focus of this work will be the growth of GaP on Si and the analysis and demonstration of pathways to improvement of dual-junction solar cells implementing both Si and III-V materials. The overarching goal will be investigated through the following objectives:

1) Grow improved crystalline GaP on Si: This objective will result in improved epitaxial layer growths of GaP on a Si substrate with reduced Si concentration.

2) Design a multijunction III-V on Si: This objective will determine the layer structure of a device utilizing the GaP layer as a buffer for further III-V epitaxial layer growth.

3) Model the device: This objective will produce theoretical device parameters for the designed III-V on Si multijunction solar cell using a first principles analysis.

4) Analyze the device: This objective will use the model to compare the effects of adding a III-V top junction above a Si solar cell, determining the absolute efficiency gain from this structure.

1.4 Thesis Outline

In order to adequately discuss the objectives of this work, and their fulfillment, the following chapters will be contained herein:

Chapter 2: This chapter will be a literature review of previous GaP on Si work.

Chapter 3: This chapter will examine the process for improving an epitaxial GaP layer on a Si substrate.

Chapter 4: This chapter will present a quantitative model for, and analysis of, two III-V on Si dual junction structures using the GaP buffer layer as a starting point for subsequent layer growth.

Chapter 5: This chapter will present the conclusions of this body of work, as well as propose further research.

Chapter 2

LITERATURE REVIEW OF GALLIUM PHOSPHIDE ON SILICON

The challenge of growing GaP on Si has been addressed in literature in various stages from theoretical analysis through to experimental results. Both of these approaches prove to be very important for the understanding of the state of the art in GaP on Si technology and provide a basis for the understanding and development of this work.

2.1 Theoretical Literature

Theoretical literature on the subject is an examination of the feasibility of epitaxial growth of GaP on Si based on fundamental material properties. The capability to produce device-quality heteroepitaxial growths for specific device purposes is a non-trivial challenge, and begins with a comparison of lattice constants, then bandgaps. Lattice constants determine the potential for success in epitaxial growth, whereas bandgap evaluations determine the aptness of the material to fulfill a specific function within the device. Another crucial parameter to be examined is the coefficient of thermal expansion, which can lead to severe fabrication issues for materials that do not have similar coefficients. After reviewing these three parameters, the conclusions of theoretical literature as to the feasibility of fabrication is apparent. These material and device parameters serve both to limit the pool of acceptable material options for growth, and to demonstrate theoretical background for the state of the art for GaP epitaxially grown on Si.

2.1.1 Lattice Constant Comparison with Si

The lattice constant is the single most important parameter to consider when choosing a material for heteroepitaxial growth. A mismatched lattice, if the mismatch is too great or not properly handled, will cause dislocations that destroy an epitaxial layer's ability to perform at required device quality levels.

There is an abundance of types of semiconductor materials, however, only some are used in the fabrication of electronic devices. This, initially, narrows down the options from which to choose. In examining selected semiconductors, Corkish determines that none are completely lattice matched to Si, but that ZnS and GaP are closest, with a mismatch of 0.4% [4]. Landis *et al.* also comment that, while there are theoretical alloys using boron or nitrogen that could be used with GaP to create an exact match to the Si lattice, these alloys have not been experimentally demonstrated [11]. Other work in GaP on Si cite this low lattice mismatch as reason to attempt growth of this heterojunction [3, 8, 13].

The theoretical course taken in literature, therefore, is that GaP cannot be adjusted to be lattice matched to Si, but the mismatch is low enough that there is promise for good epitaxial growth.

2.1.2 Bandgap as a Determination of Purpose

In photovoltaic devices, the layering of the semiconductor materials according to bandgap is crucial to the function of the device. For instance, a multijunction solar cell with top, high bandgap layers switched with the bottom, low bandgap layers beneath it would not be of any use - the entire purpose of the multijunction structure would be defeated by trapping all photons in the first, low bandgap layer. Literature evaluates the bandgap of GaP with relation to Si in order to determine for which purposes it would best serve.

The options for the semiconductor layer epitaxially grown above Si examined

by Corkish are the following: form an active junction for a dual-junction monolithically grown structure, form a passivating window layer for the Si solar cell, or form a buffer layer to be used as a platform for further layer growths. GaP as a layer above Si has been theoretically evaluated for it's potential use for each of the aforementioned purposes.

A semiconductor's value for each purpose is determined based upon its bandgap in relation to the layer upon which it will be grown, or those layers that will be further grown atop it. The first purpose - an active region to form a dual-junction solar cell with Si as the bottom cell - requires a bandgap of 1.8eV to form the ideal structure as optimized for efficiency. This bandgap requirement is developed based upon current matching and first principles analysis of device operation. A passivating window layer should have a bandgap significantly higher than that of the cell beneath so as to be as completely transparent to photons as possible. If the window layer is too close in bandgap to the Si cell, it will absorb a greater number of photons that would otherwise be generating carriers in the Si, thereby degrading the final structure performance. The bandgap of a buffer layer should equal or exceed the bandgap of the active layers grown above it. When this is the case, the photons that would be absorbed by the buffer layer have already been absorbed by the active layers above it. The buffer layer is then completely transparent to the remaining photons, which are free to pass through to, and be absorbed by, the lower active layer. A visual representation of the 2.26eV bandgap of GaP as related to the 1.12eV bandgap of Si, useful for determining the best purpose for GaP, is displayed in Figure 2.1.

The three points of interest are GaP, Si, and "IDEAL," which is marked by a red dot. The point marked "IDEAL" denotes the bandgap versus lattice constant relationship that would be required for the ideal material to be used as a top junction in a dual junction device. As can be seen, GaP is located at a bandgap

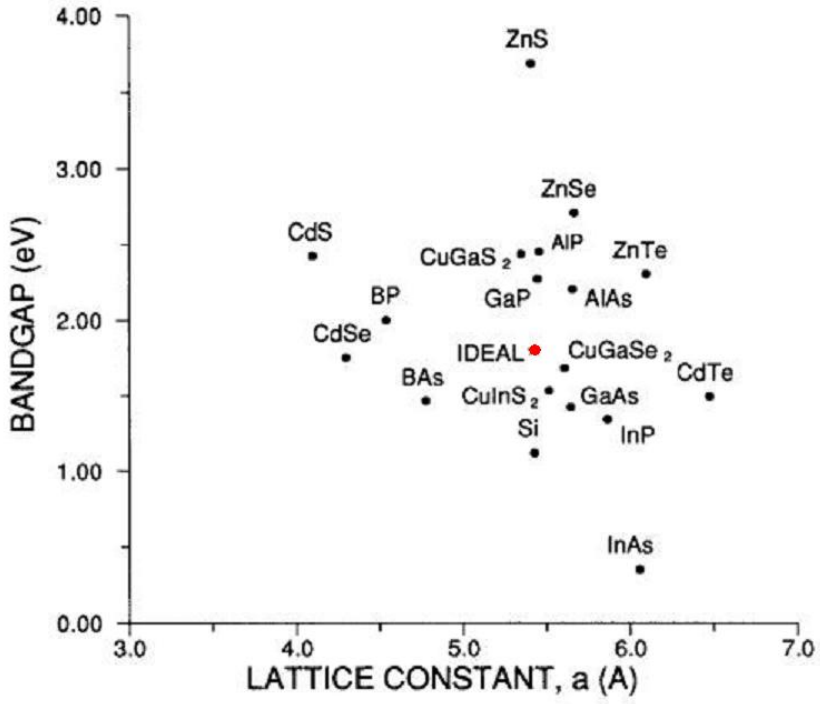


Figure 2.1: Bandgap versus Lattice Constant for Select Semiconductors [4].

well above this ideal point, indicating that the layer would fall more into the regime of passivating window or buffer layers [4, 11]. A full GaP device, however, has the potential to help address design problems that would be relevant, and useful, for the design and development of more ideal structures.

2.1.3 Coefficient of Thermal Expansion

Another critical theoretical issue mentioned in literature is the potential growth problems associated with a large difference in the coefficients of thermal expansion for GaP and Si. Si has a coefficient of thermal expansion of 2.6x10 $^{-6}$ $^{\circ}C^{-1}$, while GaP has a coefficient of 4.65x10 $^{-6}$ $^{\circ}C^{-1}$. This difference has the potential to cause cracking during cooling after growth at high temperatures [4].

2.1.4 Feasibility of Fabrication

The feasibility to epitaxially grow GaP on Si is based upon the lattice constant mismatch and the difference in coefficients of thermal expansion, while the feasibility to use GaP for specific device purposes is based on the bandgap. Other issues of fabrication come into play when considering the potential procedures involved in the fabrication of full device structures, especially with regard to the ranges in temperature required for different device fabrication stages. The fabrication of a Si solar cell occurs at temperatures that are too high for GaP to maintain stability, but GaP can be epitaxially grown on a Si substrate a temperatures that would not adversely affect devices on the Si substrate that have already been completed. The suggestion, then, is that it would be best to begin fabrication of the heterojunction with a Si substrate [3]. This provides a starting point for experimental work, and any further examination of fabrication processes should turn to experimental literature.

2.2 Experimental Literature

Theoretical evaluations of material properties and potential growth challenges are only useful up to a certain point. Once beyond that point, the only way to continue to learn and evaluate is to perform actual experiments - putting the theory into practice. The following section explores the state of the art experimentally, with a focus on our particular growth method - liquid phase epitaxy (LPE) - and the foundational work upon which this work builds.

2.2.1 Possible Growth Methods

There is an abundance of growth methods available with which to epitaxially grow one semiconductor layer onto another. The growth methods that have been used for the specific application of GaP on Si include halide transport [9], organometallic vapor phase epitaxy [17], metalorganic chemical vapor deposition

[16], chemical beam epitaxy [2], and molecular beam epitaxy [18]. For our purposes, the growth of GaP on Si through liquid phase epitaxy (LPE) has also been treated with varying degrees of analysis and success [3, 7, 8, 13, 15].

2.2.2 Liquid Phase Epitaxy (LPE)

The growth method we chose for this work is LPE, which is growth method that produces quick, yet high-quality epitaxial layers. Little equipment infrastructure is involved when compared with other methods, such as metalorganic chemical vapor deposition or molecular beam epitaxy.

LPE is a method for epitaxially growing semiconductor layers from a metal solution. The metal solvent has a much lower melting point than the semiconductor. When the metal and semiconductor are combined, the semiconductor dissolves into the metal at a much lower temperature than would be required if the semiconductor was to be melted alone. This is the key interaction that allows LPE to provide high-quality growths at temperatures well below what would otherwise be required. The metal solvent and semiconductor solute are the basic components of the LPE melt. Depending on the system - which semiconductors are being grown, and which are being grown upon - other solutes for substrate wetting, oxide removal, and layer doping are also added to the melt.

Other components of the LPE system include a furnace, graphite boat, and source and seed wafers. The furnace is the controlled heating element for the process, while the graphite boat holds the melt and wafers and allows for movement of the wafers for precise growth control. The source and seed wafers are substrates that are used to either provide semiconductor material to the melt, in the case of the former, or provide the substrate upon which the layers will be grown, in the case of the latter.

At the setup of the LPE run, the melt components are placed in a well of the graphite boat and covered by a wellcap. Then the substrates are placed in the divot

of a slidebar positioned in the vertical center of the graphite boat. It is this slidebar that allows for substrate contact with the melt at specific times during the growth procudure. A visual representation of the graphite boat is shown in Figure 2.2.

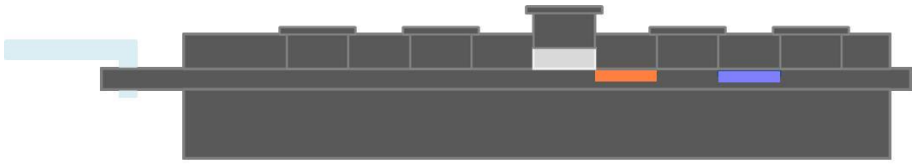


Figure 2.2: Cross-section of Graphite Boat with Melt, Source Wafer and Seed Wafer Depicted

As shown, the melt is silver, the orange is a source substrate, and the lilac is a seed substrate. The light blue device shown as connected to the slidebar is a quartz rod. This rod is manually pulled or pushed during the run to move the slidebar, which is seen to float between the upper and lower pieces of the boat. Once all of the growth components are placed within the graphite boat, the boat is placed in a quartz tube that runs through the center of a computer-controlled furnace. The system is sealed, run through a series of pumping and purging steps with alternating vaccuum and purified non-oxygenated gas to remove any contaminants, then set with a final flow of purified gas which will run for the duration of the growth process. The furnace controller is pre-set with a temperature versus time profile, and turned on. At specific points of time and temperature in the profile, the quartz rod is manually moved to bring the substrates in contact with the melt, or remove substrates from contact, in order to grow the layer.

LPE works based upon the principle of supersaturation, therefore, a standard LPE growth procedure will follow the same theoretical pattern. First, the temperature is raised to a point where the melt and all of its components are liquified. At this point, the temperature will either be lowered or kept constant, and once

the temperature stabilizes, the slidebar will be moved a precise amount in order to bring the source substrate into contact with the melt. The system will remain this way for a predetermined amount of time. During this period, the melt, which has a deficit of the source substrate material that is often the semiconductor to be grown, will etch away the substrate until the melt is saturated. It must be mentioned, however, that a source substrate is not always used. Another technique is to add the semiconductor material directly to the melt, in which case, the slidebar is not moved in the previous step because there is no substrate with which to make contact. At the end of the saturation period, the slidebar is again moved to remove the source substrate from contact with the melt, again, provided a source substrate has been used. The next step is to cool the system a precise amount so that the melt becomes supersaturated with the semiconductor to be grown. Any jolt to the system will cause nucleation and subsequent growth. This jolt occurs during the next step - the slidebar is again moved to bring the seed substrate into contact with the melt at the same time that the system begins to cool beyond the supersaturation point. This simultaneous presence of a site on which to nucleate and temperature at which the melt can no longer retain the amount of semiconductor dissolved in it is the driving force for the epitaxial growth occurring in an LPE system. The system cools to a set temperature at a specified rate to optimize the growth. The difference in temperature determines growth thickness, while the cooling rate determines growth quality. Once the final temperature is reached, the furnace is turned off and the slidebar is moved to remove the seed substrate from contact with the melt. The system is cooled, then, finally, unloaded. The generic temperature versus time profile described is shown in Figure 2.3.

All of this is merely the starting point for any growth through LPE. With each growth system comes different challenges, and to solve these challenges, the melt composition, substrates, and time and temperature profile must be adjusted

to suit the needs of the system.

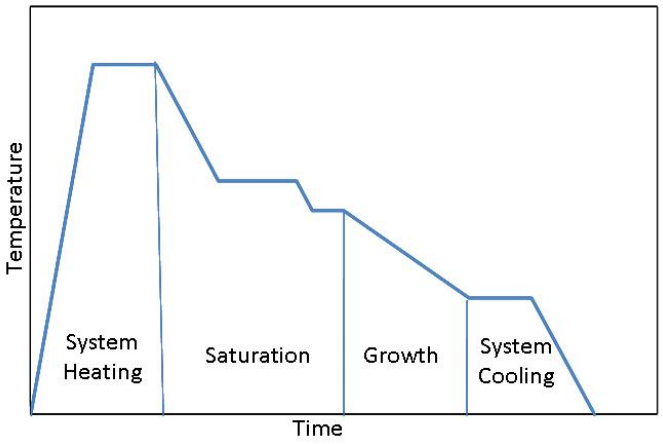


Figure 2.3: Generic Time and Temperature Profile for an LPE Growth

2.2.3 Foundational Work

In growth systems such as these, where many parameters are in play, it is often helpful to have foundational work from which to build. This work stems directly from a previous, vigorously analyzed growth technique for GaP on Si via LPE [7]. In this section, the details of the previous work will be expanded upon, as well as compared and contrasted to other published efforts where appropriate.

2.2.3.1 Substrate Orientation

There were two substrates used per growth in the foundational work - one source and one seed. The source substrates were Si, designed to saturate the melt with Si to prevent the melt from etching the seed substrate. These source substrates were n-type phosphorus doped with a resistivity of 3-8 Ω-cm (10^{15} cm^{-3}) [7]. Comparable experimental literature does not use source substrates in order to saturate the melt with Si. Instead of etching a source substrate, the Si was directly added to the melt [3]. In either case, however, it is important to note that all sources agree

on the point that Si must be a melt component [3, 7, 15]. If Si was not included in the melt, the saturability of Si in Sn would cause the melt to etch away the seed substrate rather than nucleate GaP and begin an epitaxial growth. The source substrate does not need a requisite orientation because orientation of the substrate lattice only comes into play for nucleation - not etching. For this reason, source substrate orientation is not discussed in the foundational work.

The seed substrate orientation can determine the success of nucleation and subsequent growth for epitaxial systems - especially heteroepitaxial layers with a lattice mismatch. In the foundational work the seed substrates were p-type boron doped Si (111) substrates [7]. The substrates were further oriented with a 4° miscut from the (111) plane versus a perfectly aligned sample. The Si had a resistivity of 3-6 Ω-cm, due to a doping concentration of 10^{15}cm^{-3}. There are several differences between growths on the miscut versus perfectly oriented substrates. These include a faster growth rate, higher dislocation density, and thicker layer under the same growth conditions for a GaP layer grown on the miscut Si substrate. This and other work also tested the quality of epitaxial growth on other substrate orientations, including (100) and (110), as well as for the (111) orientation [3, 7, 15]. Rotsztoczy and Stein do not mention a difference in growth quality between the (111) and (100) substrates that were used [15]. Beneking *et al.* show very distinct differences between the three substrate orientations tested: (100) yields rectangular structures, (110) elongated structures, and (111) yields a smooth, coherent surface [3]. The result from Beneking *et al.* is comprable to the foundational work for the (111) orientation, and both agree that this orientation yields the best growth results for this epitaxial process.

Based on the uses for source and seed substrates, the importance of orientation is not equal for the two. Source substrates do not need a specific orientation, as the orientation does not affect etching. The seed substrates, however, do require

a specific orientation for optimal epitaxial growth - in this case shown to be (111) according both the foundational work and other experimental literature.

2.2.3.2 Melt Composition

The melt composition for the foundational work consists of the solvent, wetting aid, oxide removal aid, and the semiconductor to be grown [7]. The solvent used is Sn, at an amount of 3.5 grams. The wetting aid is 350mg of Bi, and the oxide removal aid is 2-3mg of Mg. The GaP was added as a powder in the amount of 75mg. Si is not added to the melt directly in the foundational work because it is added using a source wafer. Other literature has fewer melt components - relying only on the direct addition of GaP and Si to the Sn solvent - and eliminates the use of a source substrate by adding Si directly to the melt [3, 15]. The foundational work is the only piece that has melt additives for wetting and oxide removal [7].

2.2.3.3 Time and Temperature Profile

The time and temperature profile of the foundational work consists of four distinct segments: melt homogenization, Si saturation, melt supersaturation, and growth [7]. The furnace ramps up to 910 °C and maintains that temperature for 1 hour. During this period, melt homogenization takes place - ensuring that all melt components are completely melted and evenly distributed throughout the melt. Then, the furnace cools down to 750 °C. Once the temperature stabilizes, the melt is brought into contact with the Si source wafer for 30 minutes. During this time, the melt, which is undersaturated with Si, will etch away the source wafer and introduce Si into the melt. After the 30 minutes, the Si source wafer is removed from contact with the melt, and the furnace cools to 748 °C. This 2 °C causes supersaturation of the melt. It has cooled the melt without causing nucleation and precipitation of semiconductor crystals from the melt. The supercooling is stabilized for 5 minutes,

at which point the Si seed substrate is brought into contact with the melt. This occurs simultaneously with a ramp down of 30 °C in 90 minutes - the growth rate.

Each piece of experimental literature has a very different approach from the others, despite operating under the same theoretical conditions. One approach using a Sn solvent was saturating at 850 °C, supersaturation at 845 °C, and cooling down to 650 °C in 3 hours for growth [15]. A second approach involves a combination of fast and slow growth rates: saturate the melt at 850 °C for 1 hour, bring the melt into contact with the seed substrate for 3 minutes, cool 10 °C in 1 minute for the fast growth, then cool 10 °C for 10 minutes for the slow growth [3]. This demonstrates the flexibility of the LPE system to produce good growth results from differing procedures, provided the theory behind the procedure is sound.

2.2.3.4 Wet Chemistry - Substrate Cleaning - Pump and Purge

This aspect of the experimental procedure is very important, as it describes substrate preparation and growth conditions. These conditions of the process are not described in comparable literature, but are found in the foundational work [7].

Substrate cleaning is pivotal for epitaxial growth on Si because of the nature of its native oxide. The oxide would prevent any epitaxial growth from occurring. For the foundational work, the cleaning procedure begins with a standard RCA1 clean ($1NH_4OH{:}1H_2O_2{:}5H_2O$) at 70 °C for 15 minutes to remove any organic contaminants. This is followed by a dip in 5% HF solution until the surface of the Si is hydrophobic. Then, an RCA2 clean ($1HCl{:}1H_2O_2{:}6H_2O$) at 70 °C for 10 minutes is performed to remove ionic contaminants. This clean is, again, followed by a dip in 5% HF solution until the surface is hydrophobic. The substrate is immediately dried with N_2, then transferred to the graphite boat for loading into the furnace. This will minimize interference from foreign contaminants directly on the surface of the substrates, as well as from the native oxide.

Once the boat is loaded into the furnace, the system is sealed. There are contaminants within the system, however, because the system was open to the atmosphere in the clean room in order to load the graphite boat. A series of pumping and purging steps is performed in order to remove any atmospheric contaminants from the system. The first step is to pump the system down to 50mTorr. At this point, the vacuum pump is closed off from the system, and the system is backfilled with Ar (99.999% purity). The system is pumped down again, then purged with Ar. This is repeated for a total of 3 pump-and-purge rotations. The final purge ends by switching over to H_2 (99.99998% purity), and setting the system to exhaust through a bubbler. This process, completed by a purified H_2 environment for the duration of the growth procedure, allows for maximum removal of foreign atmospheric contaminants.

2.2.3.5 Results

Each piece of experimental literature had different results for epitaxial growth of GaP on Si. In the case of Rosztoczy and Stein, the result was 10μm thick layers similar in quality to melt-grown GaP, and no distinction was made between results on Si(111) and Si(100) [15]. In contrast, Beneking *et al.* specifically stated that all successful growths that were analyzed had Si(111) substrates. The layers were smooth and uniform, of thicknesses between 7 and 10μm, and degenerately doped with both Si and Sn to be n-type [3].

In the foundational work, the results were epitaxial layers of 200nm thick for perfectly aligned Si(111) and 800nm-1μm thick for layers on 4° miscut substrates [7]. These layers were also degeneratively doped with both Sn and Si, and had dislocation densities of 10^8 cm^{-2} and 5x10^8 cm^{-2}, respectively. Additional analysis showed that the Si concentration in the layers was 15-20%, a much higher percentage than is allowable for Si to only be acting as a dopant in the layers.

These results show promise for lower-temperature growth regimes for successful epitaxial GaP growth on Si. The degenerative doping of Si and Sn, however, does not bode well for the use of the layer in a device - the doping would severely affect device performance. A device-quality layer would require subsequent growth layers from a melt that neither uses Sn for the solvent nor includes Si. In order to grow on the first epitaxial layer from another metal solvent, the amount of Si in the layer must be reduced. It is at this point - with these challenges - that this work begins.

Chapter 3

EXPERIMENTAL GROWTH OF GALLIUM PHOSPHIDE ON SILICON

The ultimate goal of this work is to aid in developing the technological capability to grow a monolithic III-V photovoltaic device on Si by LPE, utilizing the GaP layer developed in the foundational work. This work began with attempts to grow a first device layer - or second growth layer - on top of the epitaxial GaP layer already developed. After facing challenges with these attempts, this work turned toward the improvement of the foundational epitaxial layer in order to overcome the second growth layer challenges. These improvements occurred at three levels of understanding through experimentation. The first level experimentation explores the most fundamental issues for epitaxial growth in LPE: substrate orientation, run time reduction, phase diagram analysis, growth rate, and growth area. The second level experimentation is a higher level of understanding of the LPE growth process that builds upon what was learned on the first level through the development of the concept of a competitive growth regime. The third level builds further, discussing issues of growth thickness and deeper-level substrate challenges. These levels of experimentation will provide the foundation for theoretical device design, and the basis for even further growth improvement in future work.

3.1 First GaP Device Layer - Second Growth Layer

Due to knowledge of the successful growth of GaP from Sn, the first attempt to grow a second epitaxial layer began with using Sn as the solvent. It was believed

that this approach would eliminate detrimental material interactions that would potentially occur upon switching to a different metal solvent. Once it became clear that this approach was not likely to have success, the switch to using Ga as the solvent was made, owing in large part to the understanding of successful growth of GaP from Ga via LPE. This approach - while necessary to grow further layers - is shown to be incompatible with the epitaxial layer developed in the foundational work.

3.1.1 GaP from Sn

First attempts to grow a second layer of GaP from Sn began with an already grown GaP layer according to the procedure of the foundational work. Both the melt and time and temperature profile were changed for the second layer, and adjustments to these parameters became the focus for this portion of the work.

The components of the melt for GaP growth on Si include Sn as the solvent, Bi for wetting of the Si substrate, Mg for reduction of SiO_2 formation, and GaP as the semiconductor for growth. The melt was also saturated with Si to prevent etching of the seed substrate. For growth on another layer of GaP, all melt components designed to aid with growth on Si were no longer necessary. For this reason, the melt included only Sn, and a GaP source wafer replaced the Si source wafer. These changes to the melt and source wafers would be used for all attempts to grow a second layer of GaP from Sn.

The first time and temperature profile adjustment involved only the addition of a higher temperature at which to saturate the Sn with GaP. The homogenization occurred first at 910 °C, followed by a cool down to 800 °C. At this temperature, the GaP source wafer was brought into contact with the melt for saturation. The system then cooled to 750 °C, and continued along the exact same profile as the first layer growth. The results were unsuccessful. The buffer layer was completely etched away, leaving a clean Si substrate behind. Several growth attempts were made by

changing the portion of the time and temperature profiles that occurred prior to the actual growth step - none attempted to change the supersaturation temperatures or any part following. All of the results were etching of the GaP buffer layer to leave a clean Si substrate.

At this point, the realization was made that, as long as the same temperatures were being used to grow the second layer as were used for the first layer, the melt would reabsorb the GaP due to the solubility of GaP in Sn at specified temperatures. The next step, therefore, was to attempt the second layer of growth from lower temperatures than were used for the first layer.

For the new approach, the first layer was grown at a temperature 30 °C higher than previous attempts, beginning the growth step at 780 °C and cooling down to 750 °C. The second layer was then grown using the temperature difference from 748 °C to 718 °C. The resulting growth was a success in two ways: the first GaP layer was not etched away and a second layer of GaP was grown. This second layer had a 4.79% concentration of Si, was bright orange - a clear indicator of GaP growth - and had very poor coverage at only about $\frac{1}{20}$ the surface area of the substrate. Severe cracking was also evident, most likely caused by the difference in coefficient of thermal expansion, as shown in Figure 3.1.

One other attempt at second layer device growth was also made, with similar results. At this point, an analysis of the feasibility of continuing with this growth method was made. There are severe issues with wetting of the surface, and a remaining presence of Si in the layer, despite no Si being purposefully included in the melt. In addition, Sn solvents are well known to dope GaP layers on the order of 10^{19}cm^{-3}, much too high a doping concentration for acceptable device function, or for implementation of compensation doping. All of these aspects do not bode well for the successful use of GaP grown from Sn for the device layers.

The decision, therefore, was to move from the use of Sn as the metal solvent to

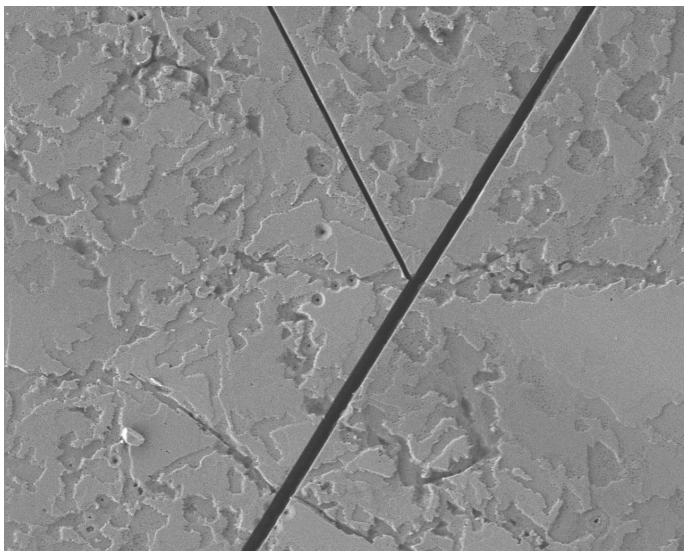


Figure 3.1: Second Layer GaP Growth

the use of Ga. While this metal solvent is known to produce excellent device-quality GaP epitaxial layers, its use presents significant challenges.

3.1.2 GaP from Ga

The most important challenge with using Ga as the metal solvent is the high solubility of Si in Ga. The degree of severity of this challenge became very evident when testing first began.

Initially, a sample with approximately 90% surface coverage of epitaxial GaP was processed according to the well-developed growth methodology for GaP on GaP from a Ga melt developed by Lu [12]. The result was complete destruction of the sample, as the Ga left behind only one small remnant of the Si substrate. It became immediately clear that a protective layer must be deposited to protect the Si from being completely absorbed by the Ga melt. The protective layer would have to guarantee coverage of the Si substrate on any and all areas where GaP had not grown.

Previous work for GaP on Si utilized selective growth approaches [7]. The Si substrate had a 500nm thick deposition of Si_3N_4 into which windows were etched, revealing limited areas of the Si. The epitaxial GaP layer would then be grown according to the same parameters, but the Si_3N_4 would prohibit growth outside of the window areas. The next test was performed using an epitaxial GaP layer grown on a selective substrate according to this procedure, using the same parameters for growth from Ga as the first test.

The result produced substrate etching. The etching pattern was different, however, as the entire substrate was not destroyed. Instead, interestingly, only the selective growth areas were completely etched through, poking holes completely through the substrate. This indicates, very clearly, that Si_3N_4 is an excellent protective layer for the Si substrate. The issue, then, is the epitaxial GaP layer's ability to withstand the Ga melt.

The belief was that the epitaxial GaP layer could not withstand the Ga melt due to its high concentration of Si. In essence, the Ga sought out the Si distributed throughout the GaP layer, and etched it away, destroying the integrity of the layer. Eventually, the Ga would reach the Si substrate, and rapid etching within the boundaries of the selective areas would ensue. In order to test this theory, a brief experiment was designed.

The test utilized two Si substrates with epitaxial GaP layers of differing Si concentrations. They were set on a hotplate and had one drop of pure Ga placed in the center of the epitaxial growth site for a 10 minute duration. This was an attempt to first test the resilience of layers with varying Si concentrations at much lower temperatures than would be experienced in the furnace. If the GaP layer could not withstand this test, it would not be able to withstand the furnace, either.

The first sample had a Si concentration of 50% in the GaP layer. The result of the hotplate test was complete etching of the GaP layer, and initial etching of

the Si substrate. In contrast, the second sample, with a 20% Si concentration, did not show any etching. These results indicated that lower Si concentrations in the GaP layer were required to withstand the Ga melt, but the question remained as to how low the concentration had to be.

The 20% Si sample was retested within the furnace under a saturated Ga melt, but was etched, providing the first boundary condition for acceptable Si concentration within the first GaP layer - less than 20%.

Selectively grown samples with Si concentrations as low as 6-9% in areas of the layer were then tested. This sample was tested in the furnace at full growth temperature, under a saturated Ga melt, for 10 minutes. The result was, again, etching within the windows. There was a difference, however, that supports the theory that Ga finds the deposits of Si in the epitaxial layer and etches those to weaken the layer. Not all of the original epitaxial layer was etched - the areas of the layer that remained were those with the lowest Si concentration and were farthest away from bulk growth areas with more Si deposits. This result made it clear that the Ga was attacking areas of highest Si concentration and causing the rest of the layer to etch around those areas.

In order for the growth of a second GaP layer from Ga to be successful, the Si concentration in the GaP epitaxial layer must be significantly, and uniformly, decreased from the original 20% value.

3.2 First Level Experimentation

The remainder of this body of work was designed to build off of - and improve upon - the results of detailed foundational work. With this being the case, the first steps were to return to first level concepts for epitaxial growth through LPE. These concepts are substrate orientation, reduction of run time, phase diagram analysis, growth rate optimization, and growth area adjustment. Once these more basic

concepts have been optimized, other levels of experimentation can be built upon these parameters to further improve the growth procedure.

It should be noted again that the starting point of this portion of the work is the end of the foundational work described in Section 2.2.3. This includes beginning with the same substrate (in our case, we worked with the same batch of p-type Si(111) with a 4 ° miscut, unless otherwise noted), melt composition, time and temperature profile, wet chemistry, and experimental setup, then working from this initial growth procedure to improve the resulting epitaxial growth layers. The systematic improvement to the growth process is expounded in the remainder of this chapter.

3.2.1 Substrate Orientation

The first step for this work was to analyze the choice of substrate orientation. Experimental literature was conflicting as to the results for growth on Si(111) versus Si(100), with some sources indicating poorer growth on Si(100) and other sources neglecting to comment on any differences between growth on the two substrate orientations [3, 7, 15]. The sources that indicated poor growth on Si(100) did not grow on these substrates from the finalized successful growth procedures, but at intermediate steps, therefore, it was determined that revisiting Si(100) would be of interest to this work [3, 7].

The comparison between Si(111) and Si(100) substrate orientations began with the selection of appropriate wafers for the Si(100). The chosen substrates were 2-inch, single-side polished, p-type boron doped wafers with a thickness of 256-306 μm and a resistivity of 5-10 Ω-cm (2x10^{15} cm^{-3}). Once the appropriate wafers were selected, they were diced and prepared according protocols for the Si(111) substrates.

The first growth on a Si(100) substrate ran according to the same parameters as the best results for Si(111) according to the foundational work. This would

provide a direct comparison between the results on the two substrates, as well as provide information as to the next step in developing the growth process on Si(100).

The first results showed islands of GaP growth, as well as 'poc-marks'. The islands of growth were separated by SiO_2. An SEM image of the growth layer is shown in Figure 3.2, in which the GaP growth is smooth and the SiO_2 growth is rough.

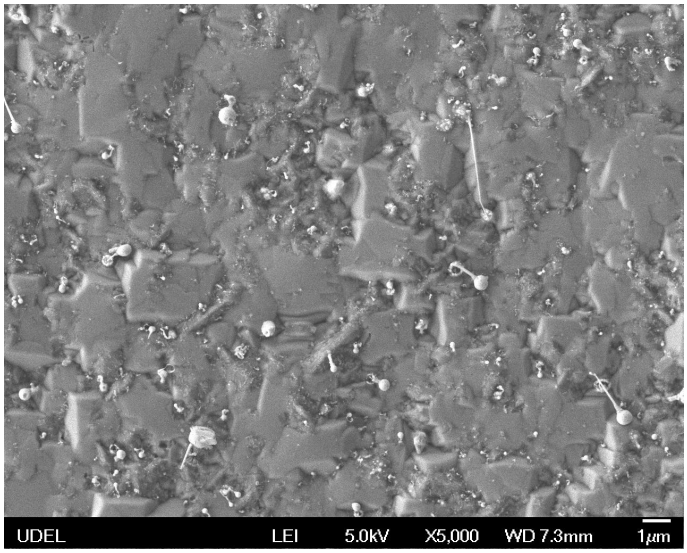


Figure 3.2: SEM Image of First GaP Growth on Si(100) - 0.1% Mg in melt

The islands of growth are rectangular at the base, and bear a strong resemblance to the results seen by Beneking *et al.* [3]. The layer has coalesced in some areas, but it was unclear as to the time at which the SiO_2 grew between the islands of growth. The first option is that, because the growth of GaP laterally across the surface is too slow, the SiO_2 had time to grow on the substrate and block further island coalescence. The second option is that the SiO_2 grew after the GaP growth had already been completed. Oxide removal was not an issue for growth on the Si(111) substrates, therefore, it is unlikely that incomplete initial oxide removal was

the cause of the SiO_2 in this case. In order to test the interaction of SiO_2 within the growth process, further experimentation was designed.

Within the melt, Mg acts as an oxide removal agent, binding with free O_2 in the system to form MgO, and preventing the binding of Si with O_2 and subsequent growth of SiO_2 on the surface of the substrate. If the lateral growth of GaP is too slow to overtake the regrowth of the native oxide, then raising the capacity of the melt to prevent SiO_2 growth might increase the time available for GaP growth to occur. This would result in increased coalescence of the GaP in the growth layer. As Mg is the oxide removal agent, systematically increasing the amount of Mg in the melt will raise the SiO_2 prevention capacity of the system.

Within the framework of the foundation work melt composition, Mg accounts for 0.1% of the melt. The next experiment was to raise Mg levels to 0.5% of the melt - 15mg. All other melt components, and experimental procedures, were kept the same. The resulting growth was pyramidal islands of Si, as shown in Figure 3.3.

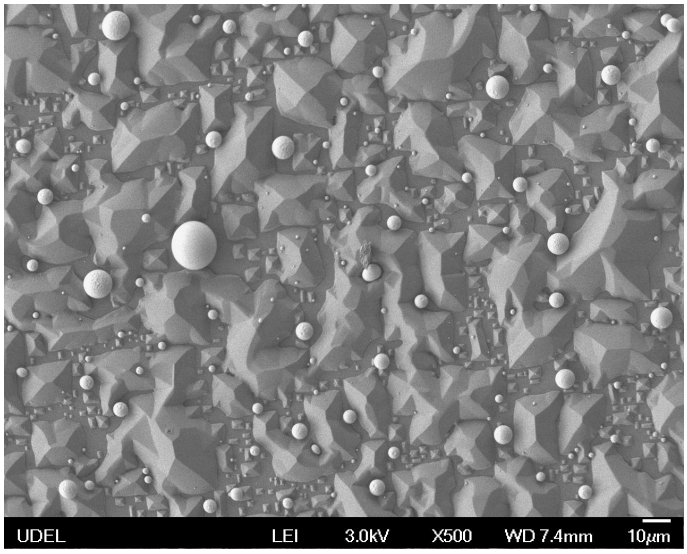


Figure 3.3: SEM Image of Si Growth on Si(100) - 0.5% Mg in melt

The only change between the two growths was an increase in the level of Mg

in the melt. As such, this must be the variable that caused the complete shift from GaP growth to Si growth, as well as leaving no trace of SiO_2 on the surface of the substrate. The Mg, therefore, not only acted to remove all of the SiO_2 as was its purpose, but is also believed to have bound the GaP thereby preventing its growth, as well. As this was clearly too much Mg to aid the growth of GaP, the amount of Mg in the melt was reduced for the next stage of the experiment.

The amount of Mg in the melt was split between the 0.1% and 0.5% of the first two experiments to 0.19%, or 7.5mg. The result was an improvement on both previous growth runs. The growth displays more densely packed GaP pyramids, as well as some GaP overgrowths around the SiO_2, as shown in Figure 3.4.

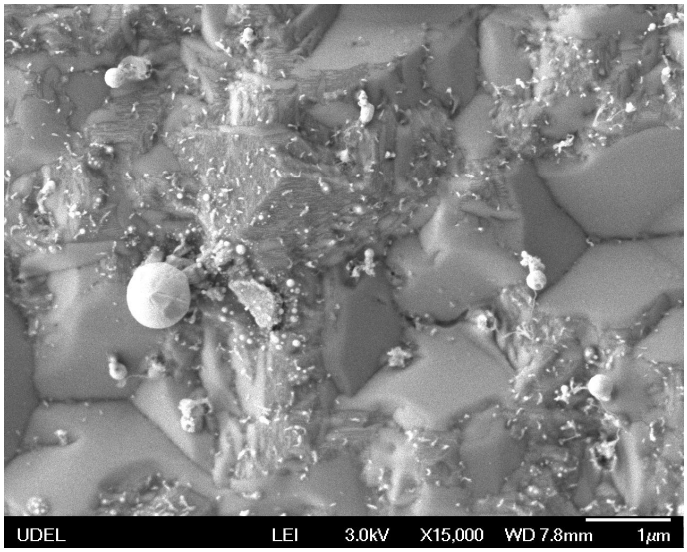


Figure 3.4: SEM Image of GaP Growth on Si(100) - 0.19% Mg in melt

This result supports the first theory - that the SiO_2 is regrowing during the slow lateral GaP growth, preventing the GaP islands from coalescing. The increased level of Mg in the melt from the original amount removed more O_2 from the system, buying more time for the GaP islands to grow and coalesce before interference from the SiO_2 blocked further coalescence.

The last result was the highest amount of Mg in the melt that successfully grew GaP, and showed that increasing the Mg in the melt could, in fact, increase pyramid coalescence. The next steps were attempts to determine the highest amount of Mg that could be used without converting the system to growth of Si. This was done by using amounts of Mg approximately halfway between the successful GaP growth Mg amount and the closest higher amount that produced Si growth. The growth attempts were performed with 0.375% (14.7mg) and 0.24% (9.3mg) Mg, in that order. Both of these attempts resulted in a growth of Si. The full flowchart of Mg levels, and their resulting growths, is depicted in Figure 3.5.

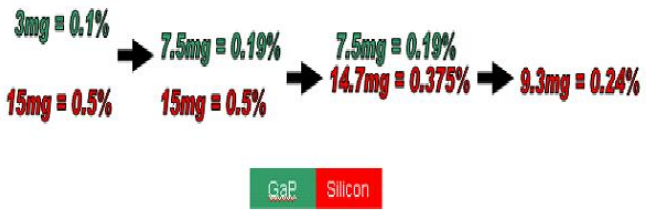


Figure 3.5: Flowchart of Testing on Si(100) with Varying Levels of Mg

At the end of this experimentation, it became clear that a level of Mg between 0.19% (7.5mg) and 0.24% (9.3mg) would be the maximum amount of Mg that the system could handle before reverting to growth of Si. It also was apparent that such a level of Mg would be highly temperamental, considering that the difference between the two amounts in the melt is 0.05%. It was unlikely that any further experimentation to narrow down appropriate levels of Mg would produce a fully coalescent GaP layer. This conclusion was reached based upon review of the level of coalescence of the 0.19% sample, and how much more coalescence would be required to produce a layer as uniform as that of the foundational work on Si(111). Given this

conclusion, it was determined that Si(111) is, in fact, the best substrate orientation to use when growing GaP on Si in an LPE system.

Remaining work, therefore, would be performed using Si(111) as the seed substrate for GaP growth on Si.

3.2.2 Run Time Reduction

The length of time required for one LPE run using the given time and temperature profile is approximately 6 hours, plus an additional hour for substrate cleaning and the pumping and purging of the furnace. Cooling down of the system requires further time that varies with environmental conditions. Rapid cooling, while convenient, is not the preferred method due to the difference in coefficients of thermal expansion. Additionally, Sn is baked out in the furnace to produce batches of small briquettes to be cleaned and used for the melt foundation - another 8 hour procedure. In order to decrease the amount of time required for one LPE run, and supplemental procedures, steps were taken to determine which portions of the growth process could be either shortened or eliminated without any detrimental effects on the results.

The first step was to determine which portions of the the growth process were able to be altered. The cleaning and pump and purge process prior to beginning the run cannot be shortened. Cleaning is a required step that is determined based upon a long history of Si technology, and so is most likely already optimized, while pumping and purging is reliant upon the efficiency of the vaccuum pump in the system on a given day. The only avenue for shortening this portion of the procedure is an increase in proficiency by the experimentalist, with a minimum timeframe of approximately one hour. The cooling down process, as already mentioned, is highly dependent upon the environmental conditions of the laboratory, and has some concerns regarding the difference in coefficients of thermal expansion of GaP and Si. The cooling process, therefore, is not a portion of the growth process that

is available for alteration. This leaves only the time and temperature profile of the growth run for potential alteration.

The sections of the growth run are the homogenization, Si saturation, supersaturation, and growth. The first step - homogenization - was determined to be the step that would be tested for necessity. The homogenization step was designed for the purpose of ensuring that all melt components were liquified and fully dispersed throughout the melt prior to interaction with any substrate. This step takes place at 910 °C for a period of one hour. In order to determine whether this step was necessary, the melting points of each individual melt component were found. The melting points are as follows: Sn, 231.9 °C; Bi, 271.4 °C; Mg, 650 °C; and GaP 1475 °C. The highest melting point is the GaP, which is well above the 910 °C homogenization temperature, but this is not an issue. The purpose of the LPE system is to provide an environment where a semiconductor will melt at temperatures much lower than its standalone melting point. The next highest melting point is the Mg, which melts at 650 °C - a temperature much lower than both the homogenization and Si saturation temperatures. It was determined, therefore, that the homogenization step is the best initial candidate for removal from the growth process.

The removal of the homogenization step eliminates 2 hours of time from the growth run, as the one hour time for homogenization and one hour cooling to the Si saturation temperature are eliminated, bringing the growth run time to 4 hours. This meets the goal for growth time reduction, but must be tested in order to ensure that the removal of homogenization will still produce GaP layers of acceptable quality.

The test of the run without homogenization began with a determination of the new time and temperature profile. The Si saturation temperature is 750 °C, which becomes the first step of the run profile. The furnace would then ramp up to 750 °C, remain at 750 °C for one hour 40 minutes to ensure enough time for even

melt component distribution and Si saturation, then finish with the previous profile for supersaturation and growth.

The growths without the homogenization step showed comparable results to those with the step. Later runs also reduced the time at 750 °C to one hour total, again with comparable results.

After the homogenization step was analyzed, the affect of a pre-baked Sn briquette versus loose Sn shot was analyzed. Several growths with plain Sn shot were performed, and the results were, once again, comparable to those with pre-baked Sn.

Based on these results, it was determined that both the homogenization and Sn pre-bake steps were unnecessary for good results, and were, therefore, eliminated from the growth process.

3.2.3 Gallium Phosphide Solubility Analysis - Growth Temperature Test

3.2.3.1 Gallium Phosphide Solubility Analysis

In order to continue to improve the growth procedure once unnecessary processes had been eliminated, an analysis of the solubility of GaP in Sn was undertaken. This began with a set of experiments designed to determine the precise amount of GaP dissolved into Sn at given temperatures.

The experimental setup involved Sn - to be used as a solvent - and one GaP wafer. A set of temperatures at which to test the GaP solubility was pre-determined. The experimental procedure began by weighing both the Sn and GaP wafer, then loading them into the graphite boat, and then the furnace. Pumping and purging of the system was performed in order to maintain equivalent environmental factors. The furnace was ramped up to the lowest temperature at which solubility would be tested. Once the temperature stabilized, the GaP wafer was brought into contact with the Sn and saturated for one hour. After saturation was complete, the GaP wafer was removed from contact with the melt, and the system was cooled and

unloaded. The Sn melt and GaP wafer were re-weighed, and the change in mass was noted. It was this change in mass that was used to determine the amount of GaP that dissolved into the Sn.

This procedure was repeated using the same Sn melt and GaP wafer, but the furnace was ramped up to the next higher temperature in the set for saturation. The Sn and GaP were weighed again afterward, and the change in mass noted. Because the solution was saturated at a higher temperature, based on the principles of solubility, more GaP went into the solution at this higher temperature rather than GaP coming out of solution. The change in mass for the second run, then, was added to the change in mass for the previous run to calculate a total amount of GaP in the melt at the higher temperature. The goal was to repeat this process multiple times - once for each additional higher temperature to be tested.

Prior to continuing the tests, we decided to evaluate the amount of time required for full saturation, to see if less than one hour produced comparable results. This would save a significant amount of time when being compounded by the number of runs to be performed. The previous steps were repeated, therefore, using a new Sn sample and GaP wafer, a half hour saturation time, but the same exact temperatures. The ratio of GaP to Sn for the two saturation times were comparable, so subsequent runs were performed using this second set of samples using the half hour saturation time.

There were some runs where melt was left behind on the source wafer. For these instances, the GaP source wafer was weighed first with the remaining melt, and then the melt was removed using RCA2. The GaP wafer was re-weighed, and the difference in mass of the GaP wafer before and after excess melt removal was calculated to determine the mass of the melt left behind. The final mass of the GaP wafer was taken to be that of the wafer after melt removal, and the mass of the melt that had been removed was added to the mass of the main melt for the final

Table 3.1: Experimental Measurements from GaP in Sn Solubility Test

Temperature (°C)	Source Before (g)	Source After (g)	Melt Before (g)	Melt After (g)
580	0.3670	0.3562	3.4790	3.4852
600	0.3562	0.3525	3.4660	3.4668
620	0.3525	0.3495	3.4668	3.4702
640	0.3495	0.3451	3.4659	3.4682
680	0.3840	0.3670	3.4400	3.4510
700	0.3372	0.3162	3.5388	3.5580
725	0.3162	0.3026	3.5580	3.5622
750	0.3026	0.3033	3.5622	3.5667
775	0.3033	0.2948	3.5632	3.5762
800	0.2948	0.2856	3.5701	3.5768

measurement. This correction was made to the melt mass only for that particular run. The next run in the series used the actual mass of the melt - not the corrected mass.

The complete test results are shown in Tables 3.1 and 3.2.

As can be seen in the table, there was a steady increase in the mass of the melt, and a decrease in the mass of the GaP source wafer. The change in mass for the GaP wafer and the Sn melt are not equal for equal temperatures, however, leading to the need to determine which measurement is more reliable and should be used for further calculations. For the 750 °C run, the source wafer actually gained mass instead of losing it. The melt also gained mass during this run. It was determined, based on this data point, that the change in the mass of the melt was a more stable, reliable data point. For further calculations, then, the change in the mass of the melt was used to calculate the amount of GaP that had been dissolved.

Once it was determined that the change in the mass of the melt would be the data used to determine the amount of GaP that had dissolved into the Sn at each temperature, calculations were made to determine several relationships between the

Table 3.2: Changes in Source and Melt from GaP in Sn Solubility Test

Temperature (°C)	Change in Source (g)	Change in Melt (g)	Difference Between CiS and CiM
580	-0.0108	0.0062	0.0046
600	-0.0037	0.0008	0.0029
620	-0.0030	0.0034	0.0004
640	-0.0044	0.0023	0.0021
680	-0.0170	0.0110	0.0060
700	-0.0210	0.0192	0.0018
725	-0.0136	0.0042	0.0094
750	0.0007	0.0045	0.0038
775	-0.0085	0.013	0.0045
800	-0.0092	0.0067	0.0025

GaP and Sn. The first calculation was the ratio of grams of GaP per gram of Sn at each temperature. Then, using the density of GaP, the volume of GaP dissolved in the melt at each temperature was determined. This volume was then used to calculate the expected thickness of a growth layer over an entire substrate area (12mm x 24mm) if the melt was to be cooled to the point where no GaP would be remaining. The results of these calculations are numerically displayed in Table 3.3, and graphically in Figures 3.6 and 3.7.

3.2.3.2 Growth Temperature Test

As can be seen from the solubility analysis, GaP is absorbed into the Sn melt at temperatures much lower than currently being used for the growth procedure. It was believed that, if GaP could be grown on Si at a lower temperature, less Si would be saturating the Sn melt, thereby reducing the potential for high Si concentrations in the epitaxial GaP layer. Experimental growth runs were designed and undertaken in order to see if GaP could be sucessfully grown on Si at lower temperatures.

The first experiment was testing to see if GaP could be grown on GaP from

Table 3.3: Theoretical Calculations from Results of GaP in Sn Solubility Test

Temperature (°C)	Total GaP in Melt (g)	Ratio $\frac{gGaP}{gSn}$	Total Volume of GaP μm^3	Calculated Thickness (μm) by Growth Area
580	0.0062	0.0018	$1.5x10^9$	5.7
600	0.0070	0.0020	$1.69x10^9$	6.4
620	0.0104	0.0030	$2.51x10^9$	9.5
640	0.0127	0.0037	$3.07x10^9$	11.6
680	0.0110	0.0032	$2.66x10^9$	10.1
700	0.0192	0.0054	$4.64x10^9$	17.6
725	0.0234	0.0066	$5.65x10^9$	21.4
750	0.0279	0.0079	$6.74x10^9$	25.5
775	0.0409	0.0116	$9.88x10^9$	37.4
800	0.0476	0.0135	$1.15x10^{10}$	43.6

Sn at a lower temperature than the original 748 °C starting growth temperature. If GaP could be grown on itself at lower temperatures, then there was a chance that it could also be grown on Si. If the result was unsuccessful, however, the odds were that the lower temperature growth would also be unsuccessful for growth on Si. The setup used a GaP source wafer, a GaP seed wafer, and Sn melt. Saturation occurred at 680 °C, with a supersaturation of 2 °C, making the starting growth temperature 678 °C. The result was epitaxial GaP growth on the GaP substrate. As this first attempt for a homogeneous epitaxial growth was successful, the next experiments returned to using Si as the seed substrate.

There were two lower temperatures that were tested for growth. The first of these utilized a 580 °C saturation and 578 °C starting growth temperature. This run design was carried out twice, and it resulted in etching of the substrate in one run and no affect on the substrate in the second run. The test temperature was then raised to a 680 °C saturation and 675 °C starting growth temperature. This resulted in growth covering all surfaces of the substrate, but the growth layer was 100% Si.

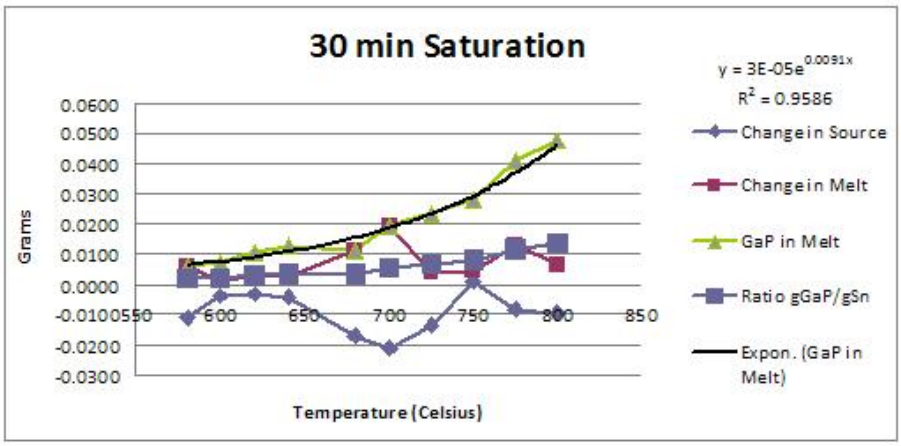


Figure 3.6: Graph of Experimental and Calculated GaP in Sn Solubility Relationships

These tests showed clearly that, while GaP may still be able to saturate the Sn at much lower temperatures than currently being used in the system, there is still a minimum temperature at which GaP will nucleate and grow on Si. The decision was made, therefore, to remain at the original growth temperature.

3.2.4 Growth Rate

The growth rate of the GaP layers to this point was a cooling of $\frac{1\,^{\circ}\mathrm{C}}{3min}$. Other sources indicated that faster growth rates, on the order of a minimum of $\frac{1\,^{\circ}\mathrm{C}}{min}$ produced better quality epitaxial layers, and that slower growth rates produced lower quality results [3]. As this distinction for growth rates is imperative for the optimization of the system, we determined that attempting growths at faster rates would be of interest. The results would provide two benefits if faster growth rates were successful: better quality epitaxial layers and shorter growth times.

The temperature difference for the system during the growth period was 30 °C, which leads to a total cooling time of one hour 30 minutes at the slow growth rate of $\frac{1\,^{\circ}\mathrm{C}}{3min}$. To test the effect of a faster growth rate, the rate was increased to $\frac{1\,^{\circ}\mathrm{C}}{min}$,

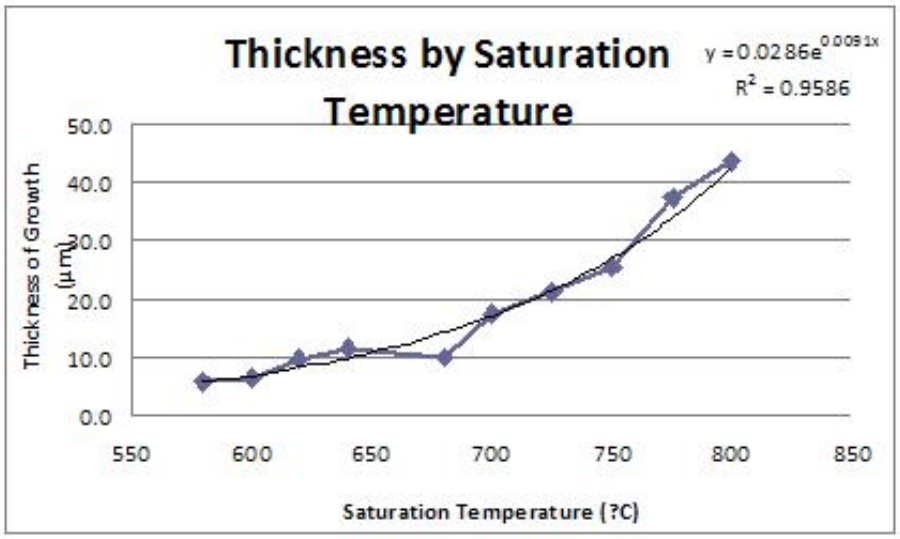


Figure 3.7: Graph of Calculated GaP Thicknesses at Each Temperature Based on Solubility Results

making a total growth time of 30 min. All other growth parameters determined to this point remained the same.

The resulting epitaxial growth was not GaP, but Si. The layer was not comparable in any way to the better GaP growth results found in literature for a minimum growth rate of $\frac{1\,^{\circ}\mathrm{C}}{min}$. It was determined, therefore, that this system requires a slower growth rate to allow for the kinetics of the system to foster GaP nucleation on the surface of the Si, thereby propagating GaP growth along the surface. Faster growth rates were not attempted.

The conclusion from these results was that the slow, $\frac{1\,^{\circ}\mathrm{C}}{3min}$ growth rate is the optimal parameter for this particular LPE growth system.

3.2.5 Growth Area

As discussed in Section 3.1.2, in order to grow GaP from Ga, there must be a protective layer keeping the Ga melt solvent from coming into contact with

the Si substrate. For our purposes, the protective layer is a standard silicon nitride (Si_3N_4) deposition. Windows through to the Si substrate were opened in the Si_3N_4 in order to provide clear growth areas that would be covered by epitaxial growth, eliminating any potential for exposed Si once the first GaP layer was grown.

The pattern of the windows included 6 - 1mm x 1mm squares, 4 - 3mm x 3mm squares, and 1 - 4mm x 10mm rectangle. This pattern is shown on a representative substrate in Figure 3.8.

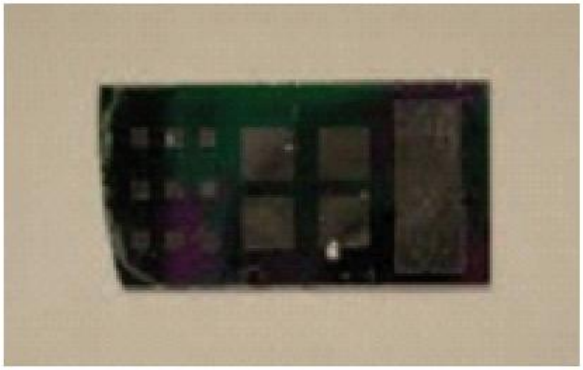


Figure 3.8: Representative Image of Windows in Si_3N_4 for Selective Growth

While analyzing growths on these selective areas, it became apparent that the size of the selective growth area affected the quality of the GaP layer contained within it. The repeatedly observed result was that the larger growth windows had more Si contained within the GaP layer than did the smaller windows, on the order of twice the atomic percentage. This was the case for all growth runs - the 1mm x 1mm windows had half the Si in the GaP epitaxial layer as the 4mm x 10mm windows on the same substrate. An example of the growth quality of a 4mm x 10mm window is depicted in Figure 3.9, which contains 9.51% Si over the total area.

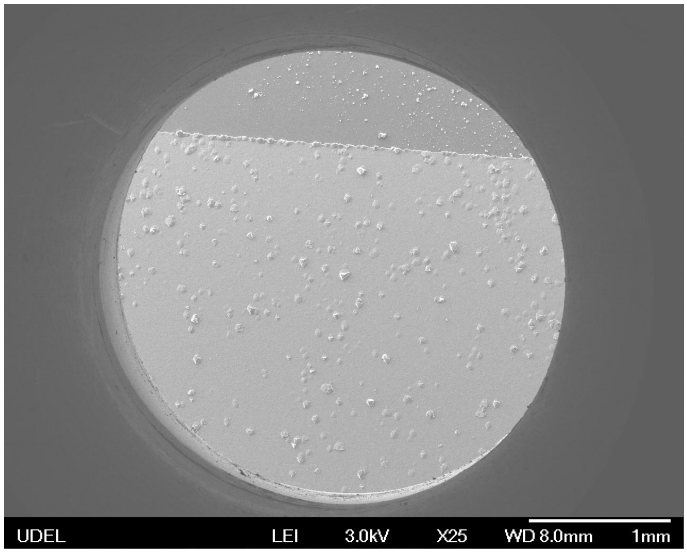


Figure 3.9: GaP Epitaxial Layer in 4mm x 10mm Growth Area Containing 9.51% Si

In contrast, the 1mm x 1mm windows on the substrate, depicted in Figure 3.10, had <5% Si.

The comparison of these two samples shows very distinct differences in growth composition and quality, as the large window sample does not show the same smooth, uniform characteristics as the small window sample. Upon further examination, it was determined that the peaks of growth in the large window sample were over 80% Si, while the smooth areas in between are <5% Si. The EDS images displaying a closer analysis of the pyramids spotting the surface of the large window and the space between are shown in Figures 3.11 and 3.12.

This is a very telling difference, as the growth conditions are exactly the same for all the windows, because they were from the same run. The only variable that has changed between the two samples is the size of the growth area. The repeatability of these results, coupled with only one variable change, allows for a highly credible analysis.

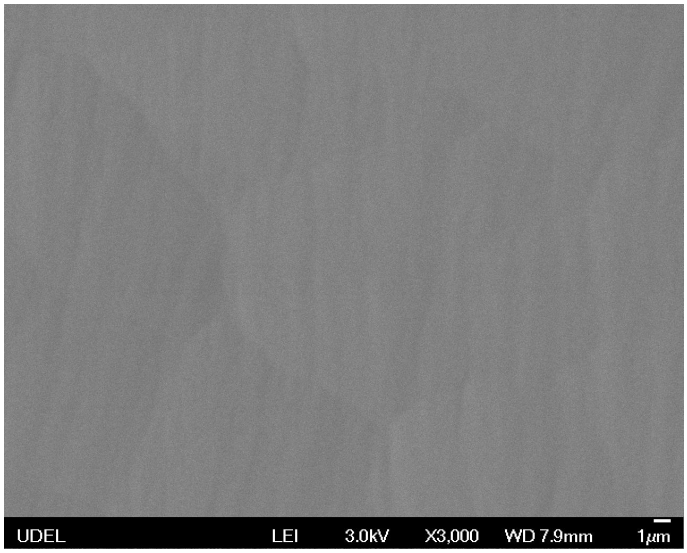
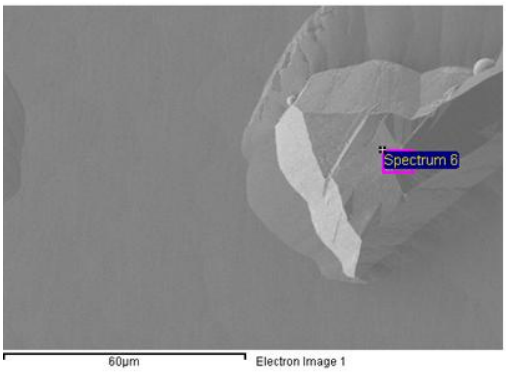


Figure 3.10: GaP Epitaxial Layer in 1mm x 1mm Growth Area Containing <5% Si

It is believed that the larger growth area takes greater time and material to fully cover the Si substrate with a GaP epitaxial layer than does the smaller growth area. It is highly probable that, because of this extra time and space requirement, the GaP does not cover the window area quickly enough to prevent higher amounts of Si from also nucleating on the substrate. The smaller growth areas are covered more quickly by GaP, reducing the amount of Si nucleation and deposition in the layer. As the goal is to reduce the amount of Si in the GaP layer as much as possible, having some areas with a large Si concentration on the substrate would only be detrimental to further epitaxial layer growth attempts.

Based on these highly repeatable results, and the subsequent analysis, it was determined that the best course of action is to eliminate the largest window, and grow epitaxial GaP using only the 1mm x 1mm and 3mm x 3mm windows.



Element	Weight %	Atomic %
Si	72.71	82.35
P	9.10	9.35
Ga	18.19	8.30
Totals	100	

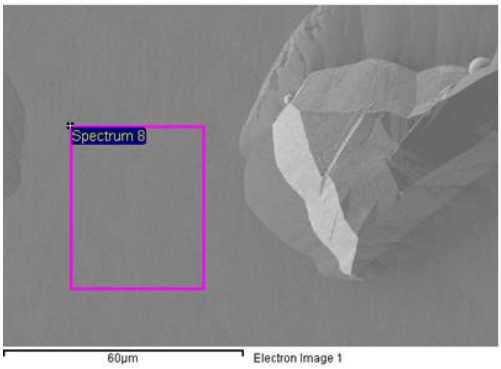
Figure 3.11: EDS of Pyramidal Structures Dotting the Growth in the Large Window Area

3.3 Second Level Experimentation

After basic growth parameters were set, the next steps were to improve upon the understanding of the interactions of components within the melt that may aid in reducing the concentration of Si in the epitaxial GaP layer.

3.3.1 Competitive Growth Regime - The Concept

One key to successful LPE growth is an understanding of the melt components, their interactions with each other, and their interactions with the substrates. The metal solvent is the first piece - the semiconductors being grown should be soluble in the chosen metal, but the seed substrate should be as insoluble as possible. Both semiconductors in the system - GaP and Si - are soluble in Sn. This requires that Si be added to melt along with the GaP growth material in order to prevent the Sn from etching the seed substrate. These two semiconductors are the next components. Other additives may be included for doping or substrate management. In our case, Bi was used to aid the Sn in wetting the Si substrate, and Mg was used



Element	Weight %	Atomic %
Si	2.50	4.27
P	33.32	51.59
Ga	64.17	44.14
Totals		

Figure 3.12: EDS of Smooth, Uniform Growth Between Pyramids in the Large Window Area

to reduce the formation of the native oxide. While the other components do have important roles, the key to this inventory is that there are two semiconductors in the melt.

This point is crucial for the LPE system, which functions using the theory of supersaturation. If a melt is saturated with two semiconductors and the system is cooled, both semiconductors will be supersaturated. If both semiconductors are supersaturated when contact is made with the seed substrate, then both will begin to nucleate and grow. The composition of the layer, then, becomes a competition between the two semiconductors as to which can nucleate first and fastest. This concept explains the results in previous sections where Si was grown instead of GaP for changes such as lower growth temperatures or faster growth rates. In those instances, it is likely that the change in temperature or growth rate gave Si an edge for nucleation and growth, whether through supersaturation differences or other mechanisms.

The concept of the competitive growth regime, then, is adjusting the system

parameters to ensure that the desired semiconductor has an edge over the other. The key is to pick a set of parameters that can be easily, and consistently, controlled. Obscure mechanisms, or those dependent upon other factors, would not be appropriate choices for this parameter set. For this work, the choice was a control of saturation through adjustments to the time and temperature profile.

There are three distinct system states that could be employed. The first is equal saturation of both semiconductors. When the system is cooled, both will be supersaturated and will begin to nucleate at the same time. This is undesirable for our purposes, as the GaP layer should have as little Si as possible. The second state is a higher saturation temperature for the desired semiconductor that, upon cooling for supersaturation, causes the desired semiconductor (GaP) to be supersaturated while the undesired semiconductor (Si) is only saturated. As the system cools for growth, the GaP will begin to nucleate first because it is supersaturated, while the melt must still cool enough for the Si to reach supersaturation before it, too, can begin to nucleate. This is a better system state for our purpose. The third system state utilizes and even higher saturation temperature for the GaP than the previous system state. As the system cools, supersaturation for the GaP will occur at a point where Si is undersaturated, rather than saturated. This will make the lag time even longer before the Si can begin to nucleate. This system is the most optimal, but must be handled with care. If the Si is too undersaturated, the melt will etch away the Si seed substrate - which was an effect that required Si to be added to the melt in the first place. There must be a balance struck between the supersaturation of the GaP and the undersaturation of the Si in order for the third system state to be successful.

3.3.2 Competitive Growth Regime - Tests

In all previous growth runs, the melt was saturated with GaP and Si at the same temperature, with most of those runs using 750 °C. For the test of the GaP

supersaturation/Si undersaturation theory, a new time and temperature profile was designed.

In the new time and temperature profile, the saturation of Si through contact with the source substrate occurred at 740 °C for 30 minutes. After the 30 minutes, the source substrate was removed from contact with the melt, and the system temperature was raised to 750 °C. This higher temperature would allow for more of the GaP powder to dissolve to saturate the melt. This step lasted for one hour. The supersaturation temperature was chosen to be 745 °C - a 5 °C difference from the GaP saturation temperature. Growth then began at 745 °C at a rate of $\frac{1\,^{\circ}\mathrm{C}}{3min}$ over a full temperature difference of 30 °C. This first growth attempt using the competitive growth concept produced a layer of 100% Si, as shown in Figure 3.13.

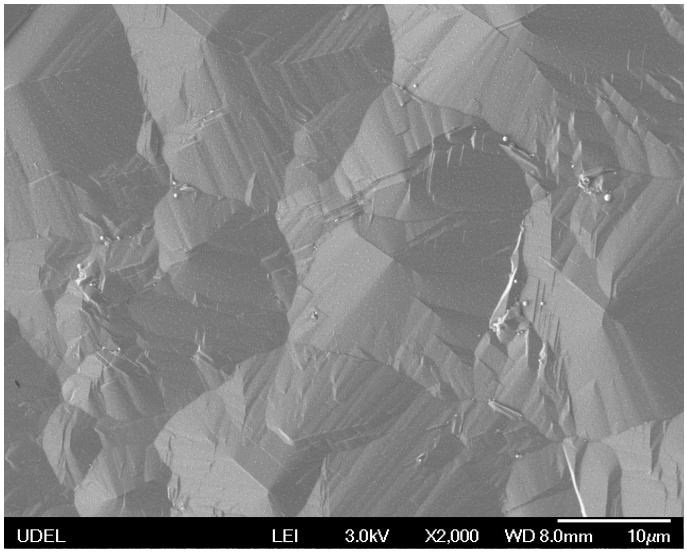


Figure 3.13: Epitaxial Si Layer - First Attempt for Competitive Growth

The substrate did not etch, which was a good result, but the fact that Si grew was counter to the goal of the experiment. After this result, it was determined that one parameter should be changed - the supersaturation temperature. In previous growth runs, including the foundational work, the supersaturation temperature

difference was only 2 °C, not 5 °C. The next growth used the exact same time and temperature profile as the first attempt, except that it changed the starting growth temperature to 748 °C. The resulting layer growth was a success. A uniform, 3.35μm thick epitaxial GaP layer with 6-10% Si concentration was grown. This was a significant reduction from the 20% Si concentration in the foundational work. Images of the GaP layer are shown in Figures 3.14 and 3.15.

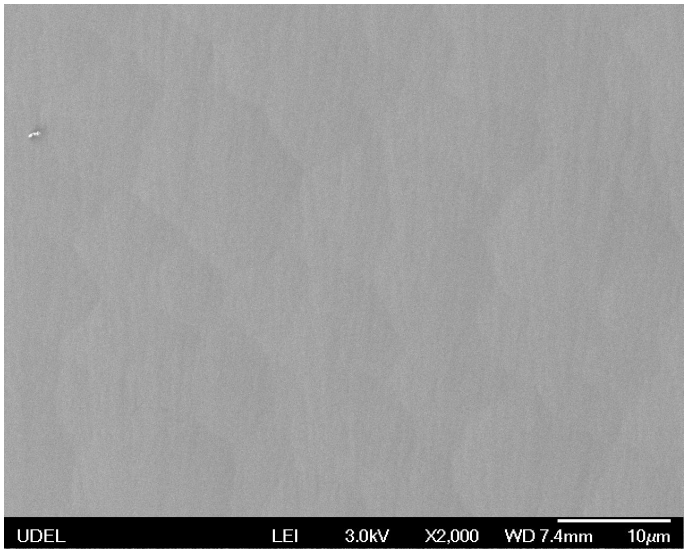


Figure 3.14: Epitaxial GaP Layer - Second Attempt for Competitive Growth - 6-10% Si

This result was tested for reproducibility using all the same parameters. It should be noted that, during this reproducibility run, a timing error was made which affected the Si saturation. The 30 minutes that the Si source substrate was in contact with the melt spanned the 740 °C, as intended, but also ran into the period where the system ramped up to 750 °C for the GaP saturation. This would have affected the saturation of the melt with Si, but did not result in a detriment to the growth. The result of this test was a uniform growth of GaP with even less

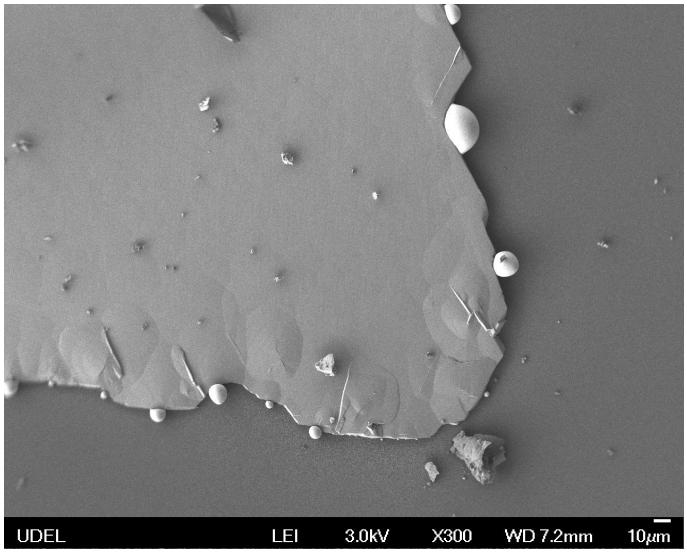


Figure 3.15: Epitaxial GaP Layer - Second Attempt for Competitive Growth - Corner of Selective Window Displaying Lateral Overgrowth

Si concentration - as low as 3-5% Si in small growth windows, up to 10% Si in large growth windows. An image of the growth is shown in Figure 3.16.

After these two successful results, the competitive growth process was repeated. Subsequent attempts using this exact growth method were unsuccessful, however, resulting in substrate etching.

Due to the occurrence of etching - signifying a detrimental amount of Si undersaturation, the GaP supersaturation temperature difference was also changed from 2 °C to 8 °C, changing the Si undersaturation from 8 °C to 2 °C. One of these attempts resulted in GaP growth with 15% Si concentration, which was revealed after removing melt that had remained behind completely covering the surface of the growth areas. Subsequent attempts were unsuccessful.

Another process was then adopted for testing - the step growth. For a step growth, instead of ramping down the temperature a certain number of degrees per minute to initiate growth, the system is held at one temperature for a period of

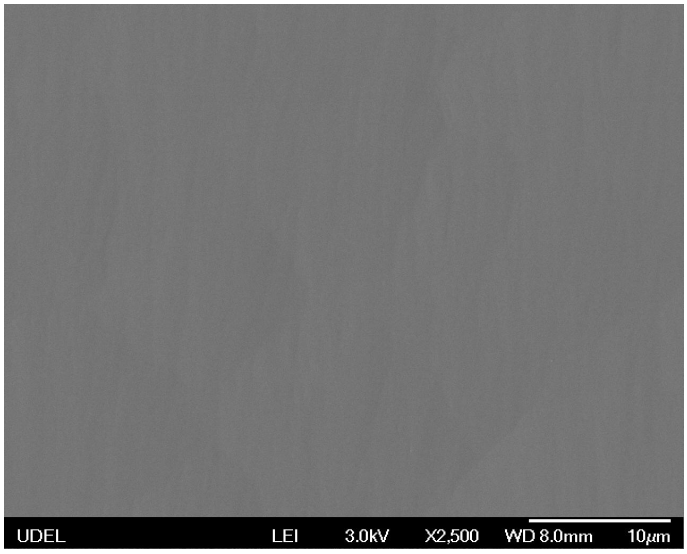


Figure 3.16: Epitaxial GaP Layer - Reproducibility of 6-10% Si - 3-10% Si Result

time while in contact with the seed substrate. The attempts of the melt to reach equilibrium cause nucleation on the substrate and subsequent growth. For this test, the Si was saturated at 740 °C, the GaP at 750 °C, and the step growth temperature was 740 °C - leaving the system at perfect Si saturation. The theory is that, if the melt is saturated with Si and remains at that temperature, the GaP will be the only semiconductor to nucleate because it is the only one that ever reaches a state of supersaturation. These attempts, again, were unsuccessful, resulting in either no affect on the seed substrate or substrate etching. It is believed that the lack of a growth rate eliminates key driving forces that cause any nucleation on the surface. While a slow growth rate is more beneficial for the growth of GaP on Si, no growth rate is worse.

After all of these experiments, it is clear that more work needs to be done in analyzing the competitive growth regime concept. The idea has been proven twice with very highly successful results. This indicates that the results should be able to be replicated. It is unclear at this point what the key factors are that ensure success

in some growth attempts and unsuccessful results in others. Further analysis is needed to solve this challenge, and will be addressed in future work.

3.4 Third Level Experimentation

The final stage of experimentation for this work was a refinement of the growth procedure and the understanding of the mechanisms at play. It was brought about by attempts to satisfy future device design constraints.

3.4.1 Substrate Orientation Refinement

When the epitaxial GaP layer is grown on Si, the phosphorus diffuses into the Si, doping it n-type. If the original Si substrate is p-type, this will form a diffused junction which will exhibit a photovoltaic effect. In order to grow and optimize a GaP solar cell grown on a Si substrate, the optimal starting point would be with only one diode, not two. The substrate used in the bulk of this body of work - and which produced all of the significant results - was p-type. In order to have only one diode created when growing the epitaxial GaP layer, an n-type substrate would be required.

Based upon the results of Section 3.2.1, it was determined that an n-type substrate with a (111) orientation would be used. The n-type wafers were ordered to have a (111) orientation without a miscut. It was believed, based upon the success of the foundational work with both perfectly aligned and 4° miscut substrates, that the miscut was not the first priority in finding appropriate substrates.

When these first, perfectly aligned substrates were used for growth attempts, the results were poor. Little to no growth occurred with the same growth procedures that performed well on the p-type, 4° miscut substrates. Many results also produced growth of Si. In addition to using previously successful growth procedures, new procedures were attempted in an effort to grow on the new substrates,

but without success. These unsuccessful attempts to use n-type, perfectly aligned (111) substrates led to the consideration of a different n-type substrate.

The next n-type substrate that was chosen had a 4 ° miscut off of the (111) axis - just like the successful p-type substrates. These substrates also did not perform successfully. Again, growth procedures that were successful on the p-type substrates were unsuccessful on the new n-type substrates. The results included very poor GaP growth, substrate etching, and Si growth from various run configurations. New attempted procedures - just as with the previous n-type substrates - were similarly unsuccessful.

At this point, there was a need to more closely compare the substrates being used.

The first step was to perform a growth procedure on both substrates that was known to work and have repeatability. For this purpose, we used the foundational work procedure - known to repeatably produce 20% Si in the GaP layer. The next step was to eliminate all variable differences between the growths on the two substrates, so that environmental changes or human error would not make the two runs different. The solution was to put samples of both substrates into the same divot for only one growth run - a half sample of each.

The experiment was performed with one half sample of the p-type, (111), 4 ° miscut substrate and one half sample of the n-type, (111), 4 ° miscut substrate. The results showed a clear difference between the two. Growth on the p-type substrate was uniform, smooth, and 20% Si, as expected. On the n-type substrate, however, there was no growth.

At this point, it was imperative that an exact difference between the substrates be determined. There were three distinct options: 1) both substrates are the advertised miscut, indicating that there is a fundamental difference in growth due to the doping of the substrate, 2) one of the substrates is not the miscut advertised,

or 3) both of the substrates are not the miscut advertised. For the first option, the indicator of a hindrance of growth based upon the dopant type is very profound and far-reaching - especially as pertains to this work. The second and third options are less severe, merely indicating that a difference in miscut is the source of growth issues.

In order to determine the exact orientation of the substrates, X-ray Diffraction (XRD) was performed on all three substrates: miscut p-type, perfectly aligned n-type, and miscut n-type.

The XRD results show a clear miscut of 4° for the p-type substrates. This is a first, good result, as it confirms that we did, in fact, perform the bulk of this body of work on the type of substrate we intended. The perfectly aligned n-type (111) substrate also displayed results matching the advertised cut orientation. This, again, is a good result, as it shows a distinct, quantifiable difference in substrate between the good results of the miscut p-type substrate and the perfectly aligned n-type substrate. The result for the final n-type sample is the most crucial, however. If the sample does, in fact, show a 4° miscut off of the (111) orientation, then the suggestion would be that the doping might be a fundamental parameter affecting growth. The resulting XRD data shows, however, that the miscut n-type samples are not, in fact, miscut. The sample is also perfectly aligned, within reasonable error. The XRD data is displayed in Figures 3.17, 3.18, and 3.19.

Based on these results, it has become clear that, in order for our particular system to produce high-quality, low-Si epitaxial GaP layers on Si, the required substrate orientation is more particular than the choice between (100) and (111). The substrates required for further development must have a 4° miscut off of the (111) plane.

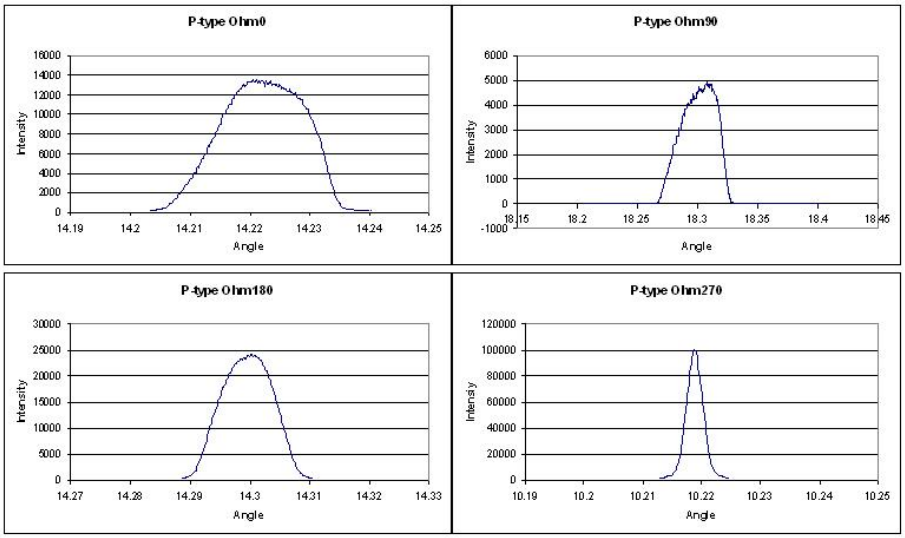


Figure 3.17: XRD Results for P-Type Si(111) with a 4° Miscut

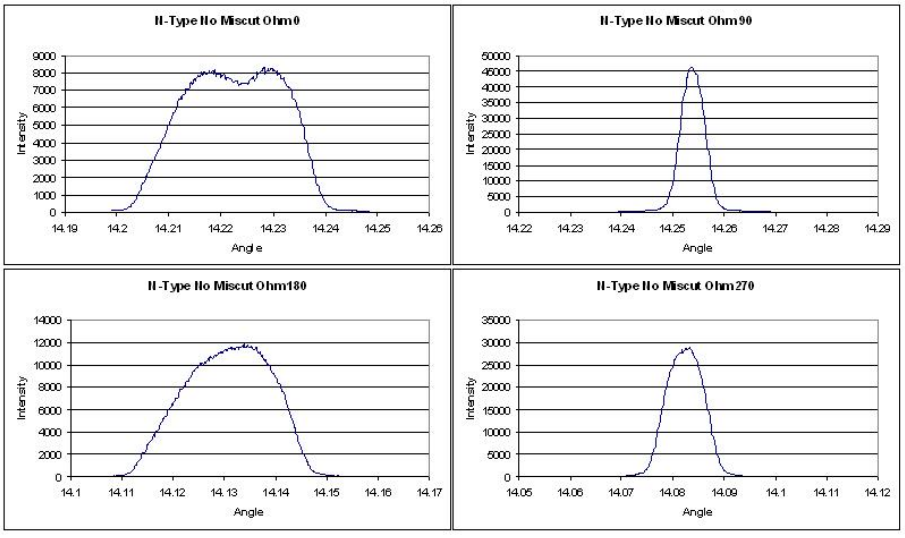


Figure 3.18: XRD Results for N-Type Si(111) with No Miscut

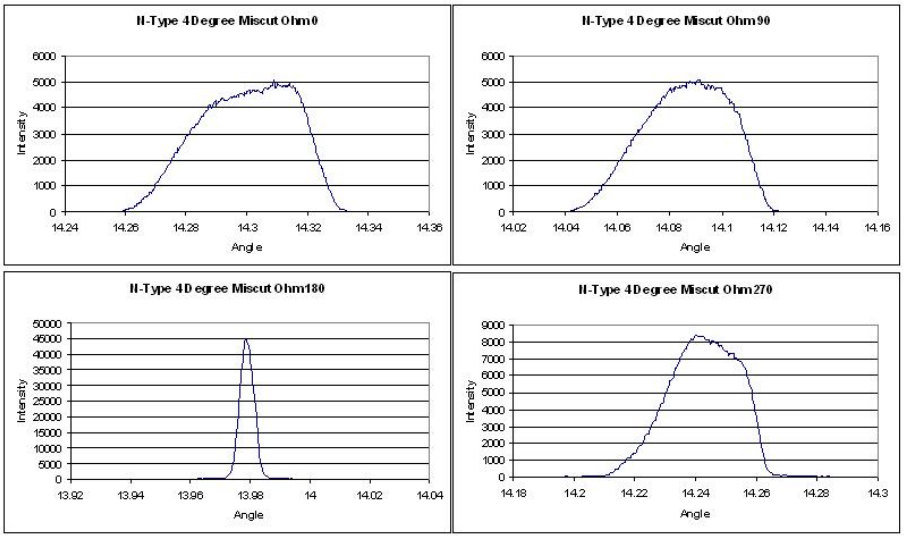


Figure 3.19: XRD Results for N-Type Si(111) with an Assumed 4° Miscut

Chapter 4

THEORETICAL DEVICE DESIGN

The ultimate intention of the previously described work is its use as a buffer layer for the growth of III-V devices on Si. As such, it is important to evaluate the theoretically obtainable performance of such devices, as well as their affect on the Si solar cell device upon which they would be grown. The details of this analysis are presented here for two candidate III-V solar cells: GaP and GaAsP.

4.1 Choice of Candidate Materials

The range of III-V materials from which to choose is important to the future of the device and this body of work. The reasons behind each choice begin with the requirements of epitaxial growth, and are followed by device performance requirements.

The first material choice was a natural progression from this work - GaP. The lattice mismatch between one epitaxially grown GaP layer and another should be nonexistent, guaranteeing a high quality device layer epitaxial growth. In addition, the high bandgap of GaP would more effectively convert the high energy photons, as well as maintaining a transparency for all photons that would be collected by the Si device. While not the optimal bandgap for the top junction in a dual junction device with Si, as discussed in Section 1.2.4, it will provide a test platform for further technological and device development.

The second material choice was based first upon the bandgap. As the optimal bandgap for the top junction in the dual junction cell is 1.81eV, the material should

be able to have a bandgap as close to this value as possible. Second, the material should have a lattice mismatch low enough to GaP to ensure adequate epitaxial growth upon the buffer layer. Two materials were chosen which fulfill these criteria: InGaP and GaAsP. In order to determine which of these two materials would be the better option, the lattice constant as related to bandgap was determined for both materials. At the required bandgap of 1.81eV, GaAsP has a lattice constant closer to that of GaP than InGaP, as shown in Figures 4.1 and 4.2. Based on this analysis, GaAsP was chosen as the material to be considered for the top junction.

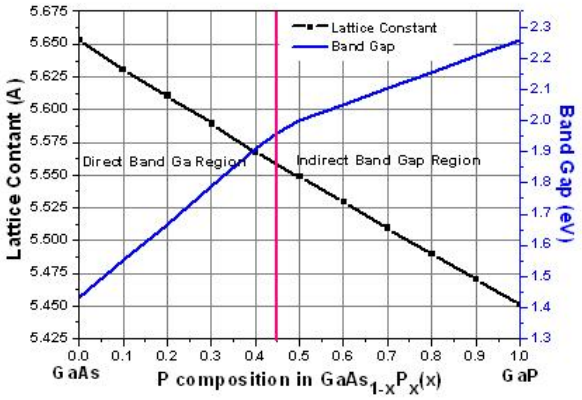


Figure 4.1: GaAsP Lattice Constant and Bandgap as a Function of P Composition

4.2 Multijunction Solar Cell Structure

Once the materials are chosen for the top junction in the device, it is necessary to design the structure. The potential device performance cannot be analyzed without a structure to which the theoretical analysis can be applied.

The substrate and bottom junction of the multijunction system will be made of Si. On top of this Si, a GaP buffer layer will be grown - stemming from the results of this work. The buffer layer should be as thin as possible to reduce complications

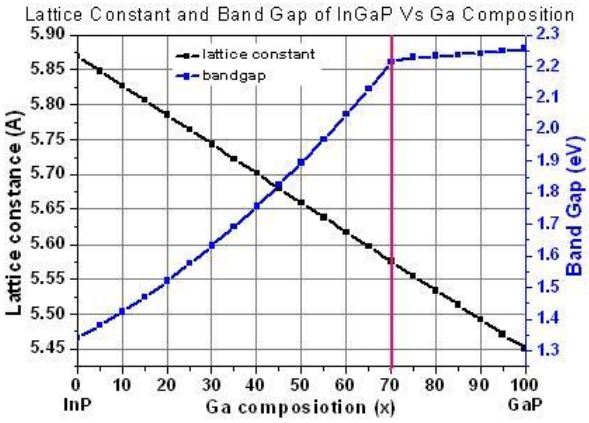


Figure 4.2: InGaP Lattice Constant and Bandgap as a Function of Ga Composition

during growth of monolithic layers. For this purpose, we have chosen to cap the buffer layer at 500 nm thick. The top junction will have a total thickness of 2 μm of either GaP or GaAsP. This 2 μm theoretical limit has been applied for both growth feasibility and cost concerns. The structure of the final device layers is shown in Figure 4.3.

4.3 Theoretical Methodology

The theoretical examination from first principles of the cells designed in this work is first performed on each individual material system as an individual cell. This results in a basic examination of the device parameters for a basic Si cell, a GaP cell, and a GaAsP cell, constrained to the parameters discussed in Section 4.2. These results are then combined to examine the resulting effects of placing a top junction above the Si cell. The steps for theoretical examination are as follows:

1) Determine the full range of absorption coefficient data for Si, GaP, and GaAsP.

2) Calculate Generation Rate at appropriate depths for each material.

Figure 4.3: Basic Layer Structure of Future Device

3) Calculate short-circuit current density (J_{sc}), dark saturation current density (J_0), and V_{oc} based upon material and device parameters.

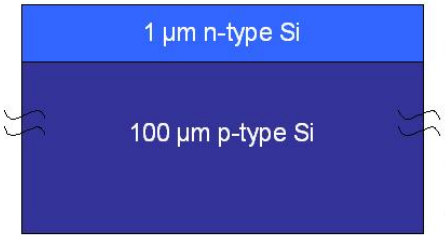
4) Determine the FF and efficiency (η) for the individual cells.

5) Using the material and device parameters from steps 1-4, re-analyze the Si solar cell considering how the addition of a top junction will affect the Si cell performance.

These steps are expanded upon in detail for each system in the following sections.

4.4 Representative Si Solar Cell

In order to determine the true value of adding either a GaP or GaAsP solar cell as the top junction in a dual junction solar cell with Si, the performance of a representative Si solar cell must first be determined. For this body of work, a Si solar cell with standard parameters was used, as shown in Figure 4.4. The analysis for the solar cell follows the methodology explained in Section 4.3, beginning with a determination of the absorption coefficient data.



Si Material Parameters				
P Region			N Region	
NA (cm^-3)	1.00E+17		ND (cm^-3)	1.00E+18
ni (cm^-3)	1.45E+10		ni (cm^-3)	1.45E+10
µn (cm^2/Vs)	1417		µp (cm^2/Vs)	471
Dn (cm^2/s)	36.64362		Dp (cm^2/s)	12.18006
τn (sec)	2.50E-05		τp (sec)	1.50E-06
Ln (cm)	0.030266987		Lp (cm)	0.004274

Figure 4.4: Si Bottom Cell Structure and Material Properties

Absorption coefficient data for Si was the first parameter determined in the analysis. Using digitized graphical data, curve fitting was used to define the absorption coefficients across the photonic spectrum. The absorption coefficient data for Si is shown in Figure 4.5.

Once the absorption coefficient data was determined, the generation rate at each wavelength for two thicknesses - thickness of the n-type emitter and of the entire cell - was calculated using the following equation:

$$G = \sum_{\lambda} N_0(1 - e^{\alpha x_L}) \cdot \Delta\lambda \tag{4.1}$$

where N_0 is the photon flux density, α is the absorption coefficient, x_L is the distance into the surface of the solar cell, and $\Delta\lambda$ is the difference between the specific wavelength being considered and the previous wavelength in the interval. By summing all G values for the full range of wavelengths, a total G can be calculated for each specified thickness of solar cell. The light generated current, J, can then be calculated for each depth using the equation:

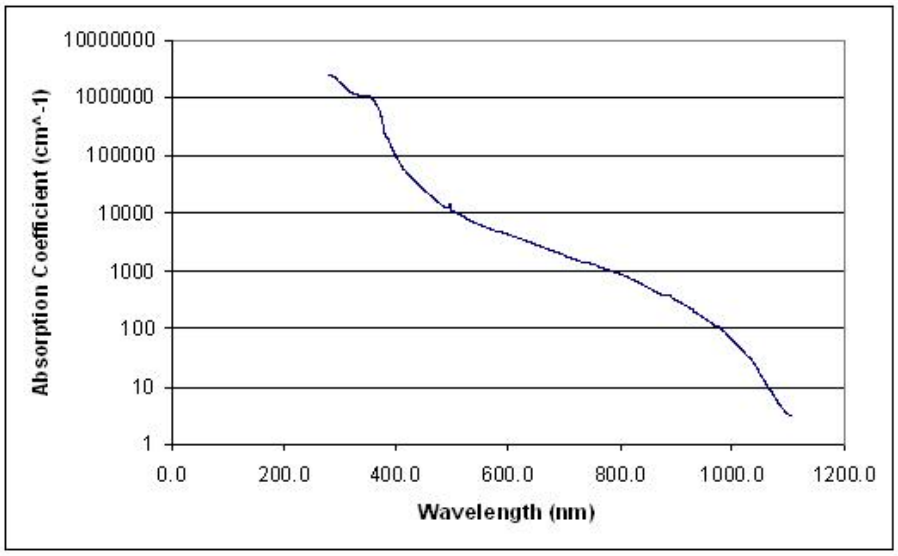


Figure 4.5: Si Absorption Coefficient Data

$$J = qG \tag{4.2}$$

where q is the elementary charge. Within the first thickness of the cell - the n-type emitter - the J_{sc} for a Si material thickness of 1 μm was calculated to be 12.13 $\frac{mA}{cm^2}$. The entire cell thickness - 101 μm - was calculated to have a J_{sc} of 38 $\frac{mA}{cm^2}$. This calculation, while a starting point, does not take into consideration differences in material properties between the emitter and base layers. In order to determine the J_{sc} taking these factors into account, the following equation is used:

$$J_{sc} = \sum [J_2 - J_1] e^{\frac{-(\frac{x_1+x_2}{2})}{L_{n/p}}} \tag{4.3}$$

where J_1 and J_2 are the calculated currents at each depth from Equation 4.2, x_1 and x_2 are the considered depths, and $L_{n/p}$ is the diffusion length in the base or emitter region, respectively. To determine the J_{sc} for emitter region, J_1 was taken to be zero and J_2 was taken to be 12.13 $\frac{mA}{cm^2}$. The other variables - x_1, x_2,

and L_p - were taken to be 0 μm, 1 μm, and 42.74 μm, respectively. The J_{sc} for the emitter was 12.06 $\frac{mA}{cm^2}$. The same technique was applied for the base region, analyzing current from the depth of 1 μm through 101 μm, and using the diffusion length for the minority carrier electrons. The resulting J_{sc} for the base region was 21.86 $\frac{mA}{cm^2}$. Combining the two results in a total cell J_{sc} of 33.92 $\frac{mA}{cm^2}$.

The J_0 and V_{oc} terms were calculated using the following equations:

$$J_0 = q(\frac{D_n n_i^2}{L_n N_A} + \frac{D_p n_i^2}{L_p N_D}) \tag{4.4}$$

$$V_{oc} = \frac{kT}{q} ln(\frac{J_{sc}}{J_0} + 1) \tag{4.5}$$

where $D_{n/p}$ is the diffusivity in the base or emitter, respectively, n_i^2 is the intrinsic carrier concentration, $N_{A/D}$ is the dopant concentration in the base or emitter, respectively, and k is Boltzmann's constant. The Si solar cell had a calculated J_0 of 5.04x10^{-10} and a V_{oc} of 645 mV.

The the diode and FF equations were then used to plot a JV curve and determine the FF, respectively:

$$J = J_0(e^{\frac{qV}{kT}} - 1) - J_{sc} \tag{4.6}$$

$$FF = \frac{V_{MP} J_{MP}}{V_{oc} J_{sc}} \tag{4.7}$$

where V_{MP} and J_{MP} are the voltage and current density, respectively, at the maximum power point.

The efficiency was the final parameter to be calculated, using Equation 1.1. The final calculated parameters showed a Si solar cell with a FF of 83.62% and a 18.29% efficiency. A summary of device performance is shown in Table 4.1, while the calculated JV curve is shown in Figure 4.6.

Table 4.1: Theoretical Device Results for a Respresentative Si Solar Cell

Parameter	Calculated Result
$J_0(\frac{mA}{cm^2})$	5.04x10^{-10}
$J_{sc}(\frac{mA}{cm^2})$	33.92
V_{oc} (mV)	645
$P_{max}(mW)$	18.3
FF	83.62%
η	18.29%

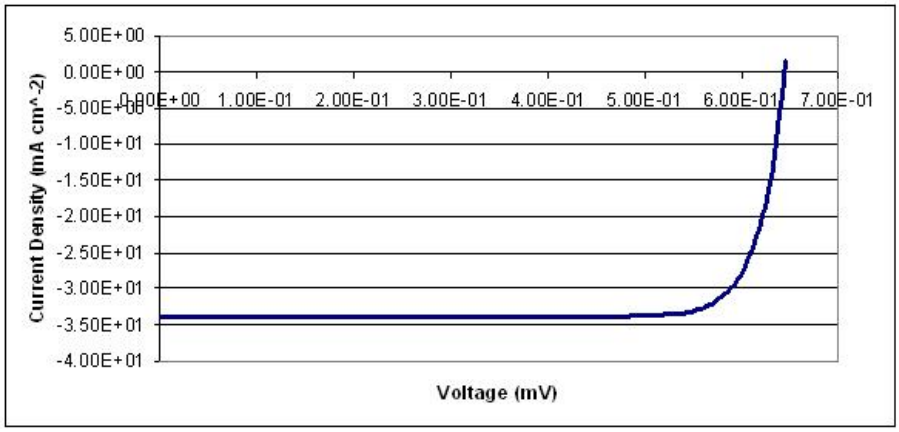


Figure 4.6: Calculated Si JV Curve

The performance of this theoretical Si solar cell will be compared both with and without the addition of either a GaP or a GaAsP solar cell on top.

4.5 GaP Solar Cell

The standalone GaP solar cell was analyzed using the same technique described in detail in Section 4.4. First, material properties were determined, and artificial boundary conditions were set. The parameters used for the GaP material system are shown in Figure 4.7.

GaP Material Parameters			
P Region		N Region	
ni (cm^-3)	2	ni (cm^-3)	2
µn (cm^2/Vs)	250	µp (cm^2/Vs)	150
Dn (cm^2/s)	6.465	Dp (cm^2/s)	3.879
τn (sec)	1.00E-07	τp (sec)	1.00E-06
Ln (cm)	0.000804052	Lp (cm)	0.00197

Figure 4.7: GaP Cell Structure and Material Properties

The absorption coefficient data was then calculated, to produce the curve shown in Figure 4.8.

Following determination of the absorption coefficient data, G for the entire 2 μm thickness of the GaP junction was calculated. Fundamental assumptions came into play at this point, where the details of device performance calculation for the GaP solar cell diverge very slightly from the calculations for the Si solar cell.

In the calculations for the Si solar cell, the determination of J_{sc} took into account varying material parameters for n-type versus p-type Si that would affect collection of the generated carriers. For the analysis of the GaP solar cell, however, the assumption was made that all carriers generated would be collected, eliminating the need to use Equation 4.3, and only requiring the use of Equation 4.2 over the full 2 μm GaP thickness for calculation of J_{sc}. The remainder of the device analysis followed the same procedure as used for Si, implementing Equations 4.4, 4.5, 4.6, 4.7, and 1.1.

The device performance summary is shown in Table 4.2, and the JV curve is shown in Figure 4.9.

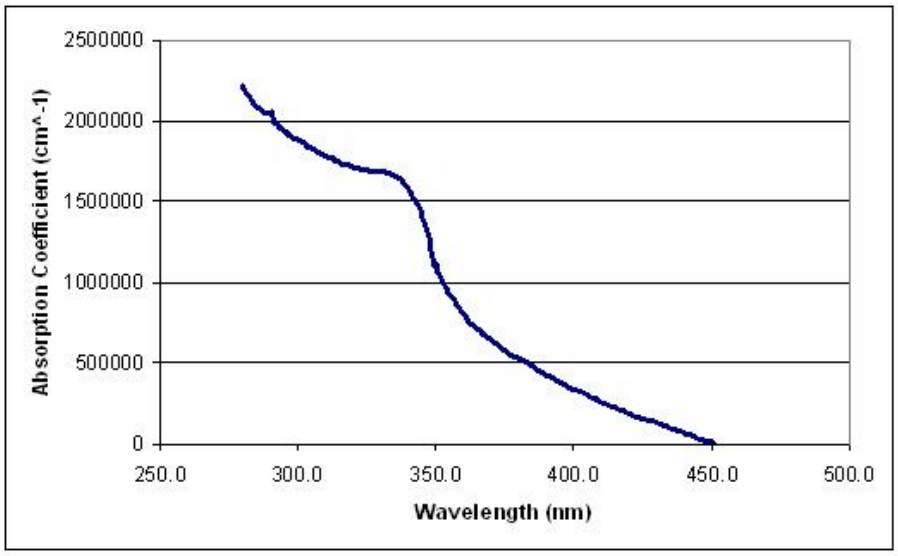


Figure 4.8: GaP Absorption Coefficient Data

4.6 GaAsP Solar Cell

The GaAsP cell proved to be a greater challenge to theoretically model according to the methods used for Si and GaP. This is due to the fact that little to no material properties exist in common knowledge for this material. As such, assumptions had to be made at each step of the analysis in order to come as close to modeling the GaAsP system, depicted in Figure 4.10, as possible.

Table 4.2: Theoretical Device Results for GaP Solar Cell

Parameter	Calculated Result
$J_0(\frac{mA}{cm^2})$	5.28x10^{-26}
$J_{sc}(\frac{mA}{cm^2})$	3.55
V_{oc} (V)	1.54
$P_{max}(mW)$	5.61
FF	92.07%
η	5.61%

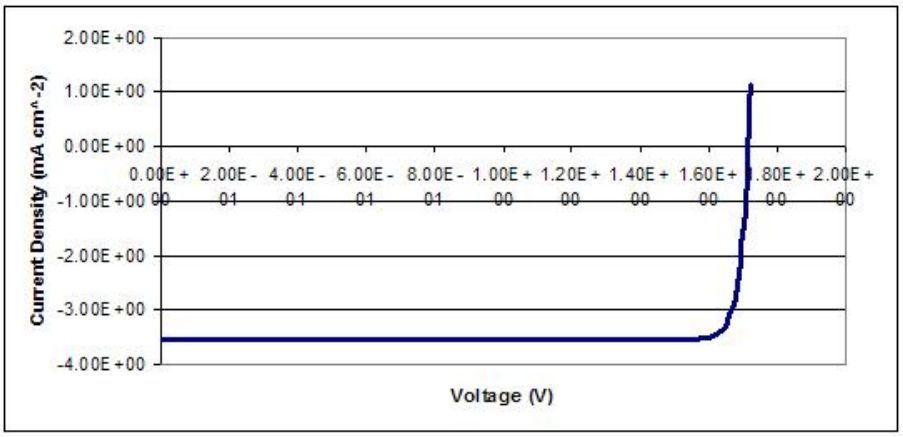
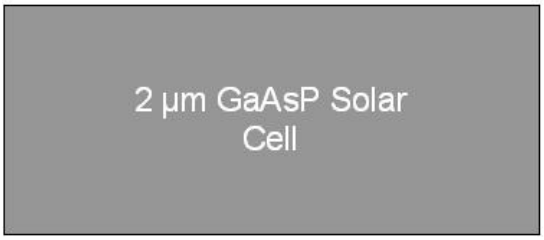


Figure 4.9: Calculated GaP JV Curve

The first parameter that required calculation was, again, the absorption coefficient data. This calculation began with a determination of the GaAs absorption coefficient data, using the same methodology as for both Si and GaP. The assumption was then made that the GaAsP absorption coefficient data would have a tail mimicking the GaAs curve, but shifted into the proper regime for the GaAsP bandgap. The relationship of the curve tail with regard to the GaAs bandgap was determined, then this same relationship was applied to GaAsP so as to shift the tail for the GaAsP bandgap. The resulting absorption coefficient curves are displayed in Figure 4.11.

Once the absorption coefficient data was determined for GaAsP, Equations 4.1 and 4.2 were used to calculate the J_{sc} using the same assumption as the comparable calculation for the GaP cell - all generated carriers would be collected as current.

Once the J_{sc} was calculated, the next step was to determine the J_0 and V_{oc} for the system. The complication stemming from lack of material property data is again an issue, here. Equation 4.4, used for calculating J_0, requires material properties in order to complete the calculation, and Equation 4.5, used for calculating V_{oc},



GaAsP Material Parameters	
Nc (cm^-3)	4.7E17
Nv (cm^-3)	7.0E18
Eg (eV)	1.81
w (cm^2)	2E-4

Figure 4.10: GaAsP Cell Structure and Material Properties

requires J_0. The challenge, then, was to determine a methodology for calculating J_0 without the material properties required for the standard J_0 equation. Such a method exists for direct bandgap materials, which is a characteristic of GaAsP. This method involves the use of the semiconductor's bandgap and an approximation of the intrinsic carrier concentration term based upon standard relationships for direct-bandgap materials. The equation set for solving for J_0 is the following:

$$B = 3x10^{-10}(\frac{E_g}{1.5})^2(\frac{300}{T})^{1.5} \tag{4.8}$$

$$n_i^2 = N_c N_v e^{\frac{-E_g}{kT}} \tag{4.9}$$

$$J_0 = qn_i^2 wB \tag{4.10}$$

where w is the thickness of the base layer of the cell and B is the radiative recombination coefficient [1, 10]. Solving Equation 4.8 is very straightforward, with the E_g being set at 1.81eV, and T being set to 300K, for an answer of 4.37x$10^{-10}\frac{cm^3}{s}$. In solving for n_i^2 in Equation 4.9, however, an approximation must be made involving

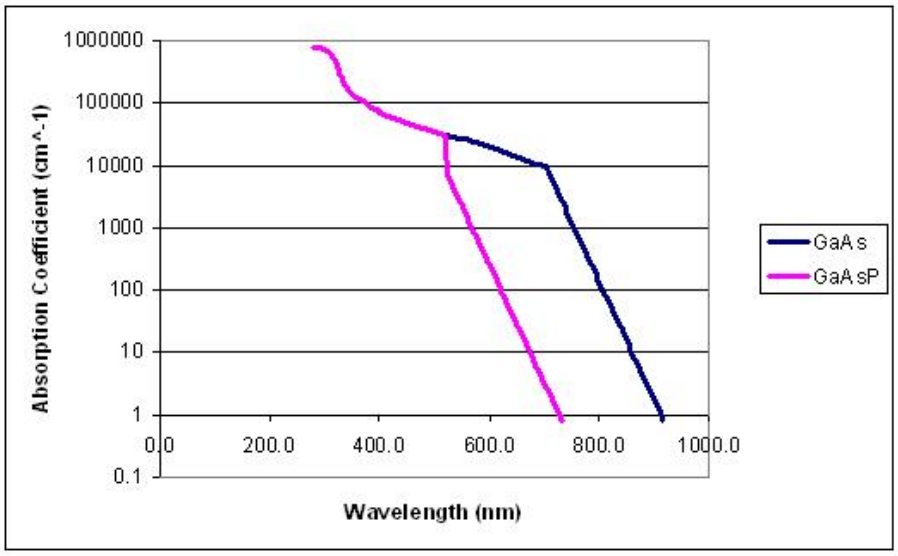


Figure 4.11: Calculated GaAsP Absorption Data from GaAs Absorption Data

the N_cN_v product. For direct bandgap materials, the approximation is that this product is constant for all materials. The product, therefore, was determined using the N_c and N_v values for GaAs at the appropriate dopant levels for this application. This product was found to be 3.29x10^{36} cm^{-6}, and completing the calculation for n_i^2 results in the intrinsic carrier concentration squared being 1.32x10^6 cm^{-6}. The thickness, w, is defined as the thickness of the base region of the cell. As seen in the model for a Si solar cell, the emitter thickness is negligible when compared to the thickness of the base region. For this reason, w was defined as the full 2 μm thickness of the GaAsP epitaxial growth.

After all supplementary calculations were performed, the resulting calculation for J_0 using this method was 1.848x10$^{-23}\frac{mA}{cm^2}$. Then, Equation 4.5 was used to calculate the V_{oc}, with a result of 1.428 V. It was important to determine whether or not this set of equations returned an appropriate answer given the nature of our system. The generally-accepted approximation of V_{oc} for any III-V material is E_g - 0.4.

Table 4.3: Theoretical Device Results for GaAsP Solar Cell

Parameter	Calculated Result
$J_0(\frac{mA}{cm^2})$	1.85x10^{-23}
$J_{sc}(\frac{mA}{cm^2})$	17.4
V_{oc} (V)	1.43
$P_{max}(mW)$	22.6
FF	91.01%
η	22.62%

In our case, the bandgap of GaAsP is 1.81eV, therefore the general approximation would allow for a V_{oc} of 1.41 V. The difference between the accepted approximation and the method implemented was only 0.018 V - indicating the validity of this method.

The calculated device performance parameters are summarized in Table 4.3, and the JV curve is shown in Figure 4.12.

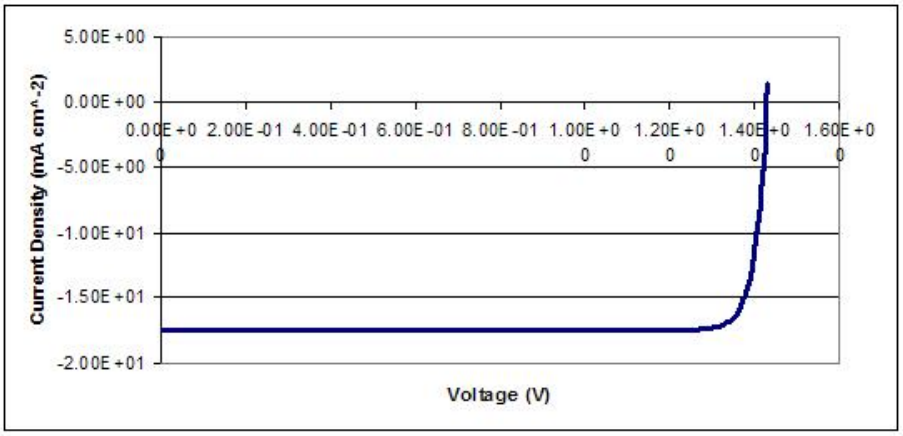


Figure 4.12: Calculated GaAsP JV Curve

4.7 Multijunction Device Performance

Once the three individual material systems to be implemented in the ultimate device design have been analyzed, the model must be changed to consider the materials' affects on each other when built into a single device.

Adjustments to the model consider the effect of placing either a GaP cell or a GaAsP cell above a Si solar cell. The main adjustment considers reduced generation of carriers in the Si, as a portion of above-bandgap photons would be absorbed by the new top junction. This will, firstly, reduce the J_{sc} of the Si cell. Issues of current matching are not considered for this work due to the assumption of separate electrical terminals for the two junctions. This provides a best-case scenario analysis of the device structure.

The remainder of the device analysis completes the determination of the device parameters calculated for the individual systems: J_0, V_{oc}, FF, and η.

Ultimately, the absolute efficiency gain by the addition of a III-V top junction above Si is determined.

4.7.1 GaP Solar Cell on a Si Solar Cell

The first step for analyzing the new performance of the Si solar cell with a GaP junction above was to adjust the generation in Si at each wavelength by subtracting the generation occurring in the GaP.

Once this adjustment was applied, the resulting J_{sc} was 30.35 $\frac{mA}{cm^2}$. This was a decrease of 3.57 $\frac{mA}{cm^2}$ from the Si device before the addition of a top junction. It was also approximately the J_{sc} of the GaP cell, indicating that the current merely moved from production in one junction to the other.

The J_0 term of the Si is not affected by the addition of a top junction, as it is based solely upon inherent material properties rather than device performance characteristics. The other terms do not remain unaffected, however, as they all have a direct relationship with J_{sc}.

Table 4.4: Comparison of Theoretical Device Results for a Si Before and After the Addition of GaP Top Junction

Parameter	Without GaP	With GaP
$J_0(\frac{mA}{cm^2})$	5.04x10^{-10}	5.04x10^{-10}
$J_{sc}(\frac{mA}{cm^2})$	33.92	30.35
V_{oc} (mV)	645	642
$P_{max}(mW)$	18.3	16.3
FF	83.62%	83.57%
η	18.29%	16.28%
Total η	18.29%	21.88%

The remaining parameters of V_{oc}, FF, and η were then calculated. The V_{oc} parameter decreases 3 mV from the previous calculation for a bottom junction V_{oc} of 642 mV. The FF had no change - remaining at 83.6%. Due to a decrease in both J_{sc} and V_{oc}, efficiency in the Si cell decreased from 18.29% to 16.28%. Adding this to the 5.6% efficiency of the GaP top cell, the total efficiency of the multijunction cell is 21.88%, a relative efficiency gain of 20% and an absolute efficiency gain of 3.0% over a single junction Si solar cell. The results summarizing the cell performance before and after the addition of the GaP top junction are displayed in Table 4.4.

4.7.2 GaAsP Solar Cell on a Si Solar Cell

The analysis of the effects caused by placing a GaAsP top junction over Si proceeded in the same manner as the analysis described in Section 4.7.1, beginning with the adjustment of generation in Si taking into account the shift of some above-bandgap carrier generation occurring in the GaAsP. The remaining calculations for V_{oc}, FF, and η followed the standard method.

The resulting effects for the Si solar cell device parameters included a decrease in J_{sc}, V_{oc}, FF, and η for the Si solar cell alone due to the shift in some carrier generation from the Si junction to the GaAsP junction. The Si J_{sc} decreased to

Table 4.5: Comparison of Theoretical Device Results for a Si Before and After the Addition of GaAsP Top Junction

Parameter	Without GaAsP	With GaAsP
$J_0(\frac{mA}{cm^2})$	5.04x10^{-10}	5.04x10^{-10}
$J_{sc}(\frac{mA}{cm^2})$	33.92	16.57
V_{oc} (mV)	645	626
$P_{max}(mW)$	18.3	8.64
FF	83.62%	83.27%
η	18.29%	8.64%
Total η	18.29%	31.24%

16.57 $\frac{mA}{cm^2}$, a total drop of 17.35 $\frac{mA}{cm^2}$, the same J_{sc} of the GaAsP solar cell. This result indicates that the generation lost to the Si junction merely shifted from the bottom junction to the top junction, just as seen with the GaP/Si device. The V_{oc} decreased 19 mV to 626 mV, a result of the large decrease in J_{sc}. The decrease in both J_{sc} and V_{oc} had a large enough magnitude in the case of the GaAsP to also affect the FF - resulting in a drop from 83.6% to 83.3%, which is still a very small decrease. Efficiency of the Si junction decreased to 8.64%, however, the addition of the GaAsP junction adds 22.6% efficiency to the device. This results in a device efficiency of 31.24%, an impressive relative efficiency gain of 71% and an absolute efficiency gain of 13% over the Si solar cell.

The results summarizing the cell performance before and after the addition of the GaAsP top junction are displayed in Table 4.5.

Chapter 5

CONCLUSIONS AND FUTURE WORK

5.1 Conclusions

Conclusions for this work address both the experimental and the theoretical results discussed throughout the paper.

Beginning with the growth methodology and results, it is clear that, in order to produce a device-quality epitaxial GaP layer using LPE, Sn is not an appropriate metal solvent. Due to this challenge, it is necessary to adjust the growth methods and parameters in order to reduce the Si concentration in the initial GaP buffer layer to protect the layer from complete etching by the Ga metal solvent desired for further good epitaxial GaP growth from LPE.

Methods for reducing Si concentration in the GaP epitaxial layer include precise substrate orientation control. For our system, a Si(111) substrate is required, with results indicating that a 4° miscut must also be present in addition to this initial substrate orientation.

Growth temperature, rate, and area also affect the quality of the resulting epitaxial growth layer. Although GaP may be soluble in Sn at much lower temperatures than used for this growth method, temperatures that are too low will, in fact, hinder the growth of GaP. In addition, despite literature results indicating better results with faster growth rates, our system has shown the opposite affect. Faster growth rates produce much poorer results in our system than do slower growth rates. Growth area - which can also be precisely controlled - has shown that minimizing

the growth areas required to be covered actually decreases the Si concentration in resulting epitaxial GaP layers when compared to larger growth areas on the same substrate in the same growth run. Controlling growth area through opening windows in Si_3N_4 also provides an added benefit in protecting the Si substrate from etching by the Ga solvent once further growth layers are ready to be grown.

There is also promise in implementing a competitive growth regime by adjusting the relationship of saturation, supersaturation, and undersaturation of the GaP and Si - the two semiconductor materials present in the melt which will attempt nucleation on the surface of the substrate. By adjusting these relationships between the saturation state of the two materials, it is possible to enhance the nucleation and growth of GaP while limiting the growth of Si and its insertion into the epitaxial layer.

Theoretical analysis shows that, once the III-V materials of GaP and GaAsP are able to be grown on this buffer layer to produce a second junction, the resulting devices would have absolute efficiency increases of 3% and 10%, respectively, over the performance of a single junction Si solar cell alone. This result indicates the promise of increased device efficiency which makes the continuation of this work worthwhile.

5.2 Future Work

This body of work, while a starting point for the improvement of epitaxial growth of GaP on Si through LPE, still requires additional work before further layer growth can be applied. The first step for future work, therefore, is to continue to develop understanding of the growth interactions occurring during LPE, optimize growth parameters based upon this increased understanding, and, ultimately, produce an epitaxial GaP layer on Si via LPE with a Si concentration that does not degrade the resistance to etching by Ga.

Once this epitaxial layer is achieved, methods for the subsequent growth of additional layers of GaP and GaAsP should be developed, tested, and optimized. The resulting growth layers can then be fabricated into complete dual-junction solar cell devices. These devices can be tested and analyzed in order to indicate further areas of potential growth or device fabrication optimization.

The final step for this work, once GaP and GaAsP devices have been successfully grown on a Si substrate, would be to include Si device fabrication to make the structure a true dual-junction III-V/Si solar cell, followed by the appropriate device testing, analysis, and optimization.

Ultimately, the future for this work is the complete fabrication, testing, analysis, and optimization of a separate terminal, dual junction, III-V on Si solar cell device. Any and all steps leading from this body of work in order to achieve this goal can be considered future work.

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Appendix

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