

**THE EFFECT OF SILICON AND COPPER-INDIUM-GALLIUM-SELENIDE
BASED SOLAR CELL STRUCTURES AND PROCESSING ON
TEMPERATURE DEPENDENT PERFORMANCE LOSSES**

by

Judith Hsieh

A thesis submitted to the Faculty of the University of Delaware in partial fulfillment of the requirements for the degree of Master of Science in Electrical and Computer Engineering

Fall 2014

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ABSTRACT

Temperature dependent current voltage measurements (J-V-T) of solar cells provide both fundamental and practical information. They give detailed insight into recombination losses within the device as well as information about module performance losses at higher outdoor operating temperatures. In this thesis, J-V-T measurements were applied to two distinctly different types of solar cells: crystalline silicon heterojunction cells and thin film (AgCu)(InGa)Se₂ or ACIGS polycrystalline cells. Crystalline silicon solar cells with heterojunction structure improve the open-circuit voltage and efficiency. Interdigitated back contact (IBC) Si solar cells obtain a higher short-circuit current and fill factor compared to front heterojunction (FHJ) solar cells. ACIGS solar cells have shown higher efficiencies at wider bandgap compared to the baseline CIGS solar cells. Two high open-circuit voltage CIGS solar cells are included and compared with ACIGS solar cells. In this thesis, the impact of different types of solar cells structure and fabrication on temperature dependent performance losses will be discussed. Devices with higher bandgap are predicted to have higher open-circuit voltage and lower temperature coefficient of maximum power output (P_{\max}). The correlation between temperature coefficient of P_{\max} and open-circuit voltage can be found in Si FHJ cells but not Si IBC or ACIGS cells. However, ACIGS cells show an inverse correlation between temperature coefficient of P_{\max} and bandgap as expected. Analysis of diode quality factor and other parameters are interpreted. S-shape J-V curve can reduce the device's fill factor with a relative high series resistance. This phenomenon tends to occur in FHJ cells rather than IBC at low temperature.

Light-dark crossover and roll over effects are commonly seen in ACIGS cells and the anomaly is enhanced at lower temperature. Most of FHJ and IBC cells obtain the ideality factor between 1 and 2 while some of ACIGS cells obtain the ideality factor less than 1 or larger than 2. The value of the ideality factor may be limited by different recombination mechanism.

Chapter 1

INTRODUCTION

As the demands for new energy resources have grown in recent decades, photovoltaic (PV) technology shows importance for its renewable and environmentally friendly properties among other energy resources. Nowadays, PV modules are installed not only at utility scale (MW) but also at a residential scale (kW). Fig 1.1 shows that cumulative amount of PV modules installed worldwide from 2000 to 2012 increased by over a factor of 80. There is now over 100 GW of PV capacity.

Solar energy can be converted into electric energy directly (the photon energy E_{ph} is greater than the bandgap E_g) from a PV module using the concept of p-n junction as shown in Fig 1.2.

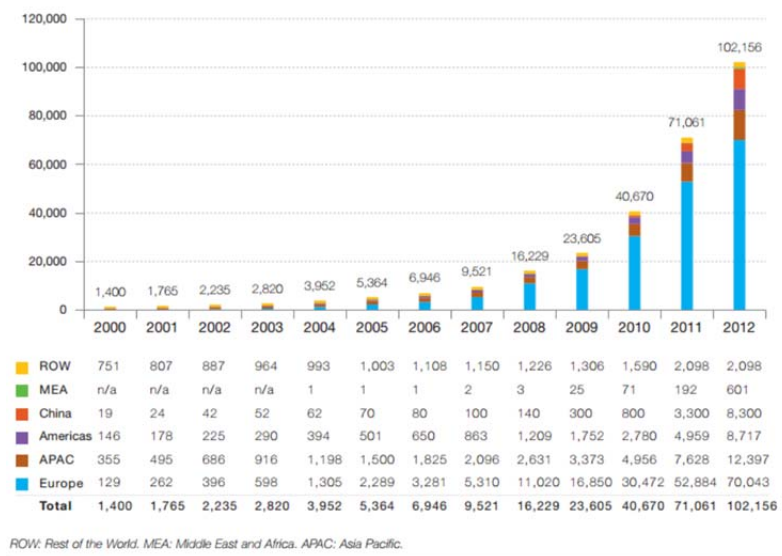


Figure 1.1 Evolution of global PV cumulative installed capacity from 2000 to 2012 (MW)[1].

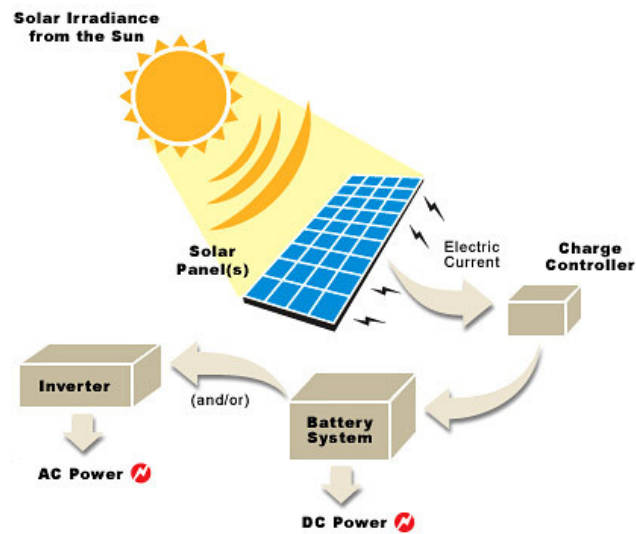


Figure 1.2 The route of solar energy converted into electric energy[2].

Most of the PV modules are made of crystalline silicon (c-Si) wafer, including p-type or n-type, monocrystalline and polycrystalline silicon. In particular, the significant advantage of crystalline silicon solar cell is relative high conversion efficiency from solar energy to electric energy. Another potential type for making PV module is thin-film solar cell (TFSC), which is also called second generation solar cell. Thin-film solar cells, including amorphous silicon (a-Si), CdTe and Cu(InGa)Se₂-based solar cells, show low cost, high kWhr/kW output and comparable long-term stability comparable to crystalline silicon[3]. In order to improve the cost/W compared to other renewable energy resources, many researchers are directing their efforts on designing high throughput and low cost TFSC[3]. In this thesis, different structures of crystalline Si-based and CIGS-based solar cells are measured and discussed separately.

Crystalline Si-based solar cells measured in the thesis are fabricated with a heterojunction structure which improves the open-circuit voltage V_{oc} and efficiency compared to c-Si homojunction structure[4]. Two different types of c-Si-based heterojunction solar cells are introduced. The first one is front heterojunction (FHJ) solar cell, which shows the excellent passivation properties of a-Si:H with low temperature processing (below 200°C)[5]. Another advantage of front heterojunction solar cell is the straightforward process step that can make the process cost less. The second c-Si-based solar cell is interdigitated back contact (IBC) solar cell. With interdigitated positive and negative electrodes on the rear, it is easy to connect than the front heterojunction (FHJ) solar cell. Also, due to its lack of grid shadowing, excellent front surface passivation and textured surface with anti-reflective (AR) coatings, it shows enhancement of light trapping ability and higher short-circuit current J_{sc} than

the FHJ cells[6]. Recently, an IBC heterojunction solar cell made by Panasonic became the champion Si solar cell with an efficiency of 25.6%[7].

CIGS-based solar cells are also heterojunction and have the higher efficiency than any other thin-film solar cells. The highest one achieves an efficiency of 21.7%[8]. From alloying different content of Ag/(Ag+Cu) and of Ga/(In+Ga), the increase of bandgap and open-circuit voltage can be achieved[9]. Thus, with the characteristics of wider bandgap and higher open-circuit voltage, (AgCu)(InGa)Se₂ solar cells are of interest for higher efficiency.

In this thesis, the results of J-V-T measurements and analysis of the temperature-dependence behaviors by comparing different cell structure are shown. The activation energy E_a , ideality factor A, series resistance R_s , and temperature coefficients are calculated from analysis of the data using standard models for each type of FHJ cells, IBC cells and ACIGS cells. Activation energy and ideality factor help to identify the recombination mechanism. A focus of this thesis is to determine if there is a correlation between temperature coefficient of P_{max} and the bandgap (for CIGS cells) or the open-circuit voltage (for c-Si heterojunction cells) since it is widely claimed that such modules will have a smaller temperature coefficient compared to standard c-Si modules. A smaller temperature coefficient will enable to the module to perform well at high temperature. The J-V curve of some devices show anomaly at low temperature such as s-shaped, roll over and crossover effects [10-13] and thus result in higher series resistance, lower maximum power output and ideality factor varied with temperature. In summary, the discussion of J-V-T measurements and results will be included in the following chapters.

1.1 Thesis Outline

In chapter 2, silicon front heterojunction, IBC and ACIGS solar cells' structures and brief process steps are introduced.

In chapter 3, experimental equipment for J-V-T measurement and measurement procedure are discussed.

In chapter 4, solar cell parameters, J-V-T characteristics, diode equations and analysis are discussed.

In chapter 5, J-V-T measurements of different types of silicon front heterojunction and IBC solar cells are presented and interpreted.

In chapter 6, J-V-T measurements of ACIGS solar cells with different process stage and contents of Ag and Ga are presented and interpreted.

The summary and conclusions are included in chapter 7. Further works are mentioned as well.

Chapter 2

SILICON AND ACIGS SOLAR CELL'S DEVICE STRUCTURE AND FABRICATION

2.1 Silicon Front Heterojunction (FHJ) Solar Cell

Fig 2.1 shows the structure of the silicon heterojunction solar cell. With the straightforward variation process steps, two different structures shown in Fig 2.2 and Fig 2.3 were also fabricated and measured. Compared to the device shown in Fig 2.1, the device in Fig 2.2 is without the intrinsic a-Si passivation layer on the front. The device in Fig 2.3 has a different n-layer contact pattern on the back. Instead of a blanket n-layer deposition, the n-layer is deposited in long strips duplicating the same processing and spatial dimensions as the n-strips on the IBC cell. The results of J-V-T characterization will be discussed in Chapter 5.

2.1.1 Structure of the FHJ Si Cells

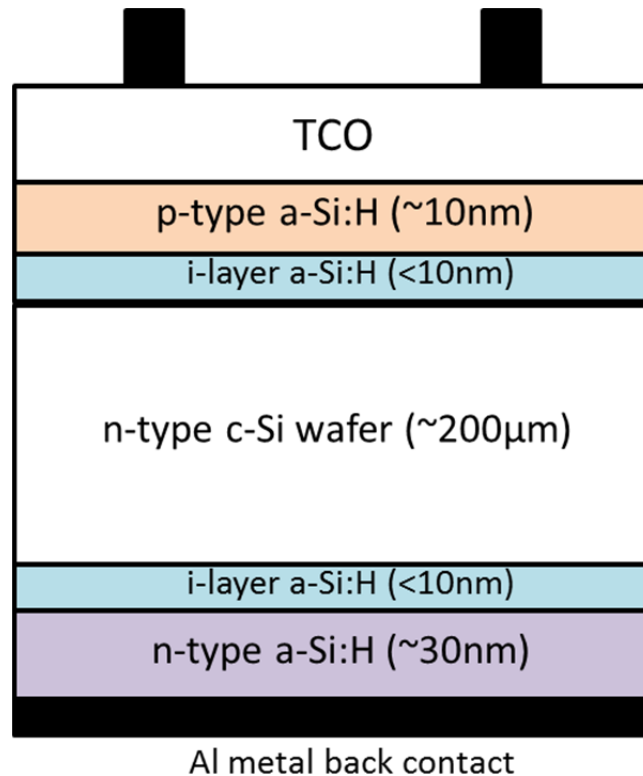


Figure 2.1 Cell structure of standard silicon front heterojunction solar cell with front i-layer and blanket rear n-layer.

2.1.2 Basic Process Steps

The process steps are as following:

1. Clean and texture wafer using wet chemical solutions.
2. Deposition of intrinsic a-Si:H on both sides of n-type c-Si wafer by plasma enhanced chemical vapor deposition (PECVD).
3. Deposition of n-type a-Si:H on the back and p-type a-Si:H on the front successively by plasma enhanced chemical vapor deposition (PECVD). This is

done without breaking vacuum by using a flipper substrate holder in the PECVD chamber.

4. Transparent conductive oxides (TCO) film is deposited on the top by sputtering (also serves as anti-reflection layer).
5. Silver front grids and Aluminum rear metal contacts deposited by electron beam deposition.

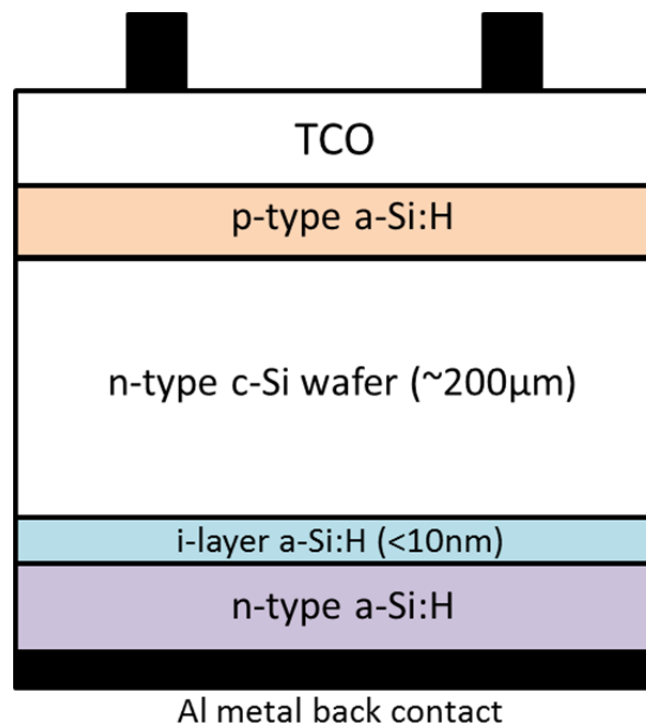


Figure 2.2 Front heterojunction device without i-layer passivation on the front.

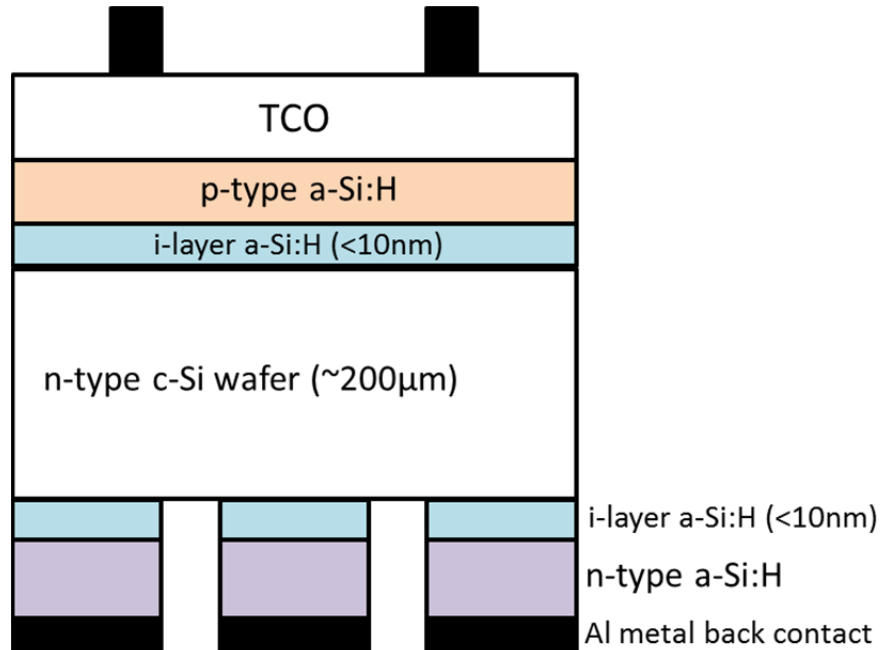


Figure 2.3 Device with front a-Si i-layer but with n-strips on the back. There are 9 strips which are $250 \mu\text{m}$ wide and 1.285cm long connected by a bus bar at the end.

2.1.3 Fabrication

First, the Si samples are cut from a c-Si wafer in dimension (1 0 0). Then they are textured by etching and cleaning by wet chemical solutions. The purposes of the surface texturing are to reduce reflection on the surface and increase light trapping. Wafer cleaning process is important due to the defect and impurity removal on the interface.

After cleaning which leaves a H-terminated Si surface with negligible oxide or contamination, the samples are immediately loaded into the PECVD system and pumped down to vacuum to prepare for the a-Si:H layer depositions. Both intrinsic and p and n doped a-Si layers are deposited in the system.

Plasma-enhanced chemical vapor deposition is a common method used to deposit amorphous silicon layers. Radio frequency (RF) is an external energy source used to generate plasma. The reaction should be at very low pressure (vacuum) to prevent impurities from being incorporated into films. Different types of a-Si layers are deposited in different chambers. The film deposition temperature is 200°C to 300°C.

The cell is completed by depositing the contact layers. The ITO (Indium Tin Oxide) layer is transparent conductive oxide (TCO) that is deposited by sputtering on the a-Si:H layers. It provides a low resistance path for the current to the grids and is the primary anti-reflective layer. The thickness of the ITO is 80nm with a sheet resistance around 50~70 Ω /square. Different thickness will influence the sheet resistance and transmittance of the light[14].

The front metal is Ag deposited by electron beam evaporation through a mask to give grids covering 4% of the total cell area. Aluminum is deposited by electron beam deposition as the back contact. Ag is used on the front grids because it is more conductive than Al and reduces the resistance losses in the narrow grid fingers.

2.2 Interdigitated Back Contact (IBC) Solar Cell

2.2.1 Structure

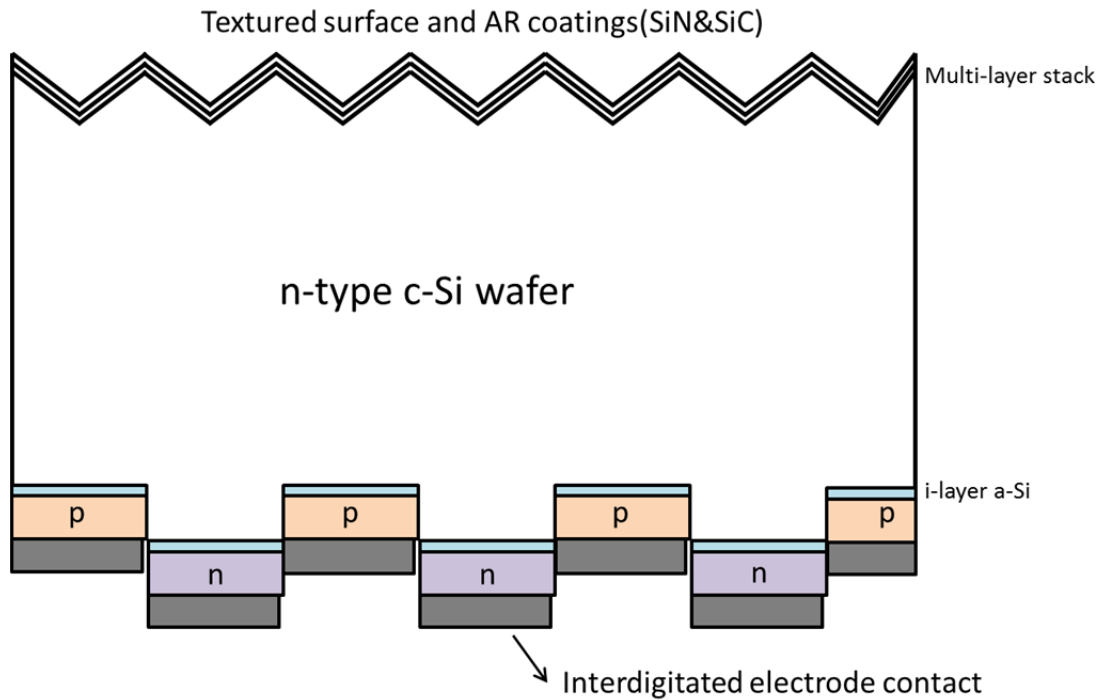


Figure 2.4 Structure of IBC-SHJ solar cell.

The fundamental interdigitated back contact silicon heterojunction (IBC-SHJ) solar cell structure is shown in Fig 2.4. The multi-layer stack on the front includes: amorphous silicon carbide, amorphous silicon nitride and intrinsic amorphous silicon layers. By changing the front surface field passivation methods and the diffusion process, different types of solar cells are shown in Table 2.1. Device MC1497-09 and MC1503-04 are made with two different passivation methods. One is with only the passivation of n-type a-Si:H, and the other one is with passivation of n-type a-Si:H on

the standard passivation of i-layer a-Si:H. Front surface passivation can reduce the recombination losses. Another comparison between device MC1483-06, MC1483-10 and MC1492-02 shown in Table 2.1 is with or without n+ diffusion on the front. Fig 2.5 shows the sample of IBC cell. Different cell structure behaviors and results from J-V-T measurement will be discussed in Chapter 5.

Table 2.1 IBC cells with different passivation methods on the front-surface field.

Cell number	Description
MC1497-09	n type a-Si
MC1503-04	i and n type a-Si
MC1483-06	no n+ diffusion
MC1483-10	n+ diffusion
MC1492-02	n+ diffusion

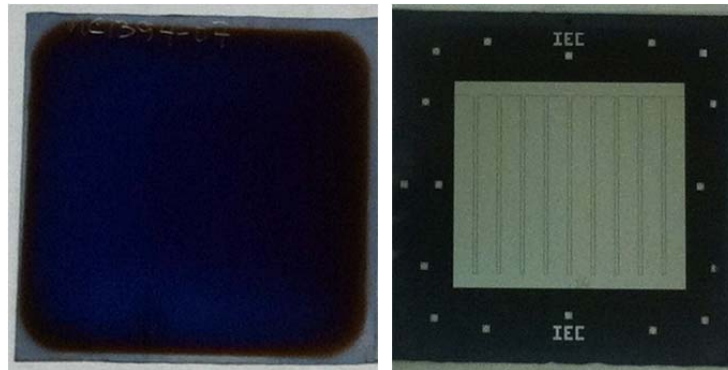


Figure 2.5 IBC piece with 2.5 cm² cell area. Front side (left) consists of textured surface and multi-layer stack. Rear side (right) consists of n-strip and p-strip contacts.

2.2.2 Fabrication

The process flow for the IBC-SHJ cells described above is shown in the following diagrams:

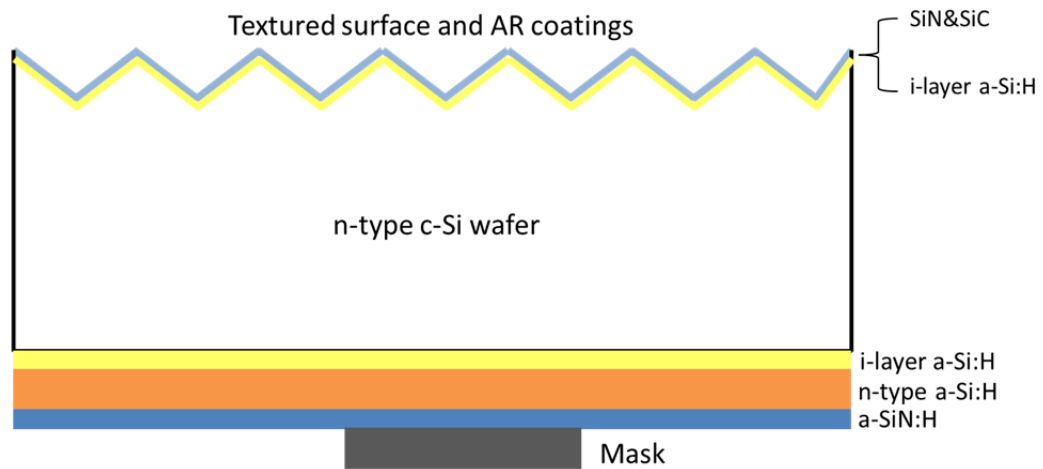


Figure 2.6 Clean the c-Si wafer and create textured surface. Deposit front passivation and anti-reflection stack. An i-layer a-Si:H is deposited on both front and rear side of the wafer. Continue to deposit n-type a-Si:H and silicon nitride on the rear. Photoresist masking is used to protect the layers from etching off.

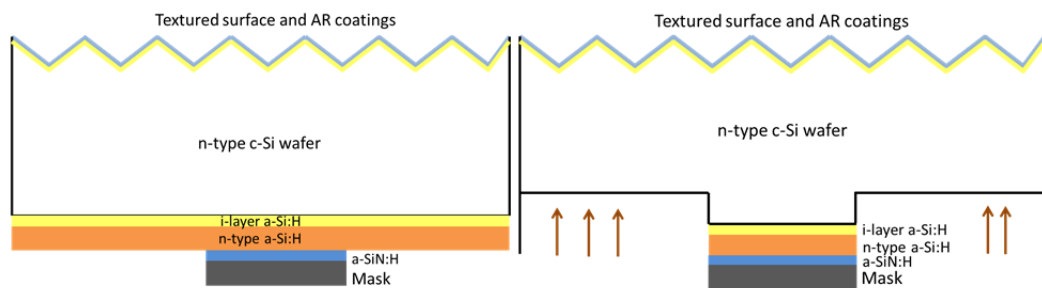


Figure 2.7 Chemical etching for silicon nitride, n-type a-Si:H, and i-layer a-Si:H.

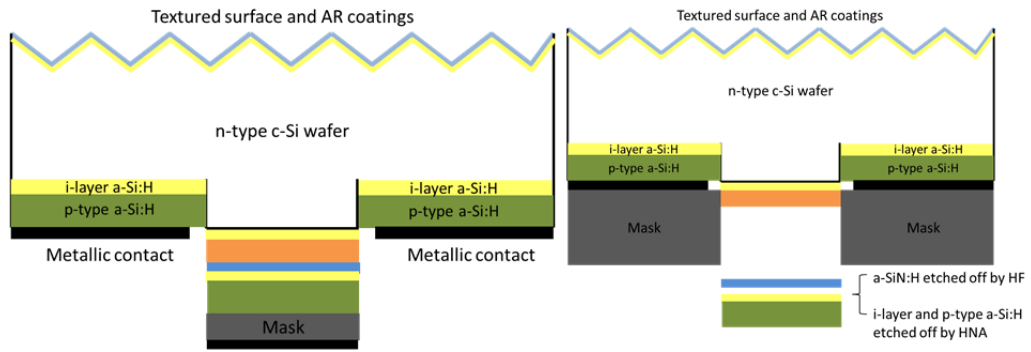


Figure 2.8 Deposition of i-layer a-Si:H and p-type a-Si:H. Apply and pattern photoresist leaving openings on the p-contact. Metallization. Lift off the photoresist masking. Etch off the p-type a-Si:H, i-layer a-Si:H and silicon nitride under photoresist.

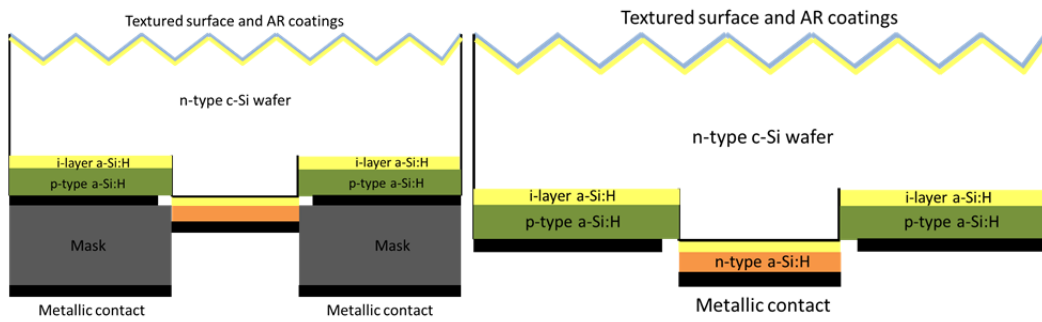


Figure 2.9 Apply and pattern photoresist leaving openings on the n-contact. Metallization. Lift off the photoresist masking.

2.3 ACIGS Solar Cell

2.3.1 Structure

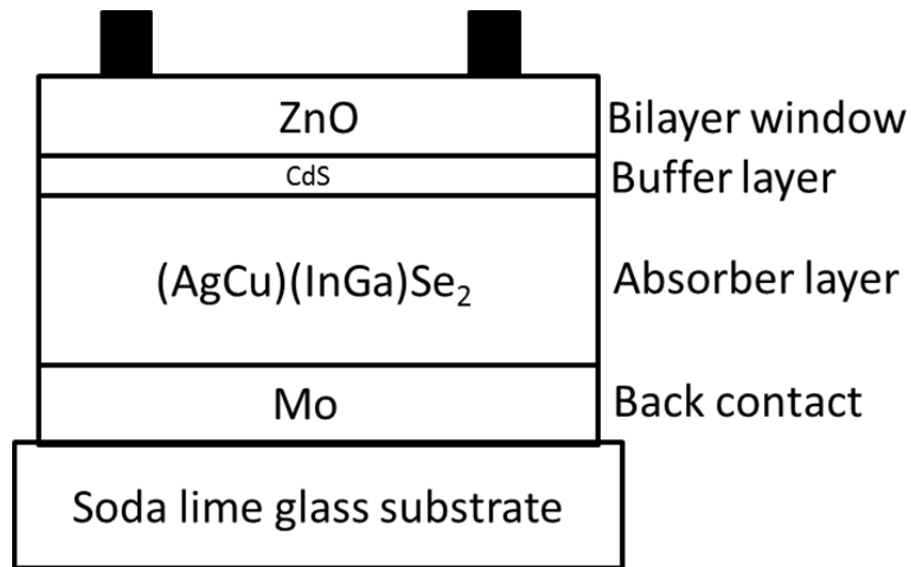


Figure 2.10 Cell structure of ACIGS solar cell.

ACIGS solar cells use the substrate device structure as shown in Fig 2.10. Soda lime glass (SLG) is a substrate that provides a stable surface with good adhesion with molybdenum layer and a path for sodium to easily diffuse from molybdenum to absorber layer. Sodium is essential for good electronic properties of the ACIGS layers. Molybdenum layer is sputtered on the SLG substrate as a back contact. After the back contact is the p-type ACIGS absorber layer. In this work, the effect of various ACIGS depositions and compositions are compared[9, 15]: 1 stage to 3 stage evaporation process, varying the content of Ga as in the ratio $Ga/(In+Ga)$ and Ag as in the ratio $Ag/(Cu+Ag)$ in this layer will affect the bandgap-gradient and variation on open-

circuit voltage. The results will be discussed in Chapter 6. A thin layer n-type CdS (50 nm) serves as the buffer layer in the p-n heterojunction formation. The front transparent conducting oxide (TCO) contact can be viewed as bilayer window that is composed of ITO (Indium Tin Oxide) with intrinsic ZnO. Fig 2.11 shows the sample of ACIGS solar cell.



Figure 2.11 ACIGS piece with four cells. Cell areas are 1.00 or 0.4 cm². The shiny white metal region on the left is an Indium solder used to connect the front metallic grid to Mo back contact of the cell.

2.3.2 Fabrication

The process flows are shown as following figures:

Substrate cleaning and Mo dc sputtering

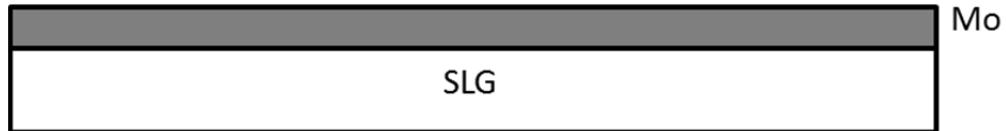


Figure 2.11 After cleaning the soda lime glass (SLG) substrate, a Mo back contact is deposited by direct current (dc) sputtering. It has low sheet resistance and good adhesion properties on the substrate.

Chemical bath deposition of CdS



Figure 2.12 Deposition of absorber layer (ACIGS) by using coevaporation and buffer layer (CdS) by chemical bath deposition (CBD). This forms the p-n heterojunction.

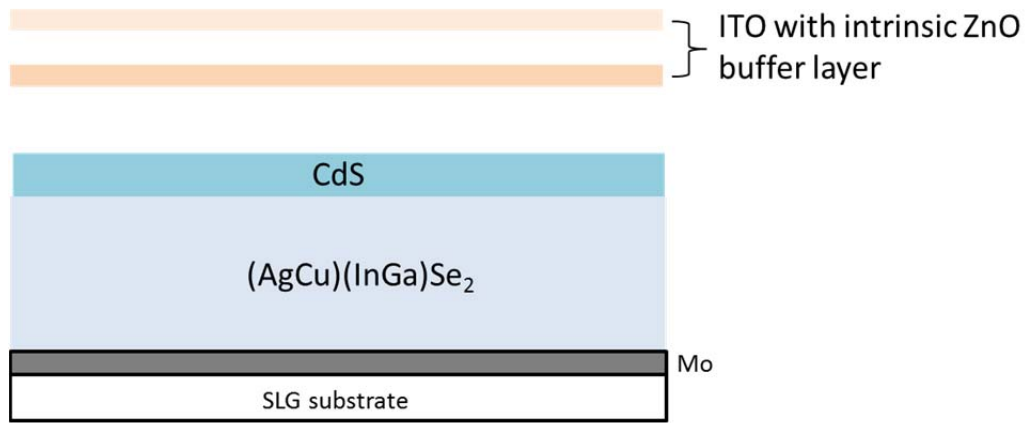


Figure 2.13 Deposition of the bilayer window ZnO by sputtering and then scribe.

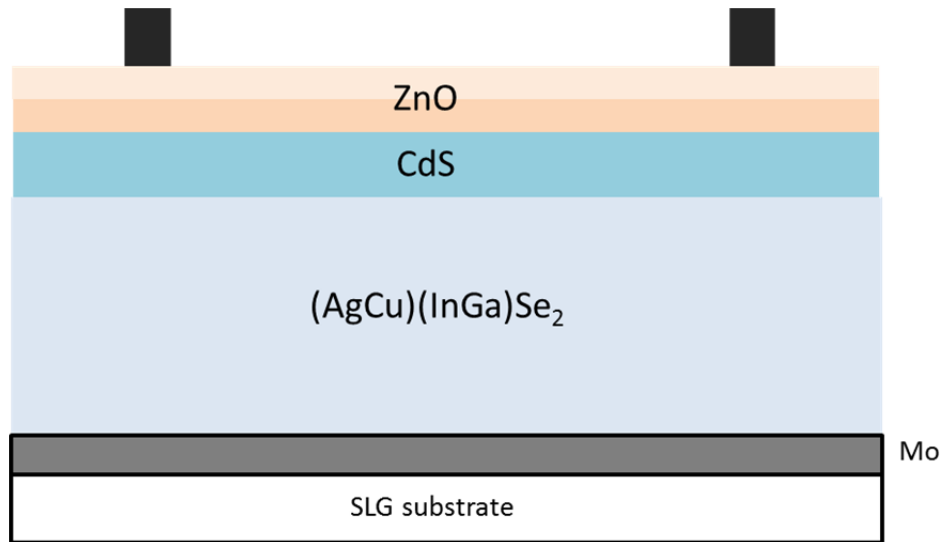


Figure 2.14 Deposition of the metallic grid (Ni/Al) on the top using a shadow mask for grid patterning.

Chapter 3

EXPERIMENTAL MEASUREMENTS

J-V-T measurement system consists of the following equipment as shown in Fig 3.1. Source measurement unit (SMU) is used to measure the device current density-voltage (J-V) curve and parameters such as open-circuit voltage V_{oc} , short-circuit current J_{sc} , fill factor FF and maximum power output P_{max} . In order to obtain more accurate parameters from device under test (DUT), four-point probe measurement method is recommended. The device under test (DUT) is inside the chamber where the temperature can be controlled from the computer monitor. A manual shutter is used to change the measurement condition from light to dark. The light source is set in front of the chamber and connected to the power supply. Both of SMU and chamber are connected to the computer with the program written in LabVIEW which can indicate the information of device's J-V curve, parameters and actual cell temperature inside the chamber. All of the equipment, cell mounting process and J-V-T measurement method will be introduced in the following sections.

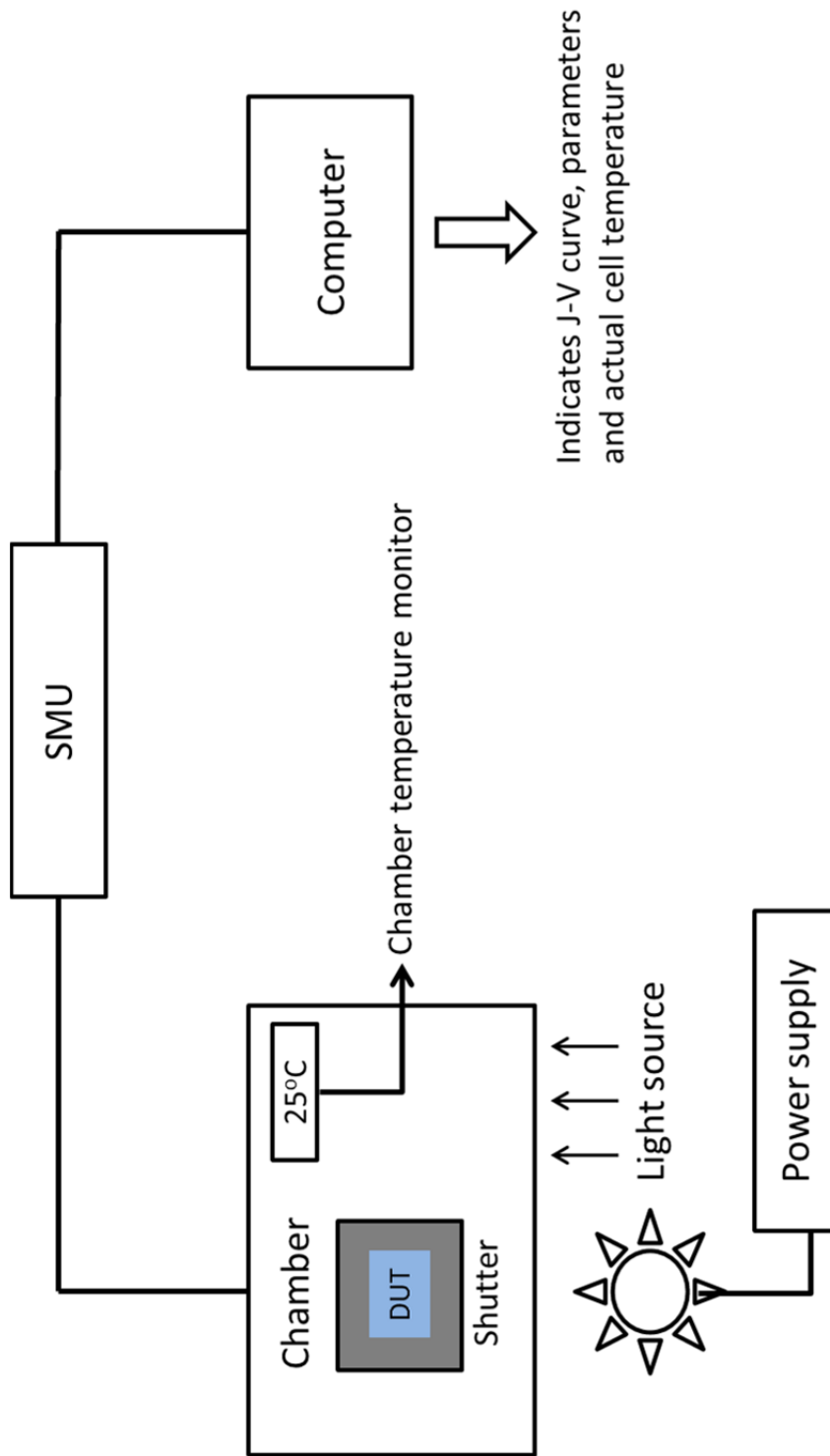


Figure 3.1 Diagram of J-V-T measurement set-up.

3.1 Equipment

3.1.1 Source Measurement Unit (SMU):

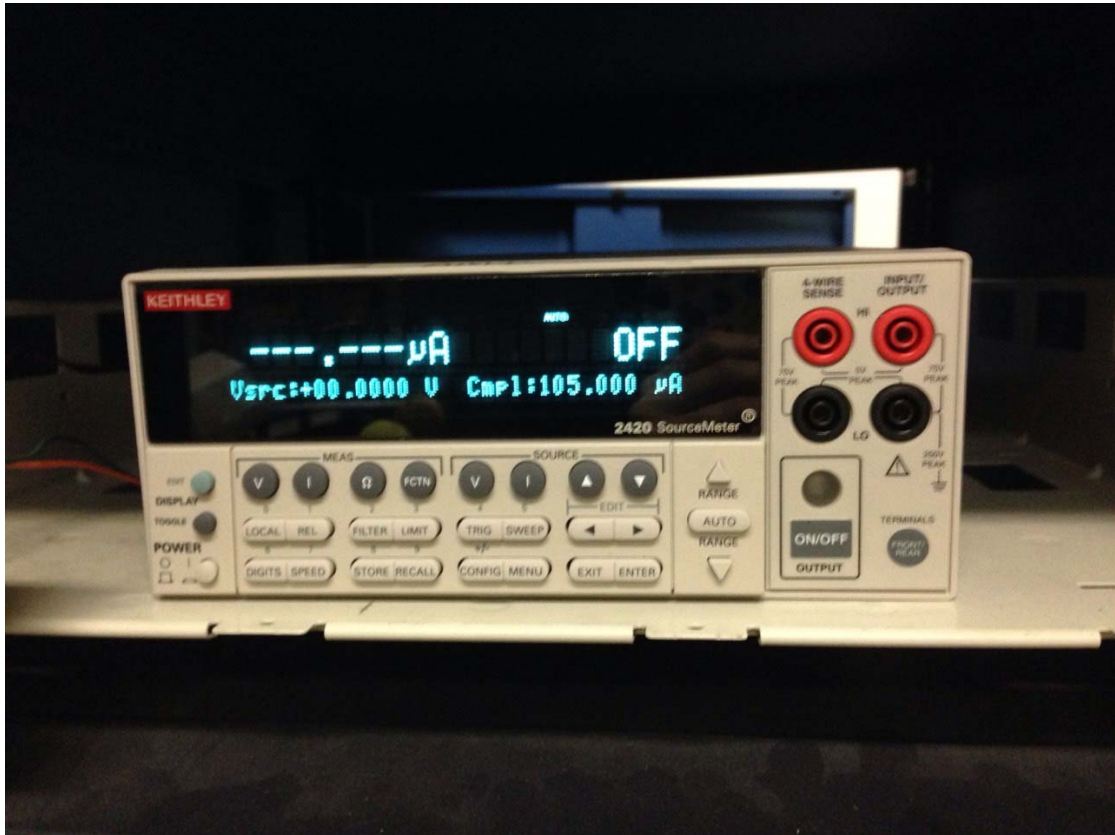


Figure 3.2 Source measurement unit (SMU) for current density-voltage (J-V) measurement.

To obtain four fundamental parameters, open-circuit voltage V_{oc} , short-circuit current density J_{sc} , fill factor FF, and maximum power output P_{max} , from a solar cell, the J-V measurement is required. Fig 3.2 shows the source measurement unit (SMU) used to sweep the source voltage and measure the resulting current simultaneously. Fig 3.3 shows the four-point probe system. Distinguished from the conventional two-

point probe system, four-point probe system can measure voltage accurately without drops since no current will pass through the inner circuit, and then measure the resulting current from DUT. A complete J-V measurement is consisted of four sweeps, light up/down and dark up/down, from the device under test (DUT). The light up voltage sweep range is from -0.3 V to 1.3 V with 300 steps, and the light down voltage sweep is reverse from 1.3 V to -0.3 V. Close the shutter and take the dark up/down sweeps to measure the dark curve.

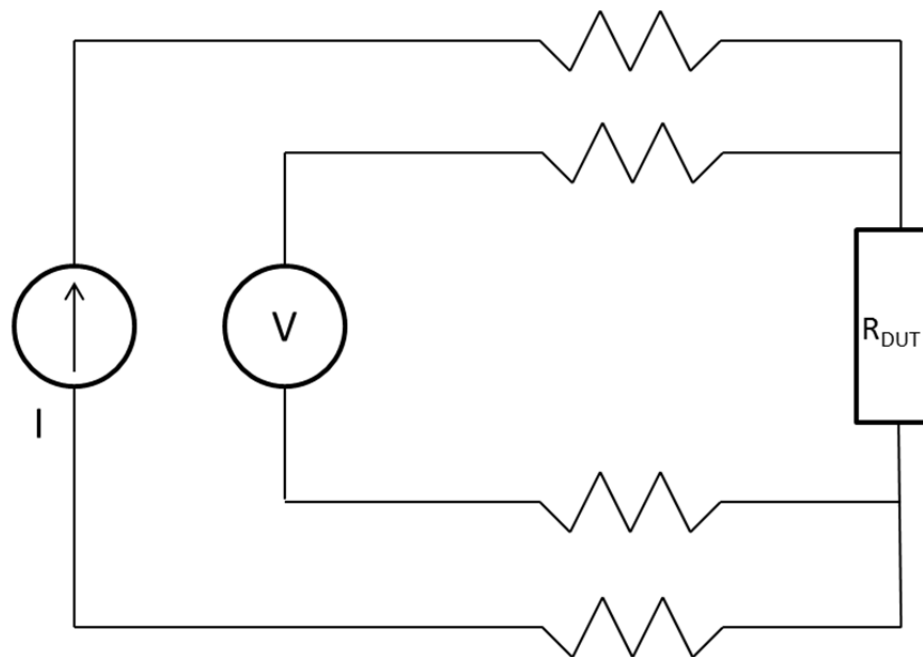


Figure 3.3 The diagram of four-point probe measurement. In this system, only the voltage across the device under test (DUT) is measured. The current flows over the probes, used for sensing, can be negligible. Series resistances exist between source measurement unit (SMU) and device under test (DUT).

3.1.2 Tenney Chamber:

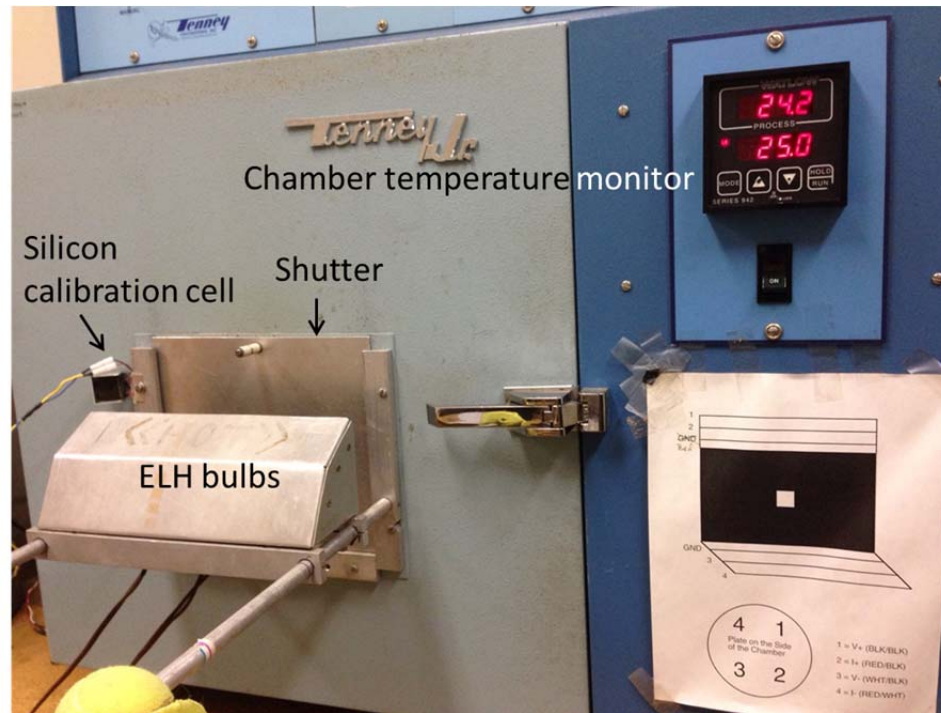


Figure 3.4 Tenney Environmental Chamber. The shutter is covering the window which allows light into the chamber.

This is a Chamber with a heat source and cooling compressor inside, shown in Fig 3.4. The air temperature inside the chamber can be varied from -100°C to 200°C , it can be manually controlled from the monitor. A shutter is used to change the measurement condition from light to dark. There are two ELH bulbs set in front of the chamber's window. The calibration procedure adjusts the ELH bulbs power supply so that the J_{sc} of the DUT matches the J_{sc} measured previously under standard test condition (STC), AM1.5 simulator. The silicon calibration cell is used as a reference cell to see if the light calibration is accurate or not.

3.2 Sample Mount

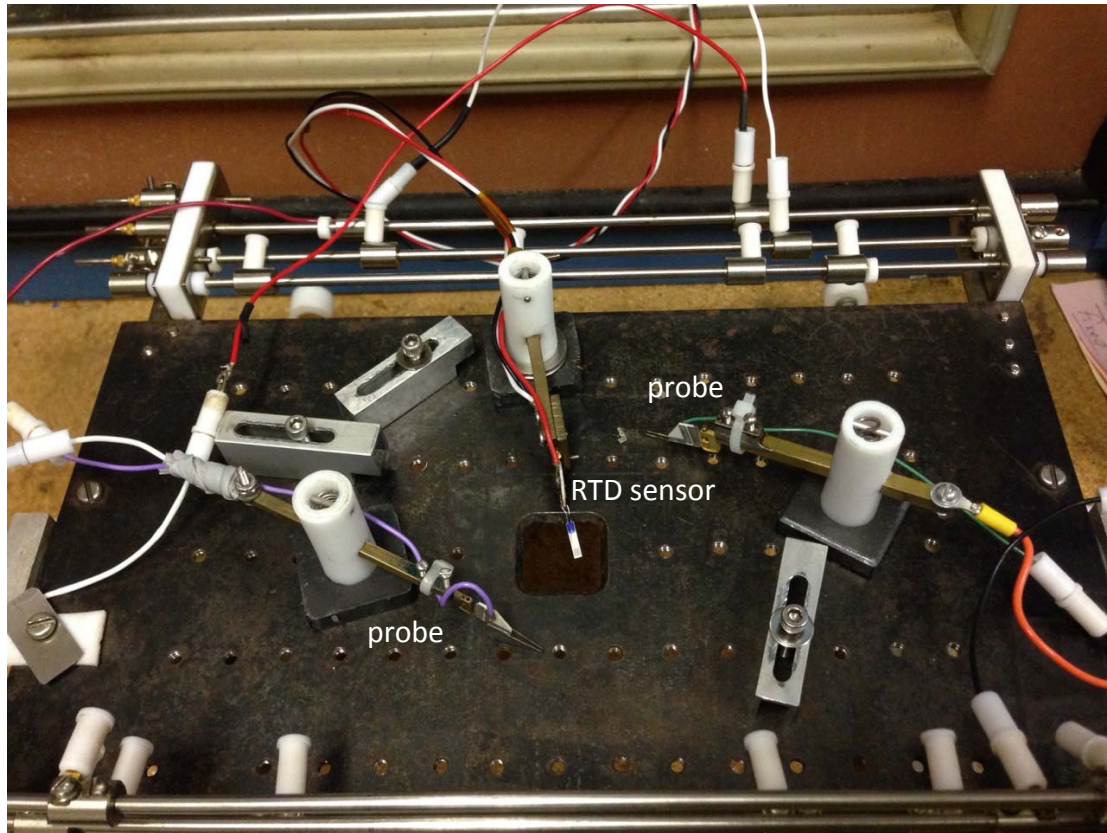


Figure 3.5 Steel plate in the Tenney Chamber used to mount and connect sample.

Inside the Tenney Chamber, there is a steel plate with a square hole in the center, which is shown in Fig 3.5. The plate is electrically isolated from the steel surfaces of the chamber walls which are at ground potential. The plate and all the electrical connection are therefore electrically floating. The procedures to mount and contact the sample are as follows. Put the sample on the center of the hole with the light receiving side facing up, and then use the probes connect to the positive and negative electrodes. Different kinds of cells require different connection to the

electrodes. For ACIGS cells, one probe should be put on the grid bus bar and the other one should be put on the metal back contact. Thus, both of the probes are on the same side of the cell. For IBC cells, the connection should be mounted on the back side of the cell, since the electrodes are interdigitated both on the back surface. Both probes contact through the hole on the plate. For silicon front heterojunction cells, the electrodes are on the different sides, so the probes need to contact both the front and the back (through the hole in the plate). Next, put the resistance temperature detector (RTD) sensor on the sample to measure the cell temperature. The final step is to use the multimeter to check the connectivity. Two things should be considered before starting the J-V-T measurement:

1. While mounting IBC cell and silicon front heterojunction cell, a mask should be put over the cell in case the cell edge has photocurrent collection which will result in measuring the wrong open-circuit voltage and short-circuit current. Also, the mask defines the illuminated area.
2. At low temperature, there might be moisture and frost. To avoid this problem, use Nitrogen purge to remove the room air and most of the moisture in the chamber with 5 liter per minute (lpm) flow for 20 minutes. After that, adjust the flowmeter down to low level (<1 lpm) while doing the J-V-T measurements.

3.3 J-V-T Measurement Method

After mounting the cell, the plate should be connected to SMU. Close the chamber, and turn on SMU equipment.

The following steps show the procedure of the JVT measurement:

1. Make a complete dark up and down sweep to make sure that the cell is connected. If the cell isn't connected well, the curve will be a flat line or very 'noisy'. If there is a problem, reposition the probes and check all the wiring and cable connections.
2. Type in the cell number, area, and other comments.
3. Click the "light calibrate" button, type in the cell area and short-circuit current.
4. Turn on the power supply -which gives power to the ELH bulbs to calibrate light- and match the light intensity to the cell's short-circuit current. Usually in the measurement, the DC volts and amperes values from the power supply are 100 to 125 volts and 5 amperes which can generate 250 to 300W for each ELH bulb.
5. Make a standard current-voltage measurement for both light up/down and dark up/down sweeps at room temperature, 25°C. Compare it to the previous measured JV parameters measured with the standard simulator test system.
6. Nitrogen purge to the chamber. Use 5 lpm for the first beginning 20 minutes, and turn down the flow to less than 1 lpm in the rest of the measurement.
7. Adjust the air temperature inside the chamber on the monitor to 65°C. Then wait about 15 minutes in light for both the air and cell temperature warming up to 65°C.

8. Use four different illumination intensity masks –which are 100%, 70%, 50% and 25%- to make light and dark sweeps at each temperature.
9. Repeat step 8 all the way down to -55°C in decrement of 10°C . The reason for choosing the range 65°C to -55°C is to see the behaviors of different kinds of cells operated at extremely high and low temperature.
10. Last, make a retest at full light intensity and room temperature again. This process allows us to compare the JV testing before thermal cycling to the after thermal cycling, to see whether the cell J-V parameters are the same or not.

Chapter 4

DEVICE CURRENT-VOLTAGE CHARACTERISTIC AND DIODE ANALYSIS

To examine the device properties from different structures, the fundamental method is current-voltage analysis[16, 17] with basic knowledge of solar cell parameters such as open-circuit voltage, short-circuit current, fill factor and cell efficiency. Diode equation analysis[18] is another method to find out diode performance quality with calculation of ideality factor and parasitic resistance in the illuminated diode. Also, the device temperature-dependence behaviors [4, 19, 20] will be interpreted which can indicate the value of saturation current density J_0 and activation energy E_a . All of the methods mentioned above are shown in the following sections.

4.1 Solar Cell J-V Characteristic and Equation Analysis

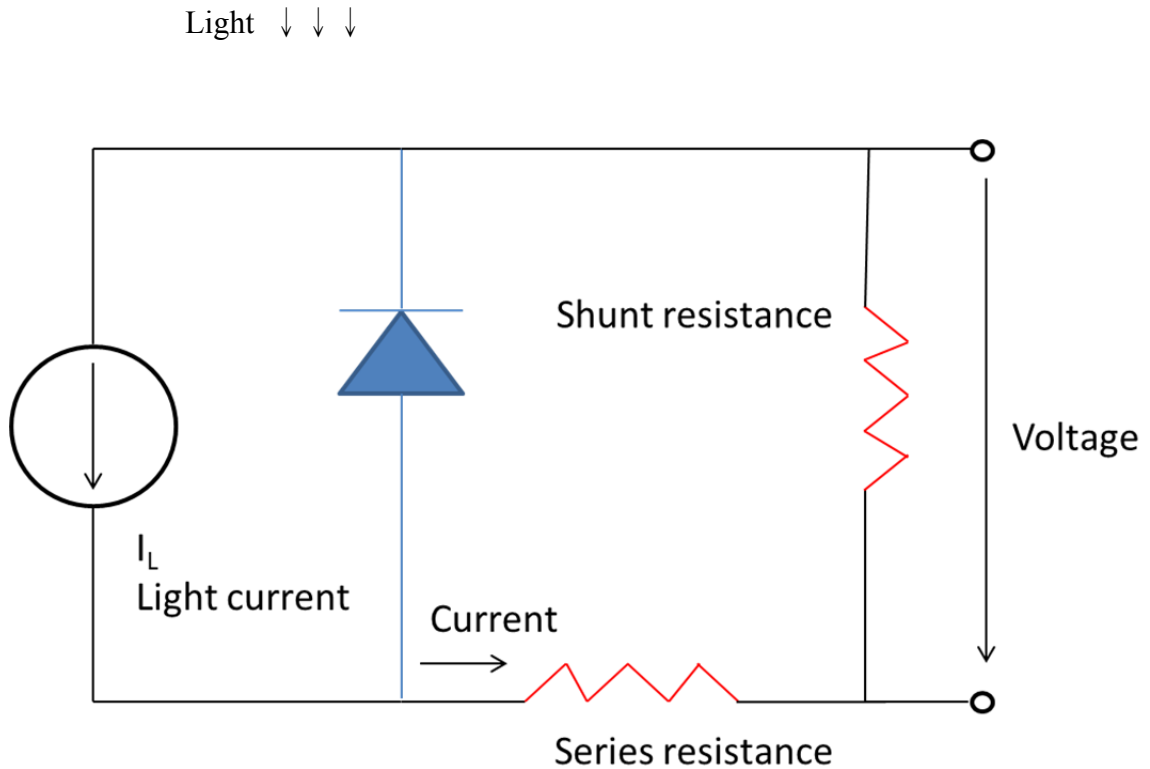


Figure 4.1 Light illuminated current flow through the circuit. The shunt resistance and series resistance can be calculated from diode analysis.

After the solar cell get illuminated, the dark curve will shift down from the first quadrant to the light curve at the forth quadrant, shown in Fig 4.2. The open-circuit voltage V_{oc} occurs when the net current equals zero. The short-circuit current J_{sc} occurs when the voltage across the device equals zero. These two parameters show the maximum voltage and current of a solar cell respectively. Fill factor is a parameter related to the maximum power of a solar cell, which can be written as,

$$FF = \frac{V_{MP} \times J_{MP}}{V_{oc} \times J_{sc}}, \text{ where } V_{MP} \times J_{MP} = P_{max}. P_{max} \text{ is the maximum power output from a}$$

solar cell. Fig 4.3 shows the plot of power output vs. voltage at 25°C. In this case, power is negative since current density is defined negative when exiting the device.

The efficiency is most important metric used to characterize the solar cell performance. It can be defined as, $\eta = \frac{P_{\max}}{P_{in}} = \frac{V_{oc} \times J_{sc} \times FF}{P_{in}}$, where P_{in} represents the input power of light. Under the Standard Test Condition (STC), P_{in} should be 1000W/m² or 100mW/cm².

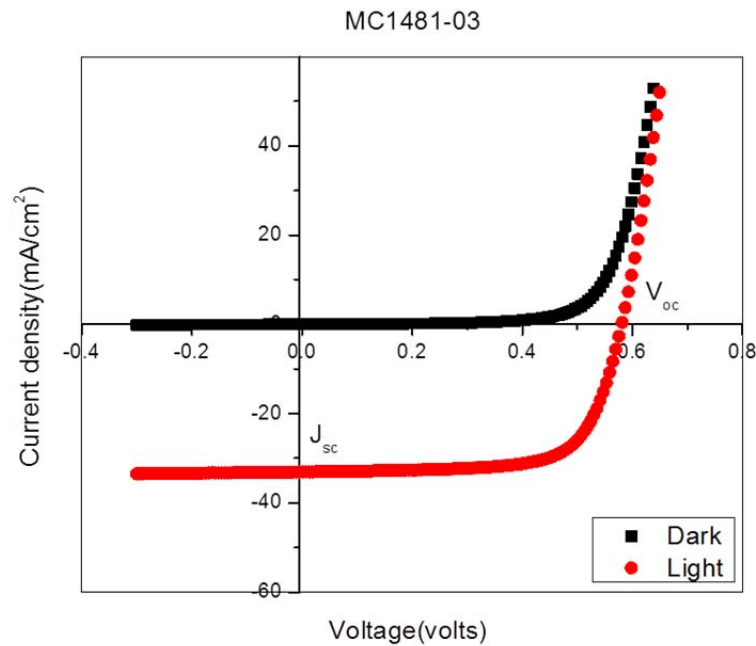


Figure 4.2 The dark and light current-voltage curve at 25°C. V_{oc} and J_{sc} can be easily found when current and voltage equals zero.

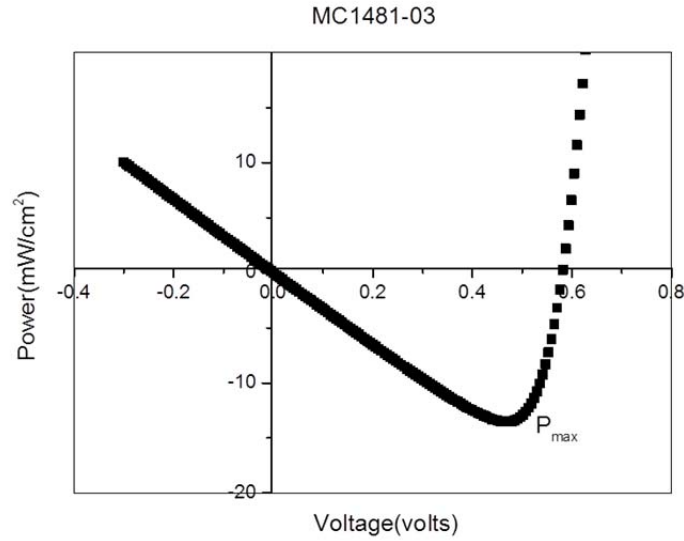


Figure 4.3 The diagram of power vs. voltage at 25°C. P_{\max} indicates the maximum power output from a solar cell.

A solar cell is a p-n junction diode that can absorb light and generate photocurrent. The following J-V equation analysis here is simplified by eliminating the parasitic resistance in Fig 4.1. Ideally, we can view the solar cell as a diode. Once the cell gets illuminated, the standard diode equation shows[16, 17]:

$$J = J_0 \left[\exp\left(\frac{qV}{AkT}\right) - 1 \right] - J_L \quad (4.1.1)$$

A is ideality factor, J_L is light generated current density, and J_0 is saturation current density,

$$J_0 = J_{00} \exp\left[-\frac{E_a}{AkT}\right] \quad (4.1.2)$$

J_0 is also determined by the activation energy of E_a , which in the case of interface recombination without tunneling, E_a will equal to barrier height Φ_b [21].

J_{00} is recombination current density.

Solving equation (4.1.1) for condition of $J=0$, the open-circuit voltage can be written as

$$V_{oc} = \frac{E_a}{q} - \frac{AkT}{q} \ln\left(\frac{J_{00}}{J_L}\right) \quad (4.1.3)$$

Assume in the case of interface recombination without tunneling[21], $E_a=\Phi_b$.

Equation (4.1.3) can also be written as

$$V_{oc} = \frac{\Phi_b}{q} - \frac{AkT}{q} \ln\left(\frac{J_{00}}{J_L}\right) \quad (4.1.4)$$

From equation (4.1.3), there are two important dependencies can be seen[19]:

1. The open-circuit voltage V_{oc} is dependent on temperature. The linearity gives a negative temperature coefficient from the slope and activation energy E_a from the intercept, as shown in Fig 4.4. The data is from FHJ solar cell. The slope gives a typical temperature coefficient of $-0.002V/^{\circ}C$ and the intercept is 1.19 which is similar to the value of the silicon bandgap 1.17 eV at 0K[22].
2. V_{oc} varies logarithmically linearly with light intensity since J_L is proportional to light intensity. Fig 4.5 shows the data from IBC solar cell. The intercept in the plot indicates $\log J_0$.

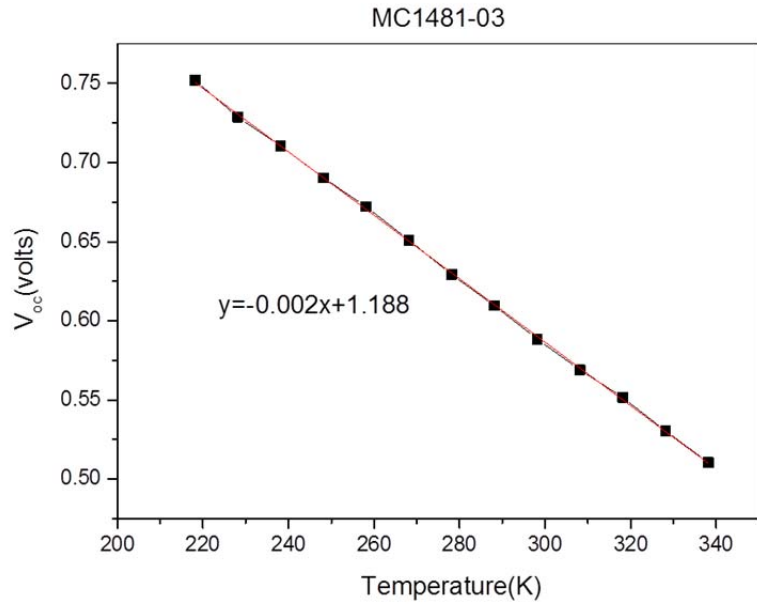


Figure 4.4 Example of V_{oc} vs. temperature at full light intensity, 25°C.

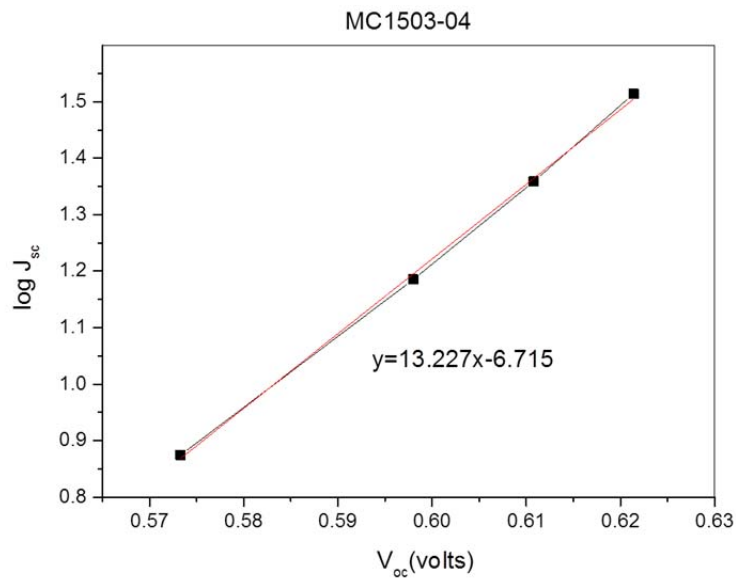


Figure 4.5 Example of $\log J_{sc}$ vs V_{oc} at 25°C, four illumination intensities.

To obtain $\log J_0$, calculate the logarithm of J_{sc} from four different light intensities at each temperature. Make a plot of $\log J_{sc}$ vs. V_{oc} , as shown in Fig 4.5, and then use the linear fit to find the slope and intercept. From equation (4.1.3), the intercept will be $\log J_0$ and ideality factor A can be calculated from $A = \frac{1}{slope \times kT / q \times 2.3}$. In Fig 4.5, the values of $\log J_0$ is -6.715 and ideality factor A is 1.264.

After fitting for all the temperature as Fig 4.6 shows, activation energy E_a can be obtained from linear fit of the slope. The value of activation energy shown in Fig 4.6 is 1.23 eV. Compare it with the value extrapolated at $T=0K$ (1.19 eV) in Fig 4.4, the two values are very close.

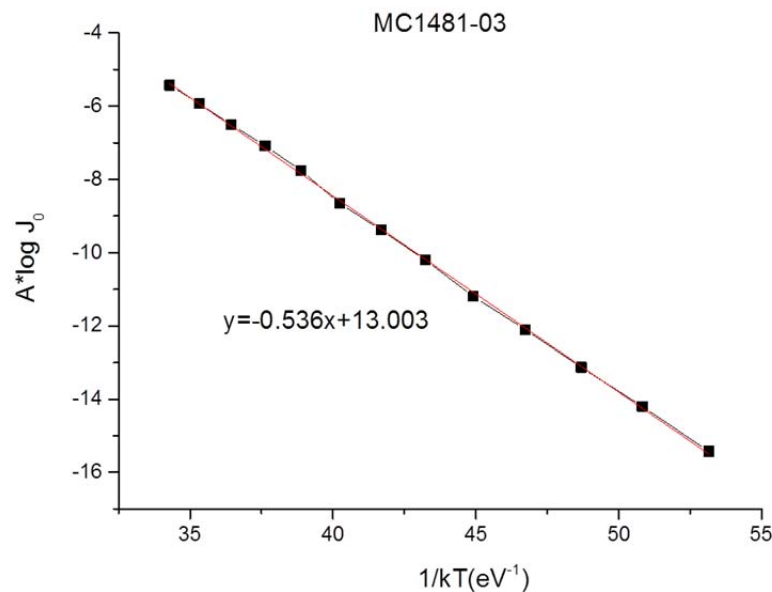


Figure 4.6 The plot shows the linearity between $A \cdot \log J_0$ and $1/kT$. Activation energy E_a can be calculated from the slope. $E_a = slope \times 2.3$

4.2 Diode Analysis

The method discussed in Section 4.1 did not consider the resistance in the circuit since its effect on J-V parameters is negligible at V_{oc} or J_{sc} . Another method[18] to analyze the J-V characteristic is to consider the resistances inside the circuit as shown in Fig 4.1. Consequently, the general diode current equation can be interpreted as

$$J = J_0 \exp\left[\frac{q}{AkT}(V - RJ)\right] + GV - J_L \quad (4.2.1)$$

R is series resistance, G is shunt conductance, A is ideality factor and J_0 is diode current, which can be written as

$$J_0 = J_{00} \exp\left(-\frac{\Phi_b}{AkT}\right) \quad (4.2.2)$$

Φ_b is barrier height and J_{00} is recombination current density which is determined by recombination effect.

In order to obtain the ideal diode behavior without shunt and series resistance, first of all, take the differential of $\frac{dJ}{dV}$ from equation (4.2.1), and ignore the constant terms. The linear slope will be shunt resistance G. In general, it is a small value that exists in the diode. Typically, only cells with very low shunt resistance are used for J-V-T measurement, or $G < 3\text{mS}/\text{sqcm}$.

Next, take the differential of $\frac{dV}{dJ}$ from equation (4.2.1), which turns out to be $\frac{dV}{dJ} = R + \frac{AkT}{q}(J + J_L)^{-1}$. By getting the linear fit from the plot, the intercept R and the ideality factor A can be obtained. When applied to a dark J-V curve, $J_L=0$.

Once the values of the parasitic elements shunt resistance G and series resistance R are obtained, a semi-logarithmic plot for $(J+J_{sc}-GV)$ vs. $(V-RJ)$ can be

constructed which is correct for the parasitic losses. It represents only the effect of junction recombination due to the diode. Ideally it should allow fitting to the linear region of at least 2 orders of magnitudes. However, under some V or T ranges, the result will not be linear indicating other losses are dominating the J-V behavior. Most commonly, these are blocking contacts, voltage dependent collection, or non-linear intensity dependence. However, if a linear fit is possible, the intercept of the plot is J_0 and by calculating the slope $\frac{q}{AkT}$, the ideality factor A can be obtained as well. Compare it to the ideality factor A from $\frac{dV}{dJ}$, these two values should be very close.

Fig 4.7 shows the case of normal diode analysis at room temperature. Fig 4.8 and Fig 4.9 show the case of diode analysis for anomaly S-shape J-V curve at low temperature.

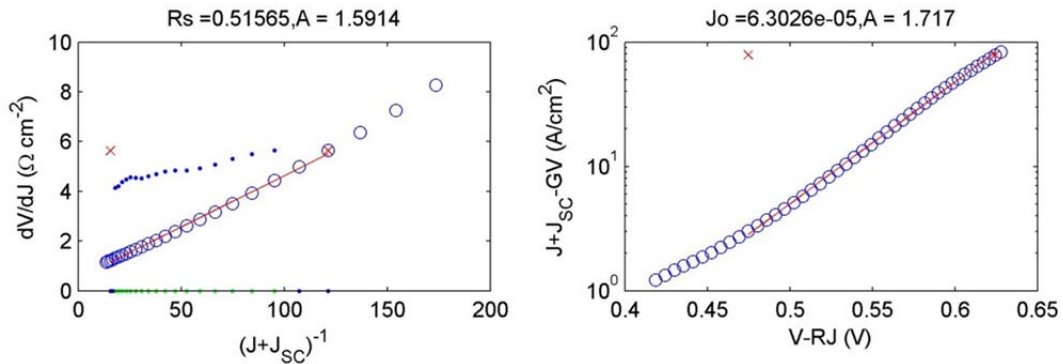


Figure 4.7 A typical diode analysis at 25°C, full light intensity. The left-hand side plot shows the linear fit of dV/dJ , and the right-hand side plot shows the linear fit of semi-logarithmic. The two red X in each plot indicates the fitting range in abscissa. The little blue dots in the left-hand side plot show the slope of dV/dJ .

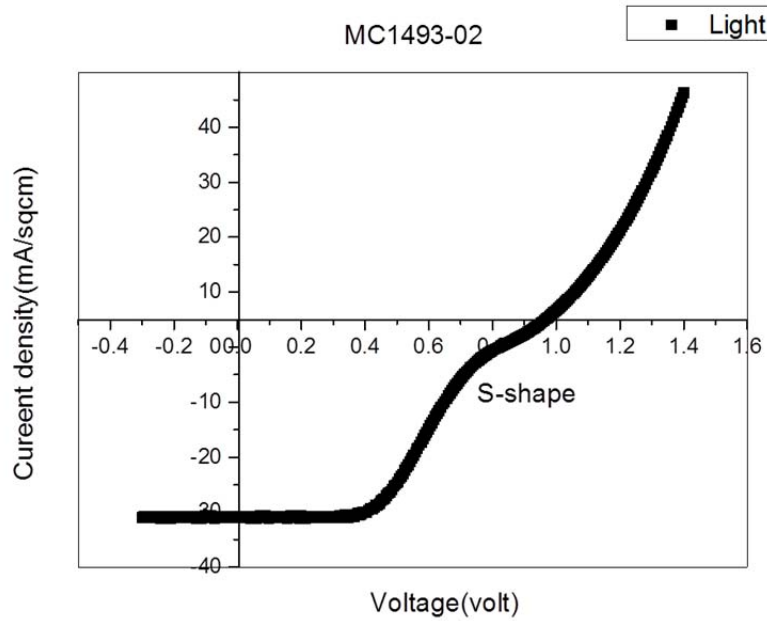


Figure 4.8 S-shape J-V curve at -55°C . If it occurs in light J-V curve, it is based on a barrier for photo current. The anomaly will get worse as the temperature get lower.

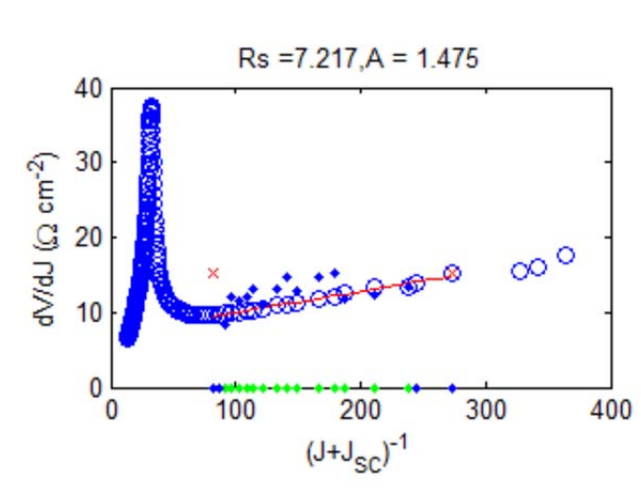


Figure 4.9 The diagram shows the diode analysis for the case of S-shape J-V curve at low temperature. There is a peak of dV/dJ which will decrease the linearity and be difficult to get accurate ideality factor A and J_0 .

Chapter 5

RESULTS AND DISCUSSION FOR SILICON FRONT HETEROJUNCTION AND IBC SOLAR CELLS

The Si cells measured and analyzed in this thesis were fabricated in the Institute of Energy Conversion (IEC). From comparing different types of silicon FHJ and IBC solar cells, effect of temperature on J-V parameters and s-shape J-V curve will be included in this chapter.

5.1 Results of J-V-T Measurements

Table 5.1 shows the initial data for silicon front heterojunction solar cells. Device MC1469-02 (with i-layer) obtains the highest J_{sc} and efficiency. Device MC1481-03 (without i-layer) shows the lowest V_{oc} and efficiency. Device MC1493-02 (with n-strips on the back rather than blanket n region) has the highest V_{oc} but the lowest J_{sc} and fill factor. Initial data for IBC solar cells is shown in Table 5.2. The primary difference between them was the front passivation stack layers especially the layers in direct contact with the Si wafer. All of the IBC cells had a-SiC/a-SiN as the outer layers. Device MC1497-09 (with only n-type a-Si passivation layer) shows the lowest V_{oc} , J_{sc} and efficiency. Device MC1483-06 (without n+ diffusion) shows the similar data as MC1497-09, but obtains almost the same high J_{sc} compared to the two devices with n+ diffusion. MC1492-02 has the highest V_{oc} , J_{sc} and efficiency of all.

Table 5.1 Initial data for silicon front heterojunction solar cells measured from standard simulator test system. Illumination mask area was 2.5 cm².

	MC1469-02	MC1481-03	MC1493-02
Voc(V)	0.679	0.594	0.705
Jsc(mA/cm2)	33.9	33.3	32.8
FF(%)	70	72.6	66.4
Eff(%)	16.1	14.4	15.4
Structure	with i-layer	without i-layer	n-strips on the back

Table 5.2 Initial data for IBC solar cells measured from standard simulator test system. Illumination area was 1.66 cm².

	MC1497-09	MC1503-04	MC1483-06	MC1483-10	MC1492-02
Voc(V)	0.591	0.625	0.596	0.659	0.68
Jsc(mA/cm2)	30.2	34.8	38.4	38.5	38.9
FF(%)	73	73.6	71	74.7	74.7
Eff(%)	13	16	16.3	19	19.8
Structure	n a-Si	i a-Si/n a-Si	no n+ diff	n+ diff	n+ diff

J-V was measured for temperature varying from 65°C to -55°C to see and compare the influence due to temperature in each different fabrication process device.

5.1.1 Silicon Front Heterojunction Solar Cells

Fig 5.1 shows that V_{oc} for all three devices has a linear negative dependence on temperature. Device MC1481-03 (without i-layer) obtains the lowest values of V_{oc} . The other two devices almost obtain the same values of V_{oc} over the entire range of temperature considered.

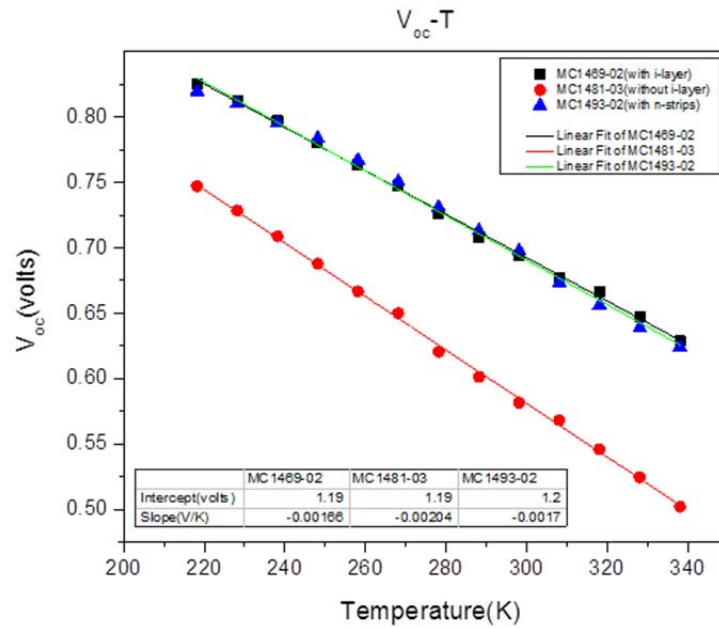


Figure 5.1 Diagram of open-circuit voltage V_{oc} vs. temperature and table shows intercept at $T=0K$ and slope from linear fitting. The temperature coefficients showing later are fitting from 270K to 340K.

Fig 5.2 shows the slight temperature effect on short-circuit current J_{sc} . All three devices have small positive temperature dependence. Device MC1481-03 (without i-layer) shows an increment at $5^{\circ}C$ to $-5^{\circ}C$. This might result from some fluctuations in the ELH lamp power supply. MC1493-02 obtains a small slope of $J_{sc}/^{\circ}C$. The temperature coefficients comparison will be included in Table 5.3.

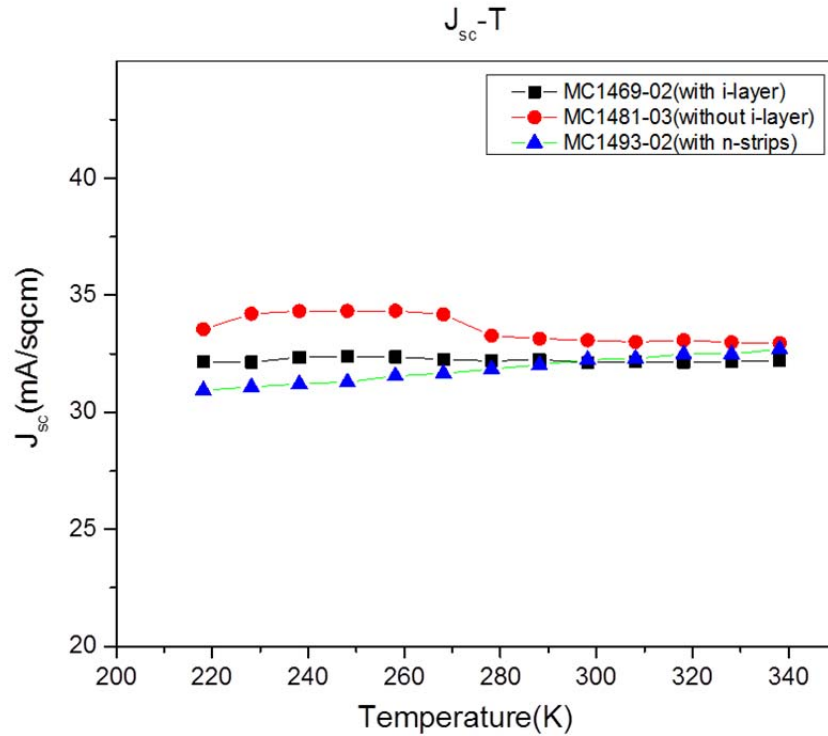


Figure 5.2 Short-circuit current J_{sc} vs. temperature.

Fig 5.3 shows the fill factor and maximum power output variation with temperature. In general, the shape of the FF and P_{max} curve are almost the same. It can be extrapolated that temperature dependence of the maximum power output is determined by fill factor explicitly. Device MC1481-03 (without i-layer) shows the lowest maximum power output at high temperatures but the highest maximum power output at temperatures below -25°C . The other two devices show the same trend of curve, but MC1469-02 (with i-layer) obtains higher maximum power output than the device MC1493-02 (with n-strips on the back).

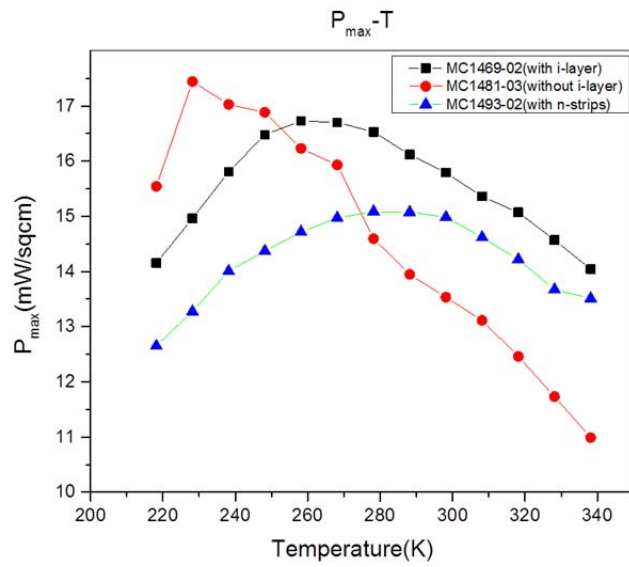
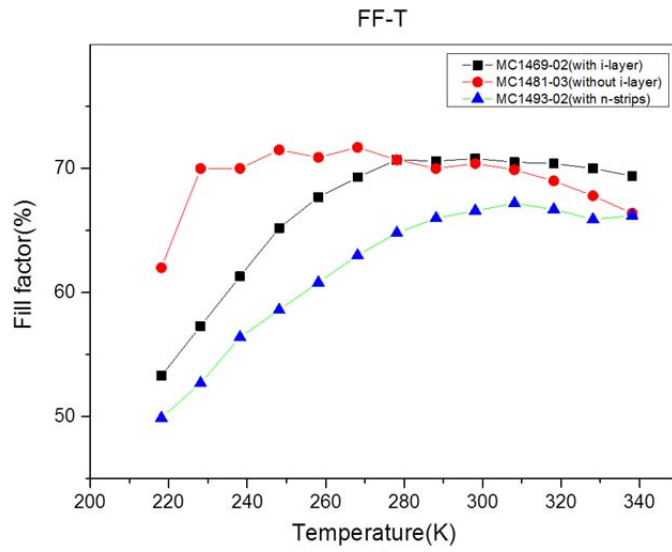


Figure 5.3 Fill factor vs. temperature (top) and maximum power output vs. temperature (bottom).

Table 5.3 shows the temperature coefficients of front heterojunction solar cells compared with typical crystalline silicon solar cell with diffused p-n junctions[23] and commercial HIT structure solar cell[24]. The linear fitting range for temperature coefficients is from 270K to 340K due to the change in slope at lower temperatures. Generally speaking, HIT solar cells show better temperature coefficients than typical c-Si solar cells with diffused p-n junctions due to less surface recombination and higher V_{oc} [4, 25]. The correlation between temperature coefficient of maximum power output and V_{oc} is shown in Fig 5.4. Therefore, devices with higher V_{oc} show lower temperature dependence of power output[25]. Table 5.3 also shows the activation energy of three FHJ devices calculated from the slope of $A \cdot \log J_0$ vs. $1/kT$ (see section 4.1). Activation energy is dominated by the recombination mechanism such as Shockley-Read-Hall (SHR) recombination and interface recombination[20]. Compared to the intercept extrapolated from temperature dependence of V_{oc} (at $T=0K$), the two values should be really close (difference less than 0.1). Device MC1481-03 (without i-layer) obtains the highest activation energy.

Table 5.3 Temperature coefficients and activation energy.

	MC1469-02	MC1481-03	MC1493-02	General Si solar cell	Sanyo
Temperature coefficient of $V_{oc}(V/^{\circ}C)$	-0.0017	-0.002	-0.0018	-0.0022	-0.0018
Temperature coefficient of $J_{sc}(mA/^{\circ}C)$	-0.001	-0.004	0.015	0.6	0.024
Temperature coefficient of $P_{max}(/^{\circ}C)$	-0.004	-0.0059	-0.0035	-0.0045	-0.003
Intercept of V_{oc} vs. T (at $T=0$)	1.206	1.186	1.236		
Activation energy(eV)*	1.227	1.233	1.203		
Fabrication type	with i-layer	without i-layer	n-strips on the back	Homojunction	HIT
*Calculated from $A \cdot \log J_0$ vs. $1/kT$					

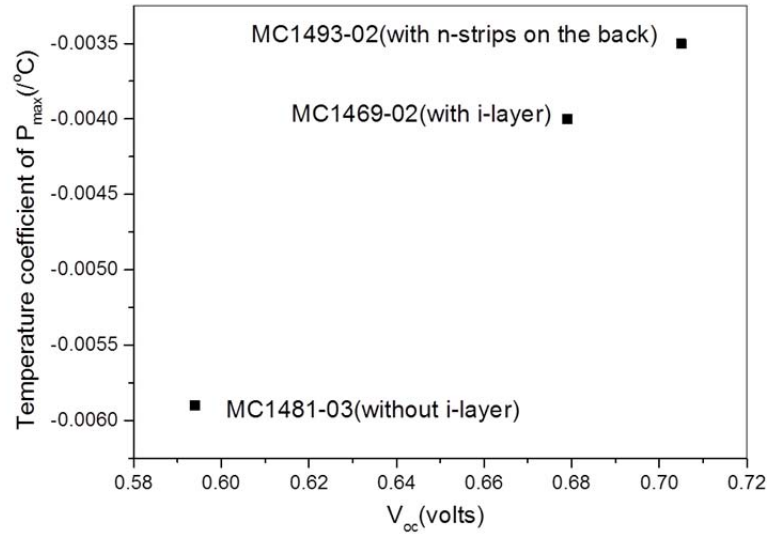


Figure 5.4 The correlation between temperature coefficient of P_{max} and V_{oc} .

5.1.2 IBC Solar Cells

Fig 5.5 shows the temperature dependence of V_{oc} for all the IBC devices. The devices with n+ diffusion, MC1483-10 and MC1492-02, show good linearity and high open-circuit voltage over the entire temperature range. Device MC1483-06 (without n+ diffusion) has the lowest open-circuit voltage while the temperature is below 25°C. Devices with different passivation layers, MC1503-04 and MC1497-09, indicate that the one without intrinsic a-Si:H layer have the lowest open-circuit voltage at temperature above 25°C. On the other hand, devices MC1483-06, MC1492-02 and MC1503-04 show that, the V_{oc} start to saturate as the temperature is near 200K. Fig 5.6 shows the saturation under different light intensities for device MC1503-04. This effect is due to the V_{oc} becoming nearly independent of temperature and recombination at temperature below 200K[26]. From equation (4.1.4),

$$V_{oc} = \frac{\Phi_b}{q} - \frac{AkT}{q} \ln\left(\frac{J_{00}}{J_L}\right), \text{ when } V_{oc} \text{ is independent of temperature and recombination}$$

(i.e. the second term), the saturation value will be close to the built-in voltage Φ_b . In this case the V_{oc} is determined by the electron affinity and Fermi levels of the contacts.

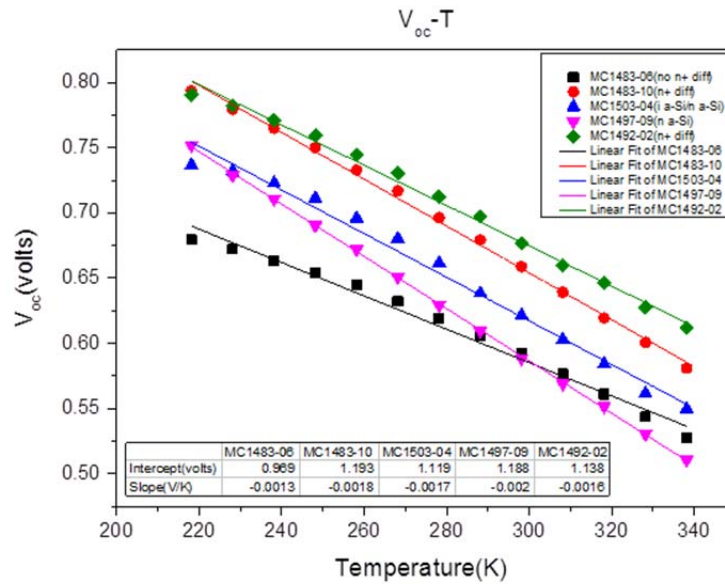


Figure 5.5 V_{oc} vs. temperature and table shows the intercept at $T=0K$ and slope from the linear fit for IBC solar cells. The temperature coefficients showing later are fitting from 270K to 340K.

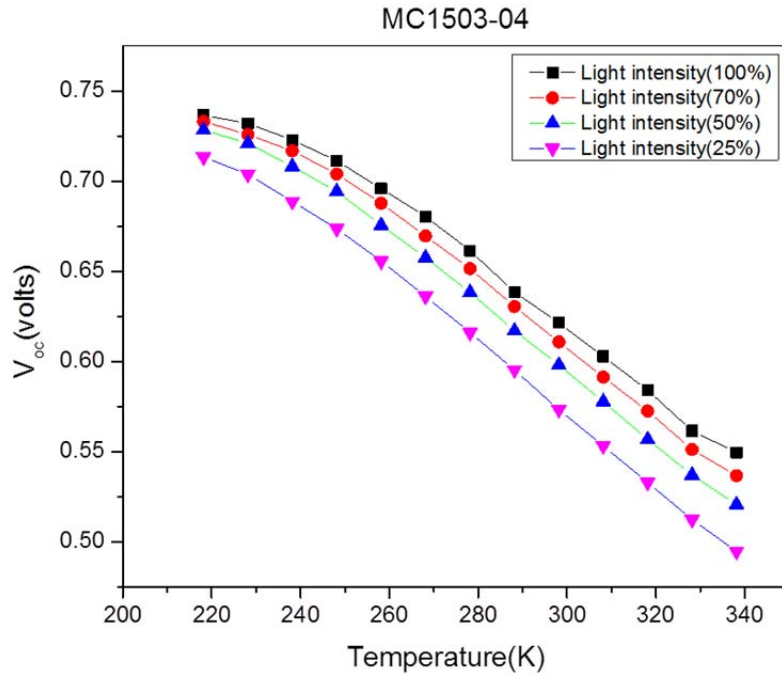


Figure 5.6 Diagram of V_{oc} vs. temperature for device MC1503-04 which shows the voltage saturation at low temperature.

In Fig 5.7, devices MC1483-06 and MC1483-10 (without and with n+ diffusion) have a J_{sc} which is independent of temperature. However, for other three devices MC1503-04, MC1497-09 and MC1492-02, J_{sc} has a small positive linear slope, indicating the temperature dependence of J_{sc} for IBC cells is not a universal trait but depends on the device structure and processing. In the case of front heterojunction cells, the devices show less dependent of temperature than the case of IBC cells.

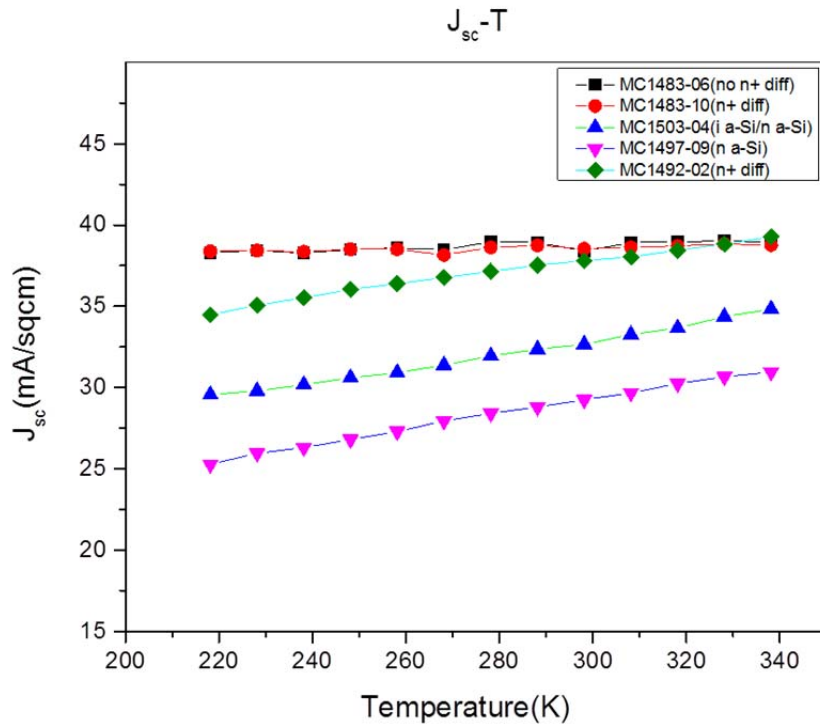


Figure 5.7 J_{sc} vs. temperature for IBC solar cells.

Fig 5.8 shows the plots of fill factor vs. temperature and maximum power output vs. temperature. There is a general correlation between fill factor and maximum power output. All devices show an increase in maximum power as temperature decreases, but devices MC1503-04 and MC1492-02 then begin to decrease at some low temperature which is caused by series resistance (will be discussed in section 5.3.2). Devices MC1483-06 and MC1483-10 show the increment of P_{max} as temperature getting lower. Comparing the two devices both with n+ diffusion, MC1492-02 has highest P_{max} at temperatures above 25°C, MC1483-10 shows highest P_{max} at temperatures below 25°C. It can be extrapolated that device MC1483-10 has

better cell performance at low temperature. Nevertheless, MC1497-09 (with n a-Si passivation) obtains second highest fill factor but the lowest P_{\max} at all temperatures and, especially at high temperatures may due to the lowest V_{oc} and J_{sc} as shown in Table 5.2. As a result, cell with n+ diffusion obtains good performance and efficiency varied with temperature.

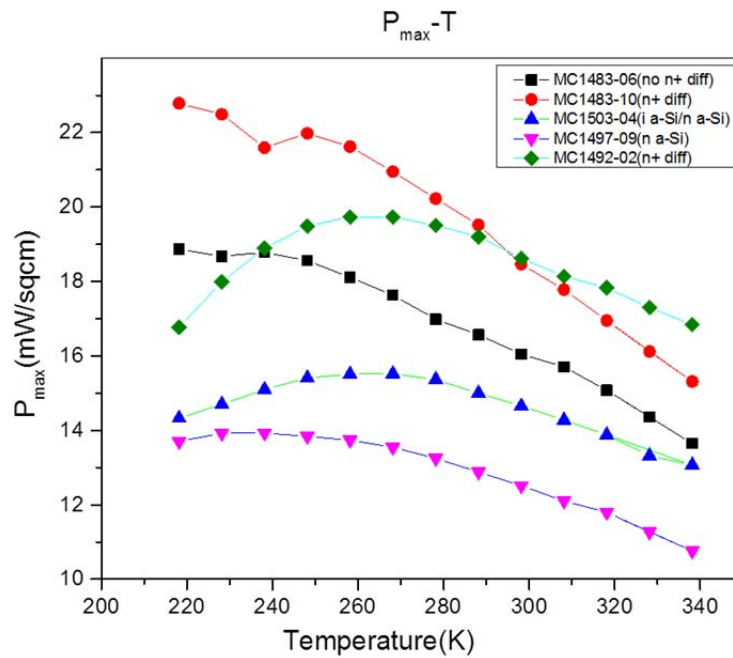
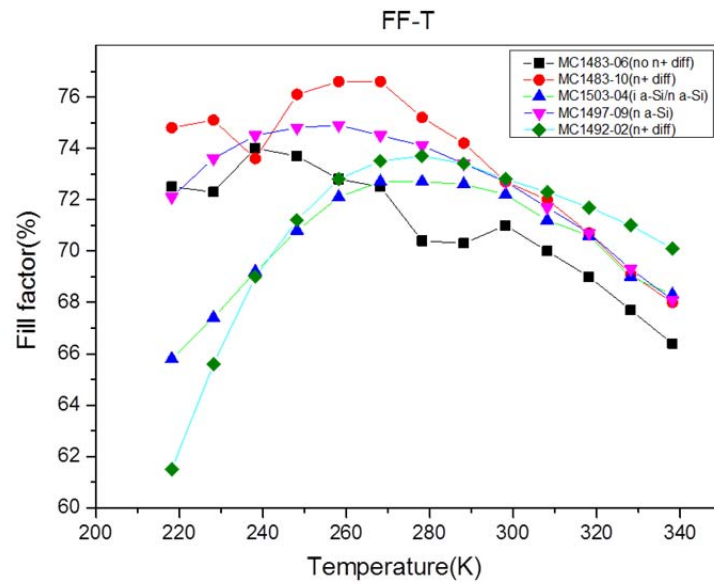


Figure 5.8 Plots of FF vs. temperature (top) and P_{max} vs. temperature (bottom) for IBC cells.

Table 5.4 shows the temperature coefficients and activation energy for IBC solar cells. The linear fitting range for temperature coefficients is from 270K to 340K. Device MC1483-06 (no n+ diffusion) was the only IBC cell with 30 seconds HNA etched back (all others had 20 seconds) and shows the lowest temperature coefficient of V_{oc} and activation energy. The other devices show an E_a with the range between 1.18eV to 1.22eV extrapolated from V_{oc} vs. temperature at $T=0K$. The value of bandgap (E_g) for silicon at 0K is around 1.17 eV[22]. When $E_a=E_g$, this implies the absorber layer is dominated by Shockley-Read-Hall recombination. But activation energy E_a is not always equal to absorber bandgap E_g if other recombination mechanisms dominate the device, such as an interface recombination mechanism[20]. The last column shown in Table 5.4 is Sunpower IBC cell's temperature coefficient compared to the IBC cells in this work[27]. MC1483-06 and MC1483-10 show their temperature coefficient of P_{max} relative higher than the general silicon solar cell whose temperature coefficient of P_{max} is $-0.0045/^{\circ}C$. Fig 5.9 shows the plot of temperature coefficient of P_{max} vs. V_{oc} . In contrast with front heterojunction cells, there is no significant correlation between temperature coefficient of P_{max} and V_{oc} . Devices MC1483-10 and MC1492-02, fabricated with the same front surface field n+ diffusion process, MC1492-02 obtains a better temperature coefficient of P_{max} than MC1483-10 which may be contributed to the different polishing process on the back surface.

Table 5.4 Temperature coefficients and activation energy.

	MC1497-09	MC1503-04	MC1483-06	MC1483-10	MC1492-02	Sunpower
Temperature coefficient of Voc(V/°C)	-0.002	-0.0019	-0.0015	-0.0019	-0.0017	-0.0017
Temperature coefficient of Jsc(mA/°C)	0.048	0.044	0.006	0.004	0.038	0.036
Temperature coefficient of Pmax(/°C)	-0.0042	-0.004	-0.0058	-0.0081	-0.0046	-0.003
Intercept of Voc vs. T (at T=0)	1.188	1.19	1.012	1.222	1.18	
Activation energy(eV)*	1.139	1.18	0.938	1.247	1.208	
Front passivation structure	n a-Si	i a-Si/n a-Si	no n+ diff	n+ diff	n+ diff	
HNA etched back	20 sec	20 sec	30 sec	20 sec	20 sec	
*Calculated from $A \cdot \log J_0$ vs. $1/kT$						

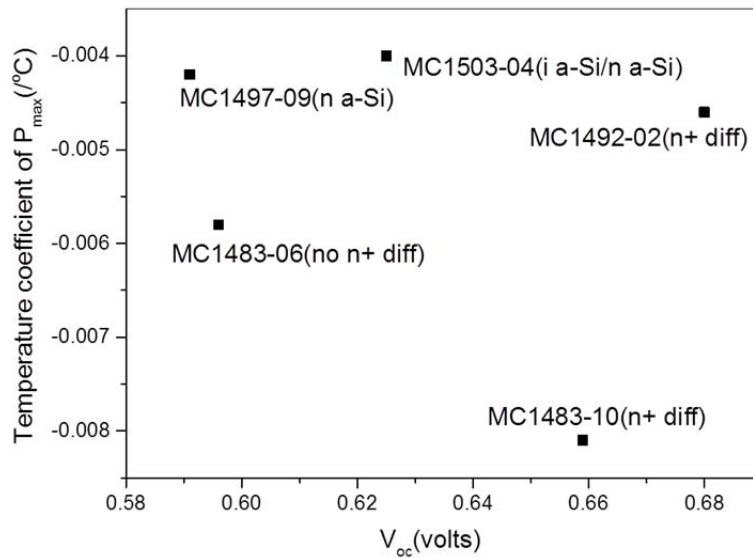


Figure 5.9 Temperature coefficient of P_{max} vs. V_{oc}.

5.2 Ideality Factor A

The ideality factor A, also called- the diode ‘quality’ factor, represents different types of recombination in the diode. It can be determined by standard diode equation (4.1.1). The ideality factor here is calculated using the log J_{sc} vs. V_{oc} at different light intensity according to equation (4.1.3) (see section 4.1). The range of

the ideality factor is supposed to be between 1 and 2 for a typical solar cell where $A=1$ represents band-to band recombination and $A=2$ represents pure Shockley-Read-Hall (SRH) recombination as in the depletion region. In general, higher efficiency devices have A closer to 1. Fig 5.10 shows the plot of silicon front heterojunction solar cells' ideality factor vs. temperature. It ranges between 1.0 and 1.5, and is generally temperature dependent, as expected, indicating nearly ideal behavior and mostly band-to-band recombination, or a good diode quality. Device MC1469-02 (with i-layer) obtains the lowest ideality factor and highest efficiency compared to other two silicon front heterojunction solar cells.

As for IBC solar cells, the temperature effect on ideality factor is shown in Fig 5.11. It can be observed that most of the devices are operated with the ideality range between 1.0 and 1.5. Several devices show A decrease with decreasing temperature, such as MC1483-06 (without n^+ diffusion), MC1503-04 (i a-Si/n a-Si) and MC1492-02 (n^+ diffusion). It might be due to the V_{oc} is independent of light intensity and saturates at low temperature, so the slope of $\log J_{sc}$ vs. V_{oc} is becoming meaningless.

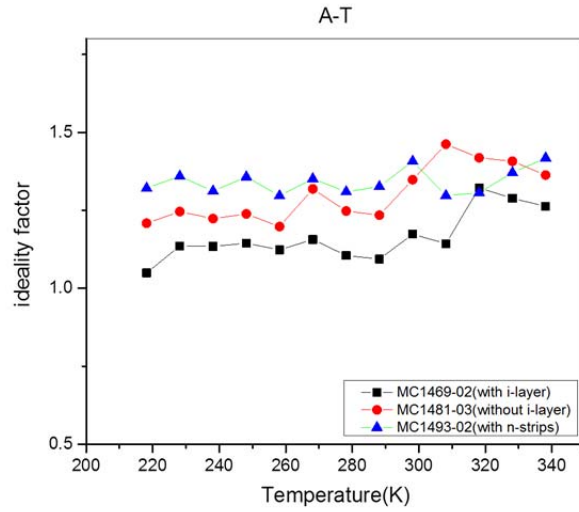


Figure 5.10 Ideality factor vs. temperature for silicon front heterojunction solar cells.

The value n was calculated from equation $A = \frac{1}{slope \times kT / q \times 2.3}$ (see section 4.1).

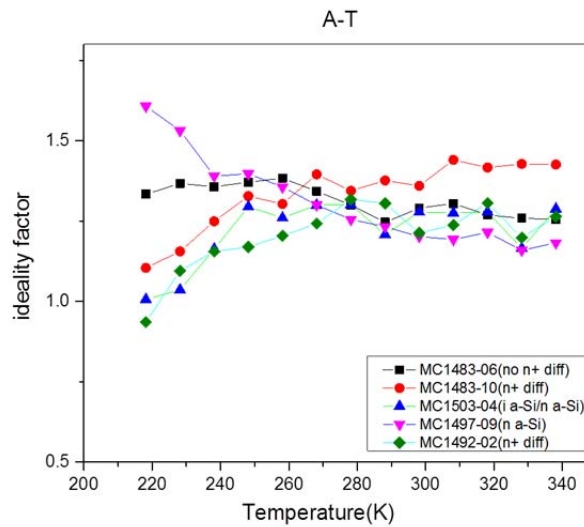


Figure 5.11 Ideality factor vs. temperature for IBC solar cells. The value n was

calculated from equation $A = \frac{1}{slope \times kT / q \times 2.3}$ (see section 4.1).

5.3 Low Temperature Performance and Interpretation of Anomalous J-V Curve

The s-shape J-V curve formation interpreted in Chapter 4 usually occurs at low temperatures. In this section, the appearance of this anomaly in front heterojunction and IBC silicon solar cells will be discussed separately.

5.3.1 Silicon Front Heterojunction Solar Cells

Fig 5.12 and Fig 5.13 show the silicon front heterojunction solar cells' J-V curves at 25°C and -55°C. Devices MC1469-02 and MC1493-02 obtain similar J-V curve at 25°C and -55°C. Both of them show the s-shape J-V curve at low temperature which results from a barrier to minority carrier collection (the photocurrent). The s-shape J-V curve is well known to decrease the cell's fill factor and efficiency[13]. Device MC1481-03 has no s-shape J-V curve but still has some influence from series resistance. Fig 5.14 shows the diagram indicating that the higher the series resistance is, the lower the fill factor is, especially at low temperature. With the decreased fill factor in the device, the power output will decrease as well. Consequently, there are two significant differences to compare at lower temperature: the increase in series resistance R_s (from the intercept of dV/dJ mentioned in Section 4.2) and the height of the peak at low values of dV/dJ . Device MC1481-03 (without i-layer) has much less series resistance at -55°C and has a much smaller peak compared to other two devices. The higher intercept and significant peak in dV/dJ in devices MC1469-02 and MC1493-02 suggest a larger barrier and relative high series resistance at -55°C.

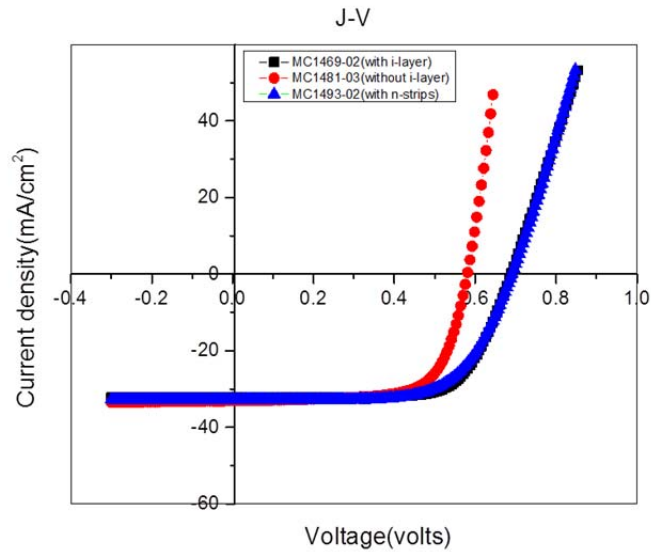


Figure 5.12 J-V curve for silicon front heterojunction solar cells measured at 25°C and full light intensity.

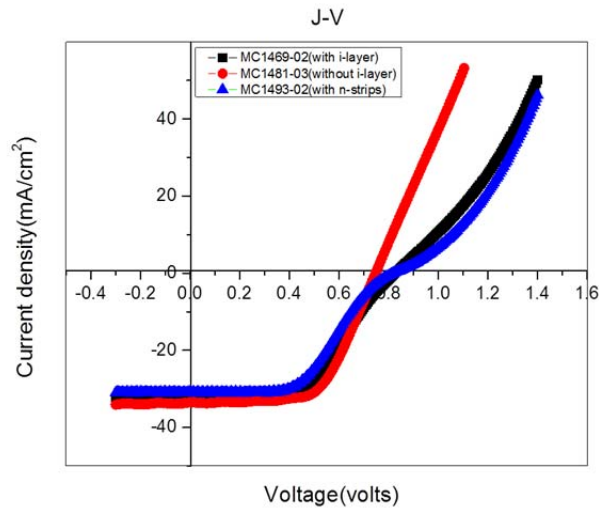


Figure 5.13 J-V curve for silicon front heterojunction solar cells measured at -55°C and full light intensity. The FF values are: MC1469-02: 53.3%, MC1481-03: 62%, and MC1493-02: 49.9%.

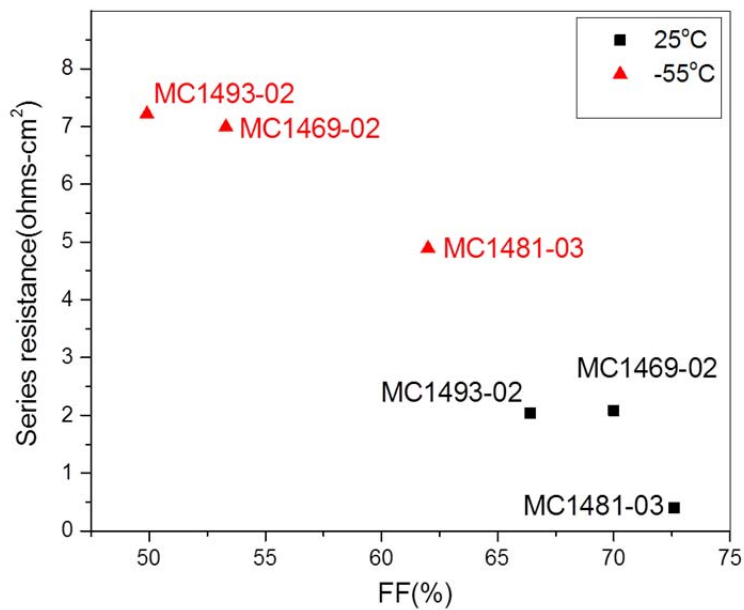


Figure 5.14 R_s vs. FF for FHJ devices at 25°C (black square dot) and -55°C (red triangle dot), full light intensity.

5.3.2 IBC Solar Cells

All of the IBC solar cells have normal shaped J-V curves both at room temperature and at low temperature as shown in Fig 5.15 and Fig 5.16. This is in contrast with the front heterojunction devices described above which have s-shaped curves at low temperature. Fig 5.17 indicates a correlation between series resistance and fill factor for IBC cells at -55°C. Devices MC1503-04 and MC1492-02 obtain higher series resistance and lower fill factor, resulting in decreased maximum power output. They also had strongest decrease in A at low temperature in Fig 5.11. On the contrary, MC1483-06, MC1483-10 and MC1497-09 obtain lower series resistance

(less than 2) and higher fill factor at -55°C . As a result, the power output is dominated by both R_s and FF.

The fact that the FHJ cells with an i-layer show clear evidence of a blocking contact at low temperature (i.e. the peak in dV/dJ) while IBC cells having the same doped and intrinsic layer contacts do not show evidence of a blocking contact is somewhat puzzling. Modeling by others from the IEC have shown that the s-shaped J-V curve in the light leading to low fill factor is due to the valence band offset since the photocurrent is due to hole collection[29]. This suggests the valence band offset is somehow different between FHT and IBC cells.

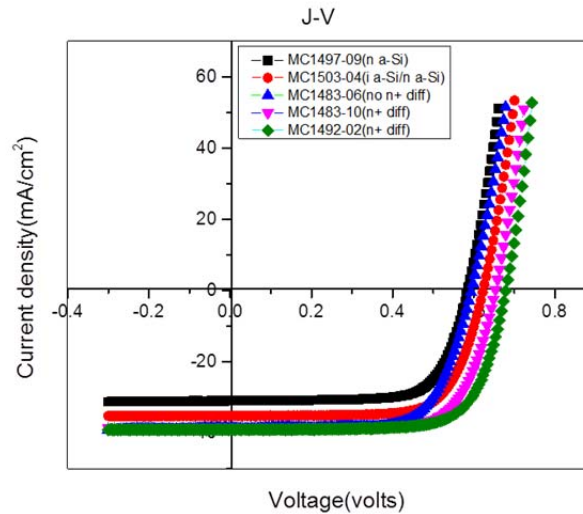


Figure 5.15 J-V curve for IBC solar cells measured at 25°C and full light intensity.

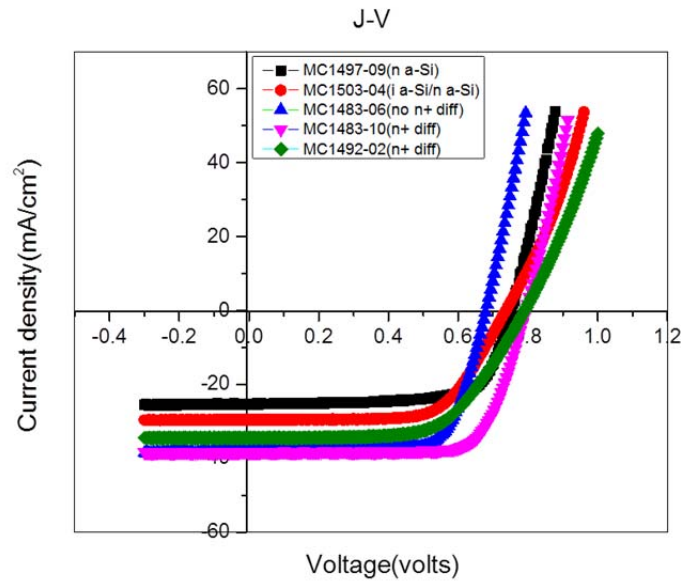


Figure 5.16 J-V curve for IBC solar cells measured at -55°C and full light intensity.

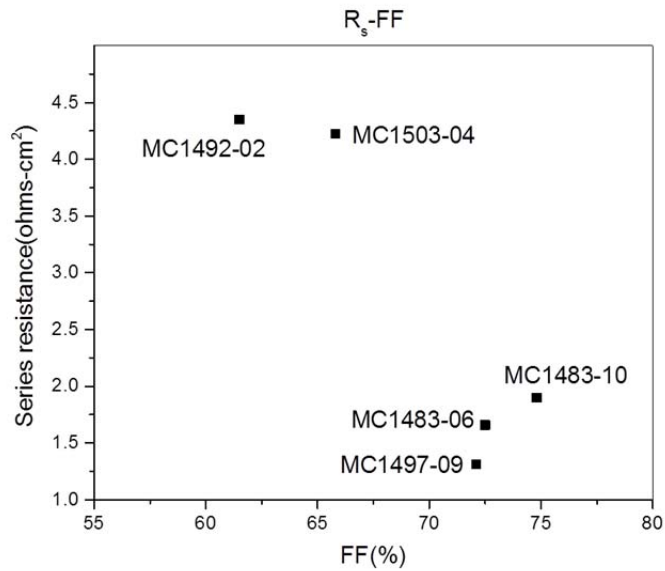


Figure 5.17 Series resistance vs. fill factor for IBC cells at -55°C and full light intensity.

Chapter 6

RESULTS AND DISCUSSION FOR ACIGS AND HIGH V_{oc} CIGS SOLAR CELLS

The cells measured and analyzed in this thesis were fabricated in the Institute of Energy Conversion. There were 7 pieces of ACIGS solar cells and 2 high open-circuit voltage CIGS (no Ag) solar cells included in the J-V-T measurements and further discussion in this section. Table 6.1 shows each type of ACIGS solar cell with difference in their processing sequence (1-stage vs. 3-stage) and composition. These have a significant impact on bandgap as shown[9]. From J-V-T measurement, temperature coefficients of V_{oc} and P_{max} can be obtained and compared with bandgap to see the impacts from different process and content of Ag and Ga. Also, at low temperature, some devices show anomalies such as, light-dark crossover, roll over effect and ideality factor less than 1 or much higher than 2. That will also be discussed in the following sections.

Table 6.1 Description of ACIGS solar cells absorber processing, composition (from EDS), and bandgap (from QE).

Cell number*	Stage-Ag/I-Ga/III	I/III	Ag/I	Ga/III	Eg(eV)**
A3LH	3-stage-low-high	0.86	0.26	0.51	1.27
A3HH	3-stage-high-high	0.8	0.6	0.54	1.32
A3HL	3-stage-high-low	0.92	0.25	0.39	1.22
A3LL	3-stage-low-low	0.85	0.32	0.36	1.22
A1LL	1-stage-low-low	0.85	0.3	0.32	1.19
A1LH	1-stage-low-high	0.87	0.35	0.44	1.24
A1HH	1-stage-high-high	0.91	0.58	0.5	1.32
C1	high Voc CIGS cell	0.7	N/A	0.71	1.48
C2	high Voc CIGS cell	0.78	N/A	0.72	1.44
I=(Ag+Cu), III=(In+Ga)					
*A=ACIGS cell, 3=3-stage, 1=1-stage, L=low content, H=high content					
C1 and C2 are high Voc CIGS cells					
**Calculated from QE measurement					

6.1 Results of J-V-T Measurement

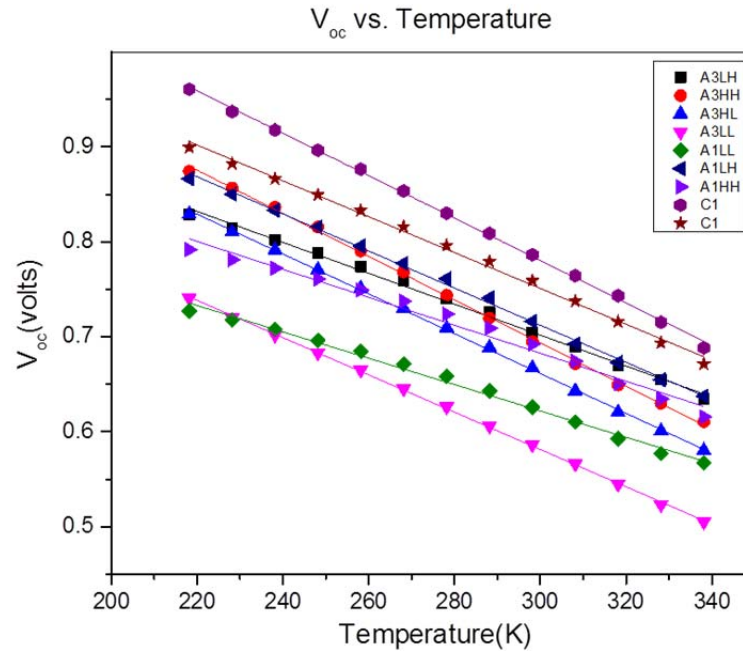
Table 6.2 shows the J-V data for ACIGS and high V_{oc} CIGS solar cells measured from standard simulator test system in IEC at 25°C. Devices A3LL obtains the lowest V_{oc} and A3LH obtains the highest V_{oc} and efficiency of all ACIGS devices. However, device A3HH shows the lowest efficiency of all ACIGS devices, due to the low J_{sc} and fill factor compared to others. Both of the high V_{oc} CIGS solar cells have the highest V_{oc} but the lowest J_{sc} and efficiency of all devices as expected for high bandgap.

Table 6.2 Initial data for ACIGS and high V_{oc} CIGS solar cells measured from standard simulator system.

	A3LH	A3HH	A3HL	A3LL	A1LL	A1LH	A1HH	C1	C2
Voc(V)	0.752	0.711	0.67	0.57	0.619	0.713	0.732	0.787	0.764
Jsc(mA/cm ²)	28.3	19.5	30.3	26.4	29.5	25.6	24.5	14.3	15.2
FF(%)	76.4	60.9	78.4	61.3	76.5	76.7	76.4	61.8	69.8
Eff(%)	16.3	8.5	15.9	9.2	14	14	13.7	7	8.1

Fig 6.1 shows V_{oc} is inversely dependent on temperature. Most devices indicate good linearity, except, devices A1LL and A1HH, which all tend to show the V_{oc} heading towards saturation below 250K. This effect is independent of temperature and light intensity and hence independent of recombination. This can happen at low temperature, (see section 5.1) indicating the recombination become ‘frozen out’ and a maximum splitting of the quasi-fermi levels so that V_{oc} is becoming limited[20, 26].

Fig 6.2 shows the saturation under different light intensities from device A1HH.



	A3LH	A3HH	A3HL	A3LL	A1LL	A1LH	A1HH	C1	C2
Intercept(volts)	1.19	1.376	1.291	1.17	1.038	1.298	1.124	1.45	1.317
Slope(V/K)	-0.0016	-0.0023	-0.0021	-0.002	-0.0014	-0.002	-0.0015	-0.0022	-0.0019

Figure 6.1 V_{oc} vs. temperature for ACIGS and high V_{oc} CIGS solar cells. The table shows intercept at $T=0K$ and slope from linear fit. Temperature coefficients shown in next section are fit from 230K to 330K.

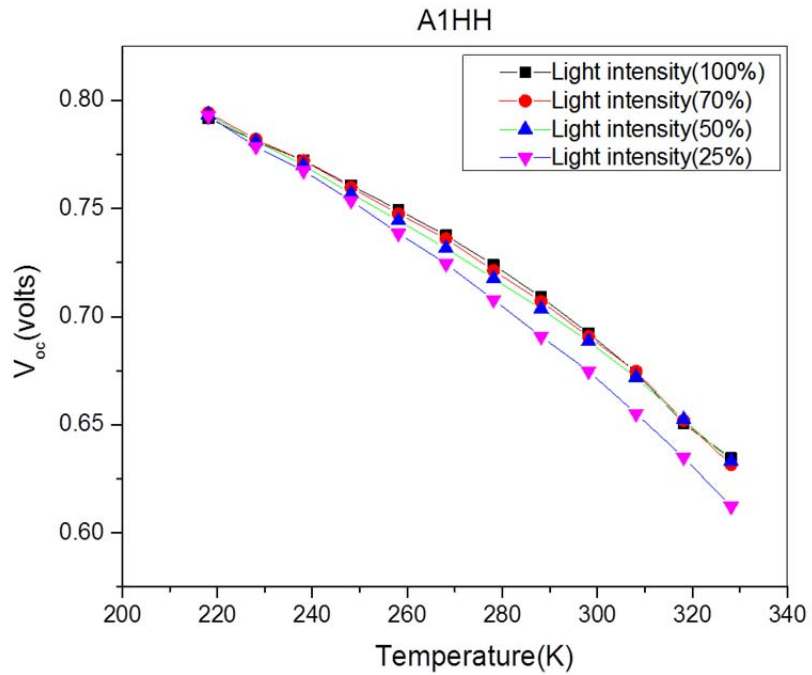


Figure 6.2 Diagram of V_{oc} vs. temperature for device A1HH which shows the voltage saturation at low temperature.

Fig 6.3 shows the plot of J_{sc} vs. temperature. It can be seen that J_{sc} is independent of temperature for all ACIGS and high V_{oc} CIGS solar cells. This is different from the Si cells shown in Chapter 5 since the bandgap of silicon cell will change slightly with temperature.

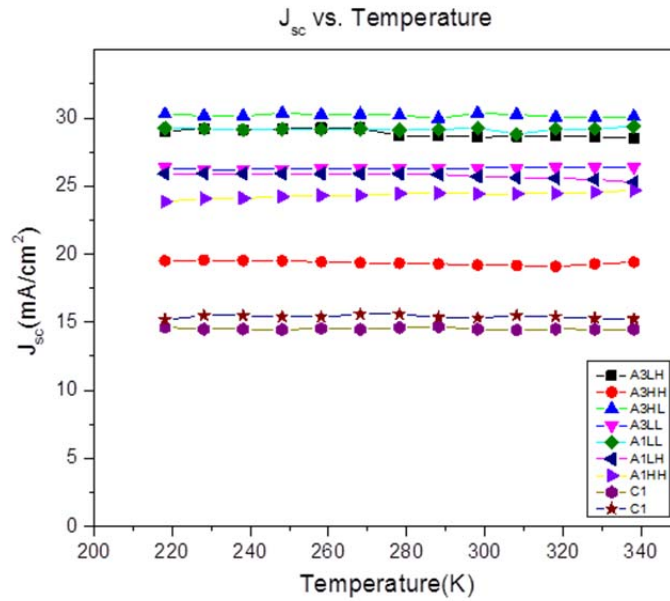


Figure 6.3 J_{sc} vs. temperature for ACIGS and high V_{oc} CIGS solar cells.

In Fig 6.4, most of the devices show FF and P_{max} are dependent of temperature. Device A3HL obtains the highest maximum power output at all temperatures. However, the two high V_{oc} CIGS devices obtain the lowest maximum power output compared to the other ACIGS solar cells. Device C1 shows a slightly decrease of P_{max} at temperature below 250K due to the reduction of fill factor. The fill factor and power tend to continue increasing monotonically and maintain the same relation to one another as temperature is reduced. There is negligible peaking and crossing of curves as was seen for Si cells in Fig 5.3 and Fig 5.8 (see section 5.1).

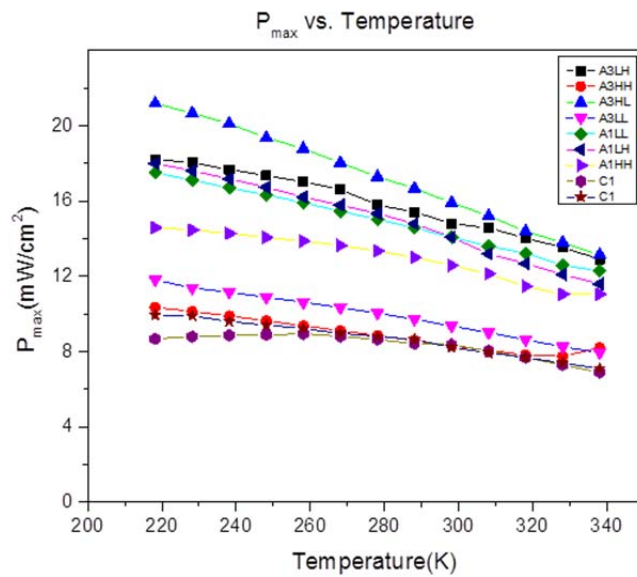
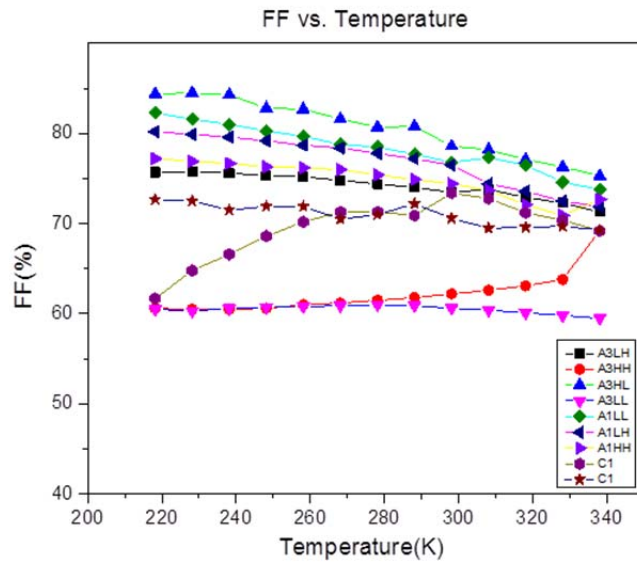


Figure 6.4 FF and P_{max} vs. temperature for ACIGS and high V_{oc} CIGS solar cells.

6.2 Temperature Coefficients, Bandgap and Activation Energy

The linear temperature fitting range to get temperature coefficient is from 230K to 330K. Activation energy is extrapolated from the plot of V_{oc} vs. temperature at $T=0K$. Bandgap is measured from the quantum efficiency (QE).

Table 6.3 Temperature coefficients, activation energy and bandgap for ACIGS and high V_{oc} CIGS solar cells.

Cell number	A3LH	A3HH	A3HL	A3LL	A1LL	A1LH	A1HH	C1	C2
Temperature coefficient of $V_{oc}(V/^{\circ}C)$	-0.0017	-0.0023	-0.0021	-0.002	-0.0015	-0.002	-0.0015	-0.0022	-0.0019
Temperature coefficient of $J_{sc}(mA/^{\circ}C)$	-0.0063	-0.0003	-0.0013	0.0011	-3.00E-05	-0.0047	0.0054	-0.0005	-0.0006
Temperature coefficient of $P_{max}(/^{\circ}C)$	-0.0048	-0.0025	-0.0071	-0.0032	-0.0045	-0.0058	-0.0036	-0.002	-0.0027
Activation energy(eV)*	1.204	1.395	1.301	1.176	1.063	1.316	1.146	1.455	1.327
Bandgap(eV)	1.265	1.319	1.216	1.216	1.192	1.24	1.319	1.476	1.442
Eg-Ea difference	0.061	-0.076	-0.085	0.04	0.129	-0.076	0.173	0.021	0.115
*Intercept of V_{oc} vs. T (at $T=0K$)									

Table 6.3 shows temperature coefficients and activation energy for all devices. Some of the devices obtain activation energy less than bandgap that could be caused from interface recombination[20]. The other devices show slight difference (less than 0.1) between bandgap and activation energy indicating the recombination mechanism dominate in the absorber layer[20]. Fig 6.5 shows V_{oc} generally increasing with higher bandgap at $25^{\circ}C$ as expected. Devices A3LL and A1LL, with low contents of Ag and Ga, show the lowest V_{oc} and bandgap.

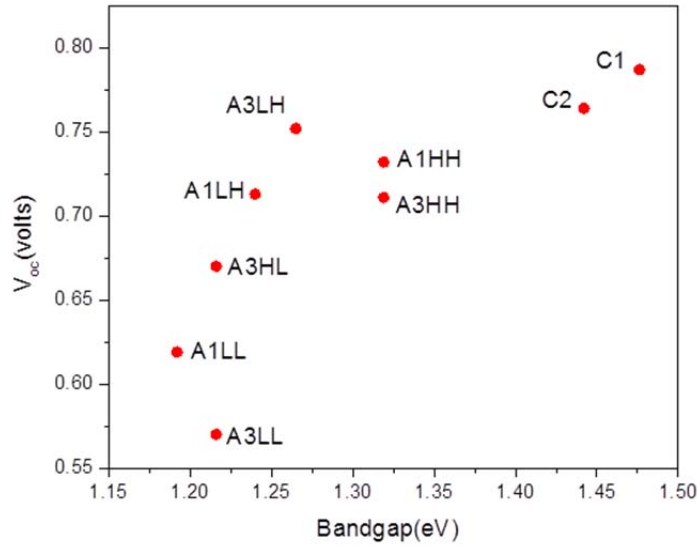


Figure 6.5 Diagram of V_{oc} vs. bandgap measured from QE.

Fig 6.6 shows the plots of temperature coefficient of P_{max} vs. bandgap. The high V_{oc} CIGS cells (down triangle symbols) show the low temperature-dependence behavior and highest bandgap. Devices A3HH and A1HH (square symbols) also indicate lower temperature coefficient of P_{max} and high bandgap. In contrast, device A3HL (hexagon symbol), indicates higher temperature coefficient of P_{max} and lower bandgap since Ga shows stronger impact on bandgap than Ag[15]. Devices A3LL and A1LL (diamond symbols), show low bandgap but still obtain smaller temperature coefficient of P_{max} . Thus, high V_{oc} CIGS cells and device A3HH obtain high bandgap and low temperature coefficient of P_{max} but the V_{oc} for device A3HH is not as high as expected for its bandgap.

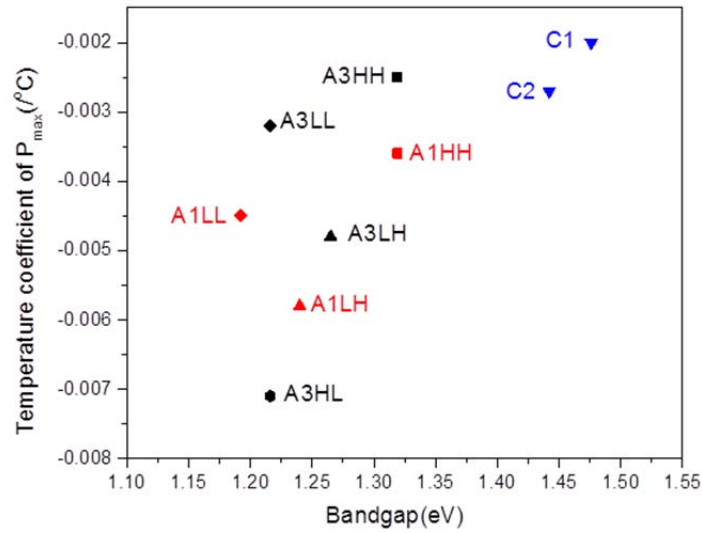


Figure 6.6 The correlation between temperature coefficient of P_{max} and bandgap measured from QE. The black dots represent the 3-stage ACIGS cells, red dots represent the 1-stage ACIGS cells, and the blue dots represent the CIGS cells.

Fig 6.7 shows the plot of temperature coefficient of V_{oc} vs. activation energy. Activation energy is extrapolated from intercept of V_{oc} vs. temperature at $T=0K$. This plot shows an opposite trend compared to Fig 6.6, indicating devices with high activation energy also tend to have a high temperature coefficient of V_{oc} .

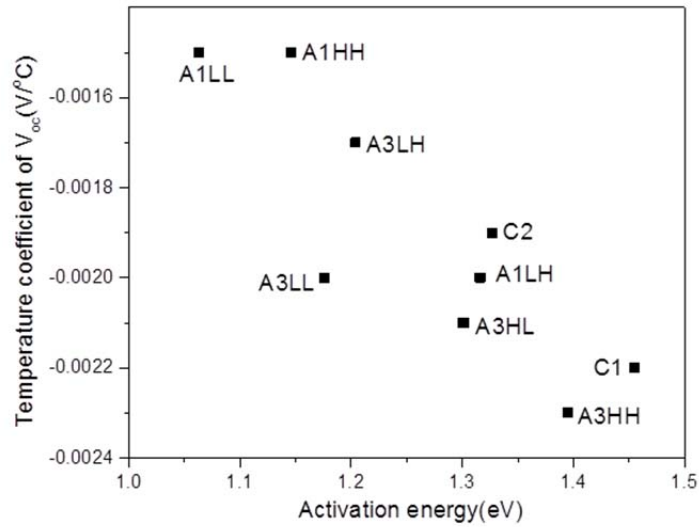


Figure 6.7 Temperature coefficient of V_{oc} vs. activation energy.

As a consequence, some conclusions can be made from the discussion above. High Ag and Ga contents can increase both device's V_{oc} and bandgap, but decrease the temperature coefficient of P_{max} . Devices with larger activation energy also indicate higher temperature coefficient of V_{oc} . Most devices show similarity between activation energy and bandgap which means the absorber layer is dominated by the Shockley-Read-Hall (SHR) recombination mechanism[20]. Comparing the ACIGS cells with Taiwan Semiconductor Company's (TSMC) CIGS cell[30], ACIGS cells show lower temperature coefficient of V_{oc} and wider bandgap, while TSMC CIGS cell obtain a lower temperature coefficient of P_{max} . The temperature coefficient of TSMC CIGS cell can be seen in Table 6.4.

Table 6.4 Temperature coefficient of TSMC CIGS solar cell.

	TSMC CIGS
Temperature coefficient of Voc(V/°C)	-0.0029
Temperature coefficient of Jsc(mA/°C)	0.0001
Temperature coefficient of Pmax(/°C)	-0.0031

6.3 Ideality Factor A

Ideality factor A can represent different types of recombination in the diode. It should range between 1 and 2 with 1 representing recombination in the neutral region and 2 representing pure Shockley-Read-Hall (SRH) recombination in the depletion region. From J-V-T measurement, most of the devices show that ideality factor is independent of temperature and within the range between 1 and 2 which could be caused by same order of magnitude recombination in the neutral and depletion region. However, some of the devices show the ideality factor is higher than 2 or less than 1. In this section, all devices are distributed into three groups, which are shown in the following list.

Group	A
Description	Ideality factor is independent of temperature and the range is between 1 and 2.
Cell number	A3HH, A3HL, A1LH, C1
Group	B
Description	Ideality factor is less than 1 and shows the independence of light intensity.
Cell number	A1LL, A1HH
Group	C
Description	Ideality is higher than 2 especially at low temperatures.
Cell number	A3LH, A3LL, C2

Fig 6.8 shows the plot of ideality factor vs. temperature. The value A was calculated from equation $A = \frac{1}{\text{slope} \times kT / q \times 2.3}$ (see section 4.1). Note that most are in the normal range between 1 and 2 above 300K. Groups A devices show the ideality factor range between 1 and 2 at all temperatures which mean they have good diode operation quality during J-V-T measurement. Group B devices (1-stage) showed the ideality factor is much less than 1 at temperature below 300K, which is due to the V_{oc} is independent of light intensity and saturates at low temperatures, so the slope of $\log J_{sc}$ vs. V_{oc} is becoming meaningless. Group C devices (3-stage-low Ag) have the ideality factor higher than 2 which can be caused from the possibility of tunneling-enhanced recombination.

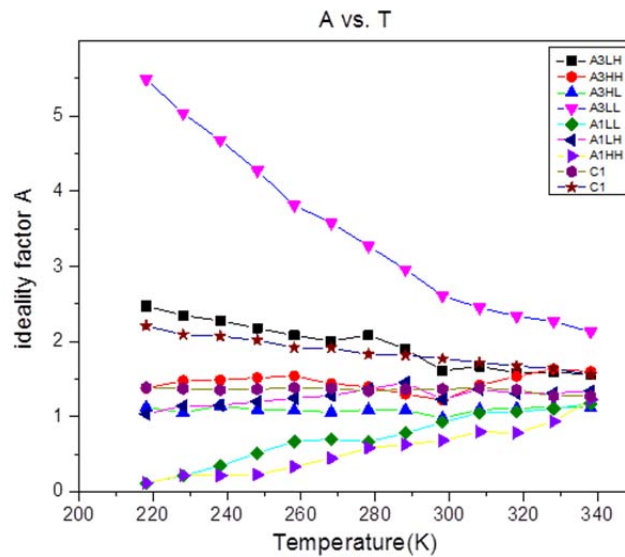


Figure 6.8 Ideality factor vs. temperature for ACIGS and high V_{oc} CIGS solar cells.

Fig 6.9 shows the plot of inverse ideality factor vs. temperature for group C devices (devices with $A > 2$) and C1, one of the group A devices ($1 < A < 2$). It can be inferred that devices with ideality factor larger than 2 with a strong temperature dependence behavior might have a possibility of tunneling-enhanced recombination at even lower temperatures. The equation $\frac{1}{A} = \frac{1}{2} \left(1 + \frac{T}{T^*} \right)$ shows the device without tunneling-enhanced recombination will have an intercept of 0.5 at $T=0K$. [31, 32]. However, from linear fit to the equation $\frac{1}{A} = \frac{1}{A_0} \left(1 + \frac{T}{T^*} \right)$, where A_0 represents the ideality factor for group C devices at $T=0K$, the fitting yields negative values unphysically realistic since group C devices have already obtained the ideality factor larger than 2 at $T=200K$.

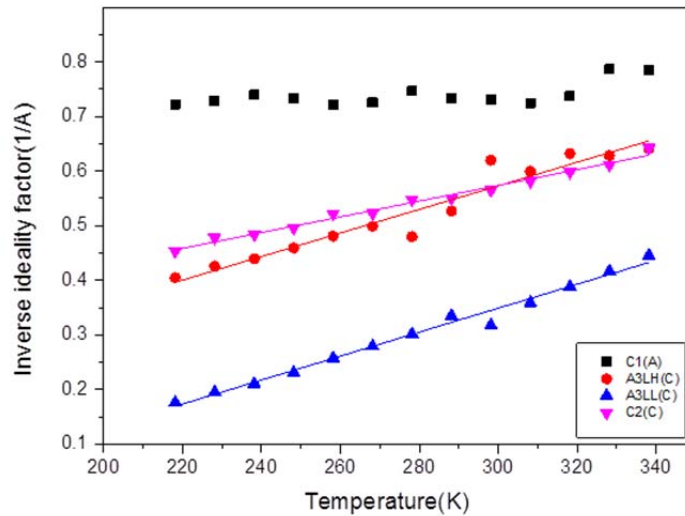


Figure 6.9 Inverse ideality factor vs. temperature.

6.4 Low Temperature Performance and Interpretation on Anomaly J-V Curve

In this section, two low temperature phenomenon will be discussed. The first one is light-dark crossover. Light and dark J-V curve cross at a large forward bias and the dark curve appears to have a higher barrier or lower J_0 [33]. Light-dark crossover in thin film solar cells is well studied. Fig 6.10 shows device A1HH obtain light-dark crossover effect at 5°C and -55°C . It is obvious that the crossover effect start getting worse when temperature getting lower as well. There are three other devices also obtain the light-dark crossover effect, A1LL, A1LH and A3HH. All of the 1-stage process ACIGS devices obtain light-dark crossover effect at low temperature. It can be caused from the enhanced photoconductive CdS or the changes in conduction band offset between absorber layer and buffer layer and thus reducing the electron barrier in the dark[33, 34].

Another effect which can also be commonly observed in ACIGS solar cells, and many other thin film solar cells as well, at low temperature is roll over effect. It indicates current saturation at an electric forward bias[33]. Fig 6.11 shows device A3HH roll over effect at low temperatures compared to room temperature. The effect enhances as temperature getting lower. It can due to the blocking contact and lower carrier density. The device also shows light-dark crossover effect, it may result from a minority carrier recombination at back contact junction[33]. The crossover and roll over effects can also be modeling by SCAPS simulation that shows good agreement with J-V-T measurement[35].

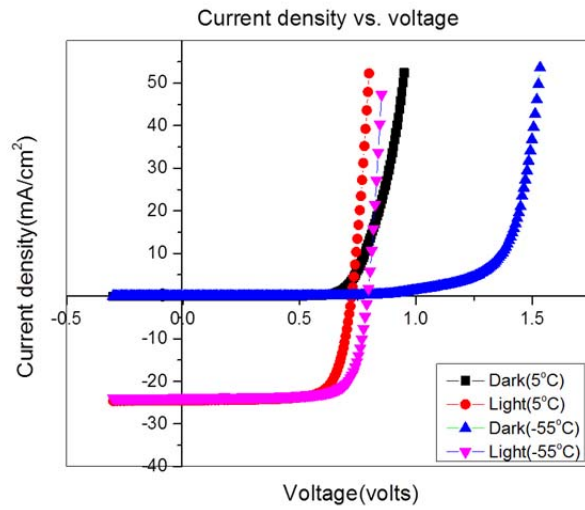


Figure 6.10 Light-dark J-V curve crossover for device A1HH, at 5°C and -55°C.

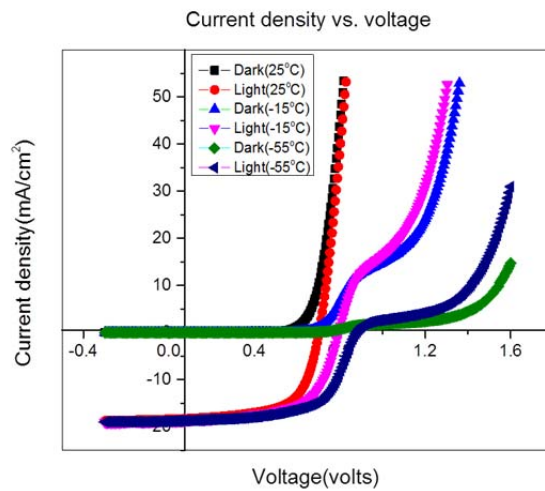


Figure 6.11 J-V curve roll over effect for device A3HH at 3 temperatures.

Chapter 7

CONCLUSIONS AND FUTURE WORK

By analyzing various FHJ, IBC and ACIGS solar cells' parameters from J-V-T measurement, the devices temperature dependent performance were obtained and discussed.

7.1 Discussion for FHJ and IBC Solar Cells

FHJ cells obtain higher V_{oc} than IBC cells but also lower J_{sc} and FF than IBC cells. Some IBC cells show voltage saturation at low temperature while FHJ cells don't. Fill factor shows impact on maximum power output for both FHJ and IBC cells. At low temperature, cells with front and back i-layer MC1469-02 and MC1493-02 show s-shape J-V curve which makes the series resistance increase and decrease the fill factor. The cell without an i-layer did not show an s-shape J-V curve at low temperature, so although it had a much lower efficiency at 300K, it had a much higher efficiency at 240K. The correlation between series resistance and fill factor can be seen both on FHJ and IBC cells. The higher the series resistance, the lower the fill factor, and thus, the maximum power output will decrease as well.

FHJ cells have a clear correlation between temperature coefficient of P_{max} and V_{oc} . The results show that device with higher V_{oc} tend to have lower temperature coefficient of P_{max} . Nevertheless, IBC cells do not show this behavior. Both FHJ and IBC cells obtain the ideality factor with the value between 1 and 2. In general, device with good diode quality and performance usually shows the ideality factor close to 1. The results show that FHJ cell MC1469-02 (with intrinsic layer) and IBC cells MC1483-10, MC1492-02 (both with n+ diffusion on the front surface) and MC1503-

04 (with i a-Si/n a-Si) obtain ideality factor closer to 1 at low temperature. Device MC1493-02 with only 13% n-strip coverage on the back shows the highest V_{oc} and lowest temperature coefficient of P_{max} suggesting that P_{max} is controlled by the passivation quality of the surfaces.

7.2 Discussion for ACIGS Solar Cells

ACIGS solar cells indicate different temperature dependence behaviors on J_{sc} , FF and P_{max} , compared to FHJ and IBC solar cells. J_{sc} is constant rather than showing a slight increase like silicon solar cells. Instead of showing FF and P_{max} which increase then decrease with lower temperatures, most ACIGS solar cells show their FF and P_{max} which are more linear than silicon solar cells. The recombination becomes ‘frozen out’ for some ACIGS devices at temperature below 250K so that V_{oc} is limited.

Fig 7.1 shows the plot of V_{oc} vs. E_a for both silicon (FHJ and IBC) and ACIGS cells. The correlation between V_{oc} and E_a can be seen in IBC and ACIGS cells while FHJ devices did not show a significant correlation between these two parameters. Also, most of ACIGS devices show the activation energy approximately 0.1 eV less than the bandgap, that is to say, the SRH recombination may dominate in the absorber layer. Devices with high contents of Ag and Ga obtain higher V_{oc} and bandgap. Furthermore, those devices also show the lower temperature coefficient of P_{max} . However, devices with larger activation energy indicate higher temperature coefficient of V_{oc} .

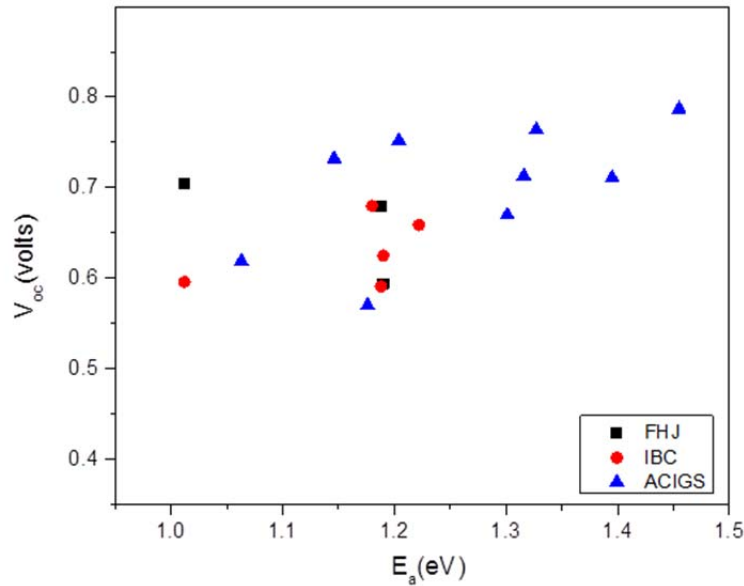


Figure 7.1 V_{oc} vs. activation energy extrapolated at $T=0K$.

Three types of recombination mechanism can be shown from the value of ideality factor. Devices with ideality factor range between 1 and 2 obtain good diode performance. Devices with ideality factor less than 1 can be resulted from the saturation of V_{oc} at low temperature. Devices with ideality factor higher than 2 can be caused from the possibility of tunneling-enhanced recombination.

Light-dark crossover and roll over effects are commonly seen in thin film solar cells with decreasing temperature, which can result from photoconductive buffer layer, barrier at the front heterojunction which blocks minority carrier collection and lower carrier density and minority carrier recombination at back contact junction.

The comparison between temperature coefficient of P_{max} and temperature coefficient of V_{oc} is shown in Fig 7.2. It is hard to find a correlation between these two

parameters. However, Fig 7.3 indicates the correlation between temperature coefficient of P_{max} and temperature coefficient of $V_{oc} * (J_{sc} * FF)$. Both FHJ and ACIGS cells show the positive trend of correlation which is less significant in IBC cells. As a result, it can be inferred that temperature coefficient of P_{max} can also be dominated by J_{sc} and FF for most devices.

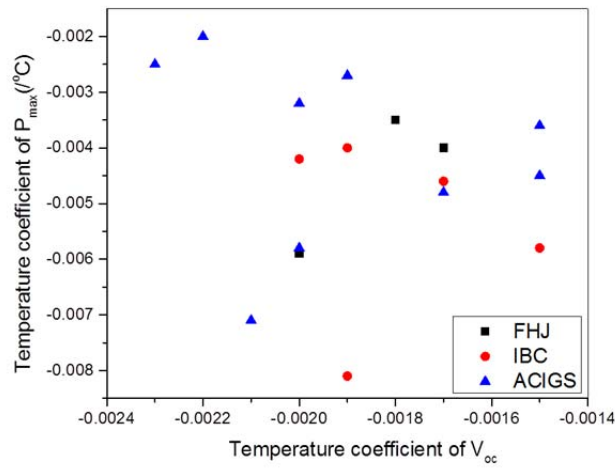


Figure 7.2 Temperature coefficient of P_{max} vs. temperature coefficient of V_{oc} .

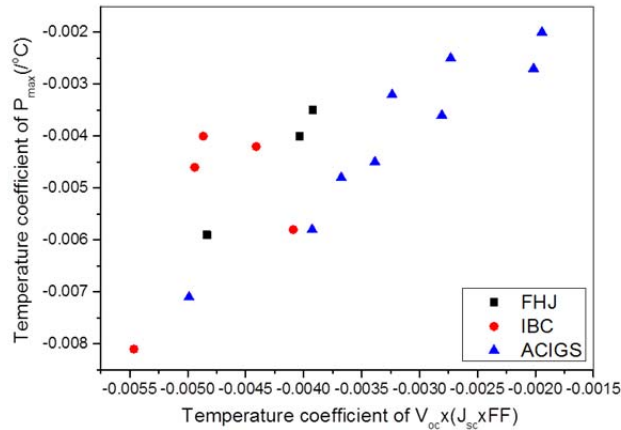


Figure 7.3 Correlation between temperature coefficients for FHJ, IBC, and ACIGS cells.

7.3 Future Work

For silicon solar cells in this work, FHJ cells obtain lower fill factor than IBC cells. The FHJ cell with n-strips on the back shows highest V_{oc} and lowest temperature coefficient of P_{max} but the fill factor is 66.4%. So, for the future work, we would like to measure another FHJ cell with both high V_{oc} and fill factor to see if the device can also show high efficiency and low temperature coefficient of P_{max} .

Furthermore, another IBC cell without n+ diffusion on the front surface but obtain high efficiency (~20%) will be measured. It can be compared with the one with n+ diffusion on the front surface to see if the diffusion really shows impact on temperature coefficient of P_{max} .

Since 1-stage ACIGS cells in this work all obtain light-dark crossover effect, we would also want to measure another 1-stage ACIGS cell with high content of Ag and low content of Ga to see if light and dark crossover effect will occur at low temperature.

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