THERMALLY ENHANCED

MUTC PHOTODIODES

by

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Summer 2024

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ABSTRACT

Modified uni-traveling carrier photodiodes offer world leading capabilities in terms of their power handling and linearity. For this reason, it is no surprise that they are an irreplaceable tool in RF Photonics, namely in RF Photonic links. As these devices develop further, applications for them will continue to grow, but not until significant advancements are made in their power handling capability. As of now, joule heating remains a factor not addressed within MUTC epitaxies which leads to thermal failure.

In this work, developments are made on a new MUTC epitaxy which specifically addresses joule heating for the first time. Based on simulations from UVA, this epitaxy has the capability to increase dissipated power at failure, but to produce useful, functional devices from this epitaxy is an entirely new challenge. The process and considerations of making devices from this new epitaxy will be shown. As will be demonstrated, this epitaxy under the right conditions offers a promising future for increasing power handling capabilities.

Chapter 1

MOTIVATION FOR HIGH POWER MUTC PDS

1.1 Overview of MUTC PDs

Modified uni-traveling carrier photodiodes serve as an irreplaceable tool in modern RF photonics applications. In a MUTC structure, carriers are generated in an undepleted InGaAs absorption region, which allows for the transit of only electrons through an InP drift region, as opposed to both electrons and holes. Because only electrons are transited through this drift, the total transit time for these devices is lower than would be possible for a traditional P.I.N. structure photodetector.

With a transit time that is kept low, MUTC photodiodes are capable of high frequency operation up to 110 GHz, and Radio Frequency (RF) power outputs as high as 25 dBm, allowing them to be useful tools in analog optical links and phased antenna array transmitters. In the case of analog optical links, noise figure is inversely proportional to the square of the photodetector's photocurrent, making the photodetector's power handling critical. For phased array transmitters, the power available for the link itself is proportional to the current squared of the photodetector, again meaning that a photodiode with high power handling is critical. It stands to reason that both of these types of systems are directly benefitted by extending the capabilities in RF output power for the MUTC photodetectors used within them.

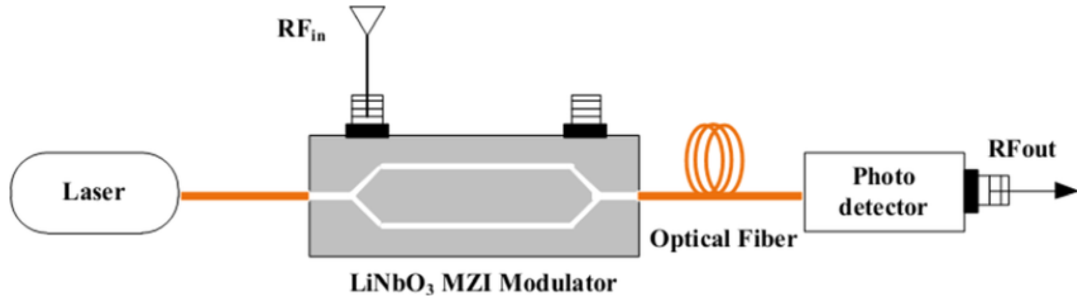

Figure 1.1 Basic diagram of a RF photonic link [5].

$$F = \frac{V_\pi^2 N_{out}}{I_{dc}^2 \pi^2 R_i R_o \left|H_{pd}\right|^2 k_B T_s'}$$

Equation 1.1. V. J. Urick, K. J. Williams, and J. D. McKinney detail the noise factor for an IMDD link including an inverse square relationship to the photodetector's DC photocurrent [2].

1.2 MUTC vs. P.N. Junction Photodetectors

In a standard P.N. junction photodiode, both a P-type and an N-type semiconductor are joined together, which causes an intrinsic region to form in between. Upon illumination, photons absorbed in this intrinsic region generate pairs of electrons and holes. From here, under the influence of an electric field, the electrons and holes move in their respective opposite directions based on their polarity. It is the movement of the electrons and the holes in these directions which is the final current through the device, ultimately being the current source that the device provides for the user or system. Because both the electrons and the holes contribute to this current, both of their respective transit times (often different) are responsible for determining the overall transit time and thus the maximum cutoff frequency for the device.

In Uni-Traveling Carrier and Modified Uni-Traveling Carrier photodiodes, photons are absorbed in an n-type region referred to as the absorption region. In this region, the electrons and holes are generated the exact same way as would happen in an intrinsic region, but due to the location of this n-type region the holes are quickly swept out of the device. The electrons on the other hand move in the opposite direction where they travel very quickly through the bulk of the device which has been designed to keep their travel time as low as possible. The electrons are therefore the main contributors to the current through the device, and as a result the total transit time is dictated by them. Because the transit time of the electrons has been designed to be low, these photodiodes are capable of cutoff frequencies that would otherwise not be attainable.

In short, UTC and later modified MUTC photodiodes use only electrons as their single (uni) traveling carrier to achieve extraordinary cutoff frequencies compared to traditional P.N. junction detectors. Traditional P.N. junction detectors, with their use of both electrons and holes as traveling carriers are significantly slowed down. While traditional P.N. junction detectors certainly still have applications, today’s push to use higher frequencies in 5G and beyond technologies means that MUTC photodetectors are the clear choice.

$$B = \frac{1}{\sqrt{\left(\frac{1}{f_{RC}}\right)^2 + \left(\frac{1}{f_d}\right)^2}}$$

Equation 1.2. A photodetector's bandwidth in terms of its RC and transit time components.

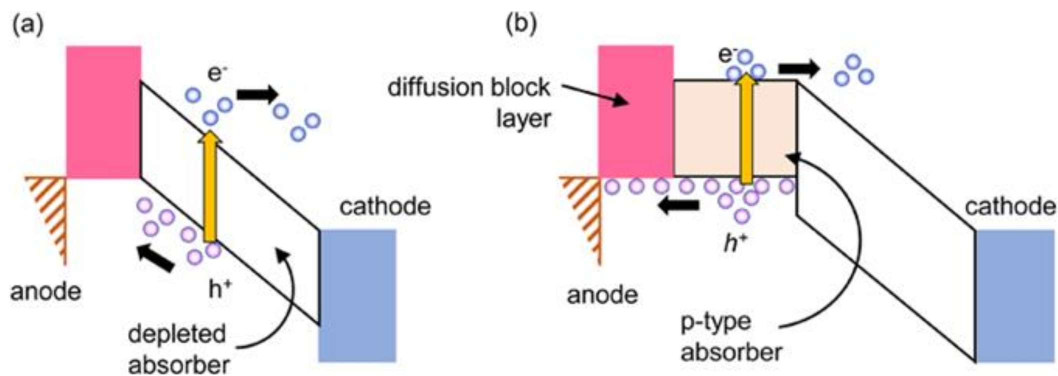

Figure 1.2. Band diagrams of (a) pin-PD and (b) UTC-PD [4].

1.3 Power Handling Limitations

In terms of RF output power capabilities, MUTC PDs have two limiting factors that are often problematic. The first is space charge screening, arising from the fact that photogenerated carriers distributed throughout the depletion region have their own associated electric field that opposes the ionized dopant and bias field. This opposing field can be enough at high current levels to increase transit time, leading to saturation of the detector. The second limiting factor, the focus of this work, is thermal

failure, where the joule heating associated with the photocurrent multiplied with the bias voltage causes non-reparable damage to occur somewhere within the device. The most common and successful method for addressing this problem is flip chip bonding these devices to highly thermally conductive submounts, where heat is transferred out of the device to keep the device's internal temperature as low as possible.

For flip chip bonding, the most common options for submounts are aluminum nitride and diamond, diamond being better because of its higher thermal conductivity. In both cases, these submounts contain coplanar waveguides with bonding pads, such that these bonding pads form strong electrical contacts to the coplanar waveguides, and strong thermal contacts to the heat dissipating (aluminum nitride or diamond) substrate. In this work, the more standard aluminum nitride submounts were used.

As effective as flip chip bonding is at keeping internal device temperatures low, The University of Virginia in 2023 demonstrated through simulation of MUTC epitaxies that joule heating is most significant within the drift region, which is unideal because of its placement on the opposite side of the epitaxy from where the heat sinking submount will later go. In this epitaxy, a significant portion of InGaAs, which has low thermal conductivity, lies between the drift region and the submount, meaning that heat sinking from the submount is severely limited.

1.4 Flipped Absorber Epitaxy

In the flipped absorber epitaxy, which is the focus of this work, the MUTC epitaxy has been rearranged for best possible thermal performance. The drift region sits nearest to the flip chip bonded submount side, and the undepleted absorber sits closest to the substrate side. In this manner, as photo-generated electrons travel through the drift region, the resulting joule heating transfers easily to the submount,

with no InGaAs barrier in between. In this orientation, devices from this epitaxy will be N-side down, but still maintain a standard backside illumination as is typical. In comparing this epitaxy to standard MUTC epitaxies, UVA determined that the flipped absorber epitaxy's improved heat sinking will translate to a 110% improvement in dissipated power density at thermal failure when used on aluminum nitride submounts [1].

In the following diagrams are a traditional MUTC epitaxy (left) and the flipped absorber MUTC (right). The undepleted absorbers of each are seen in green, the P-contacts in blue, and the N-contacts in orange. As seen, the flipped absorber epitaxy is completely inverted with respect to the illuminated substrate side and the oppositely located flip chip bonded side. For this reason, a device based on P and N-mesas must be bridged through a 900 nanometer N-contact region in the traditional epitaxy, and through a 150-nanometer P-contact in the flipped absorber epitaxy.

Traditional MUTC 4 epitaxy	Flipped absorber epitaxy
InGaAs, p^+, Zn, 2e19, 50nm	InP, n^+, Si, 1e19,50nm
InP, p^+, Zn, 2e18, 100nm	InP, n^+, Si, 1e18,100nm
InGaAsP, p^+, Q1.1, Zn, 5e18,15nm	InP, n^-, Si, 1e16,900nm
InGaAsP, p^+, Q1.4, Zn, 5e18,15nm	InP, n^-, Si, 1.4e17,50nm
InGaAs, p^+, Zn, 5e18,150nm	InGaAsP n^-,Q1.1 Si, 1e16,15nm
InGaAs, p^+, Zn, 2.4e18,200nm	InGaAsP, n^-,Q1.4, Si, 1e16,15nm
InGaAs, p^+, Zn, 1e18,200nm	InGaAs, n^-,Q1.4, Si, 1e16,150nm
InGaAs, n^-, Si, 1e16,200nm	InGaAs, p^-, Zn, 5e17,250nm
InGaAsP, n^-,Q1.4, Si, 1e16,15nm	InGaAs, p^+, Zn, 8e17,200nm
InGaAsP, n^- Q1.1, Si, 1e16,15nm	InGaAs, p^+, Zn, 1.2e18,150nm
InP, n, Si, 2.8e17,50nm	InGaAs, p^+, Zn, 2e18,100nm
InP, n^-, Si, 1.5e16,200nm	InGaAsP, p^-,Q1.4, Zn, 2e18,15nm
InP, n^-, Si, 1e16,250nm	InGaAsP, p^- Q1.1, Zn, 2e18,15nm
InP, n^+, Si, 1e18,100nm	InP, p^+, Zn, 2e18,400nm
InP, n^+, Si, 1e19,900nm	InGaAs, p^+, Zn, 3e19,150nm
InP semi-insulating substrate	InP semi-insulating substrate

Figure 1.3. Traditional MUTC 4 epitaxy (left) and flipped absorber epitaxy (right).

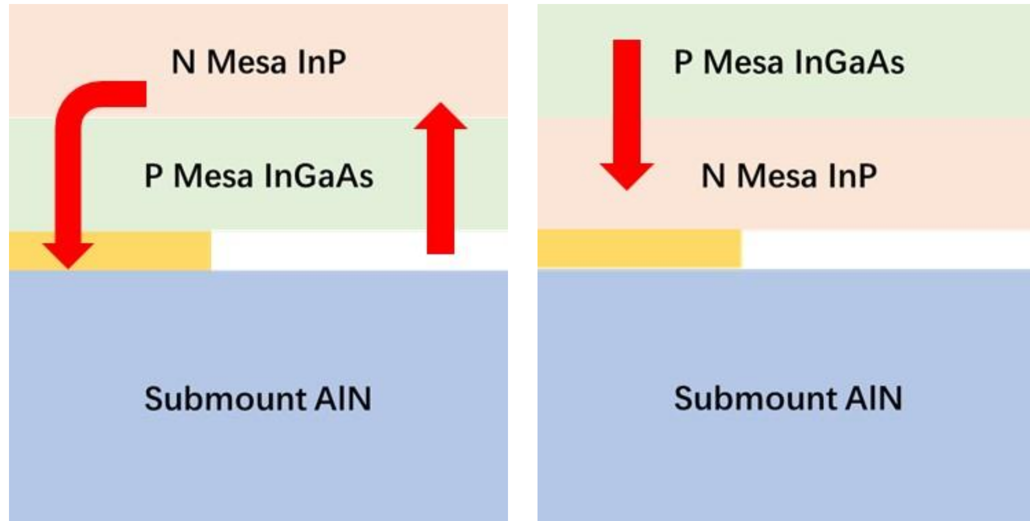

Figure 1.4. Schematics of normal MUTC PDs (left) compared with flipped MUTC PDs (right) when flip chip bonded to AlN submounts. Red arrows summarize the general heat flow in each epitaxy, which in the case of the flipped MUTC is direct to the submount without any InGaAs reflection.

Chapter 2

FABRICATION OF FLIPPED ABSORBER DEVICES

2.1 Overview

With the goal of being made into N-side down but backside illuminated photodetectors, the flipped absorber epitaxy was made with an InGaAs P-contact that is 150 nanometers in thickness. Because InGaAs has a bandgap that matches the photon energy at a 1.55-micron wavelength, it was critical that this region was made thin to reduce early absorption. Premature absorption of light in this region reduces the photons absorbed in the intended undepleted absorber region, and thus will lead to a lower responsivity. While ensuring a high responsivity from fabricated devices, this thin P-contact region added a number of considerations to the fabrication process.

To make devices from this epitaxy, mesas were etched from the N-contact to the P-contact using a hybrid ICP and wet etch approach to form N-mesas. After the completion of N-mesas, contact metal was placed at each mesa base with a liftoff process to form P-contacts. With the addition of finalizing steps for device isolation and sidewall passivation, these N-down devices were gold electroplated at their contact points to allow for flip chip bonding to aluminum nitride submounts. In total, this process included five different contact lithography steps and associated mask patterns.

As mentioned previously, this epitaxy has a relatively thin P-contact region of 150 nanometers. ICP etching always has an associated etch depth error, and in this case of this epitaxial structure, an over etch into this region would translate into

significant added series resistance. To address this issue, an ICP etching system was used only for the creation of N-mesas down to its 400 nm InP electron blocking layer. From here, an InP wet etch was used to remove this layer, thus completing the N-mesa. In this manner, the ICP etch kept the mesa sidewalls as straight as possible, while the high selectivity of the InP wet etch guaranteed an etch stop set perfectly at the top of the P-contact region.

2.2 N-Mesa ICP Etch

Beginning with a Ti/Pt/Au/Ti evaporation for N-contact metal, an SiO2 hard mask was first deposited, with the addition of a lithography pattern for N-mesa features. A Fluorine ICP system was used to translate these features into the hard mask. Next, the sample was CL ICP etched, with the intention of forming mesas terminating perfectly in the center of the InP electron blocking layer. By targeting the center, etch depth error could be plus or minus 200 nanometers with no major consequences. A stylus profilometer was used to confirm that this etch had in fact ended near the center of this region.

Layer #	Material	Thickness	Recipe
1	Ti	0.1 kÅ = 10 nm	38
2	Pt	0.2 kÅ = 20 nm	40
3	Au	1 kÅ = 100 nm	49
4	Ti	0.1 kÅ = 10 nm	38

Table 2.1. N-contact metal evaporation deposition.

Figure 2.1. Lithography features for N-mesas are added on top of N-contact metal and SiO2 hard mask.

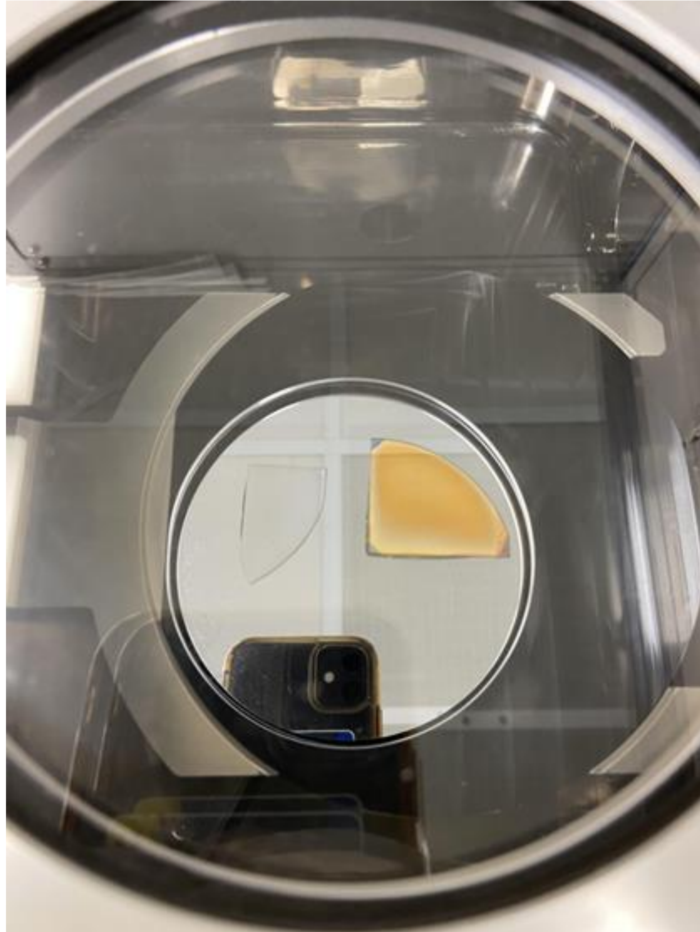

Figure 2.2. Placement of SiO_2 witness sample for F-ICP defined hard mask (left). As seen, the silicon is back to its regular color, indicating that the SiO_2 has been removed everywhere besides the areas protected by the photoresist lithography pattern.

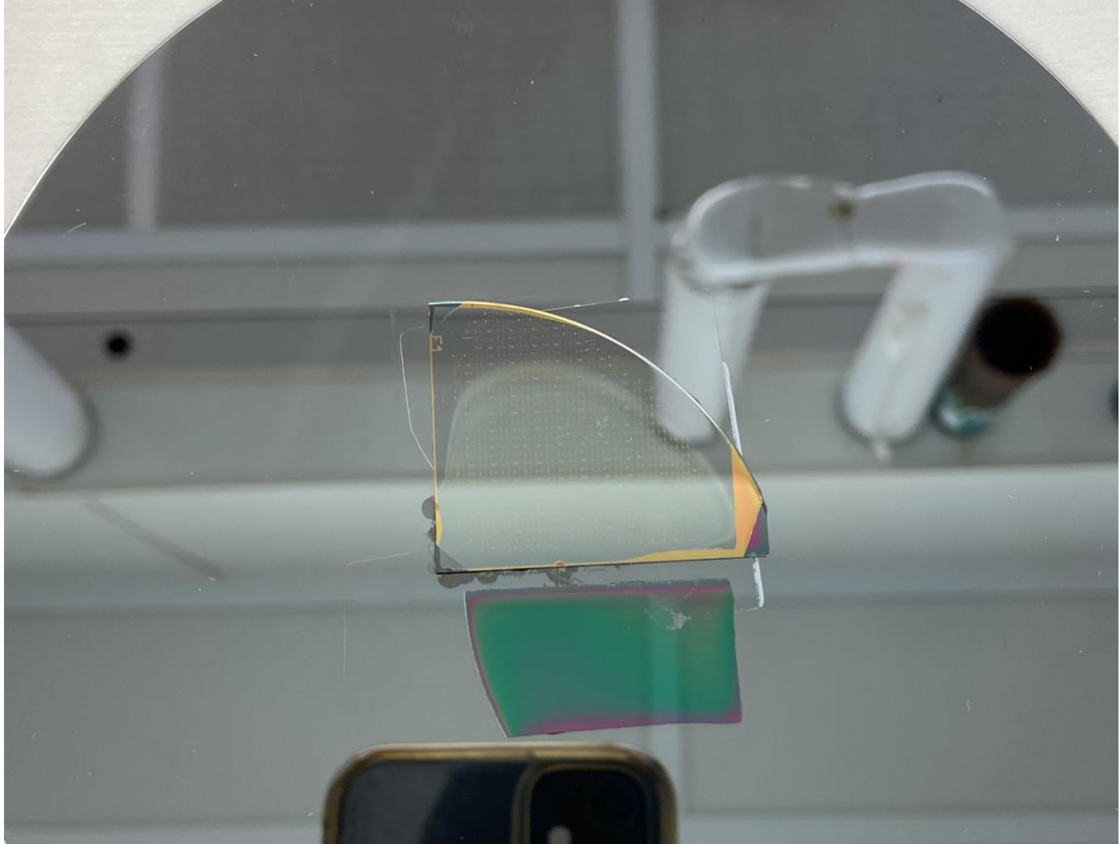

Figure 2.3. Flipped absorber sample and witness sample midway through CL-ICP mesa etch. Different shades of gray show a slight variance in etch rates.

As can be seen in figure 2.3, there was a noticeable variance in etch rate across the flipped absorber sample during the CL-ICP mesa etch. This is indicated by different shades of gray when moving radially outwards from the center of the carrier wafer. In the case of this etch step, this was a problem because the targeted electron blocking layer is only 400 nanometers thick. Thus, if the variance in etch depth was more than 400 nanometers, it would be impossible for all the devices to have their mesas ending in the electron blocking layer.

To address this non-uniformity in etch rate, the flipped absorber sample was taken out of the CL-ICP midway through the mesa etch and rotated 180 degrees with respect to the witness sample. After doing so, the flipped absorber sample was seen to have a much more uniform gray color than that seen in figure 2.3, as indicated below in figure 2.4. Without this critical step, it is unlikely that the electron blocking layer would have been correctly reached in every device, which would make it unlikely for the wet etch in the next section to have worked.

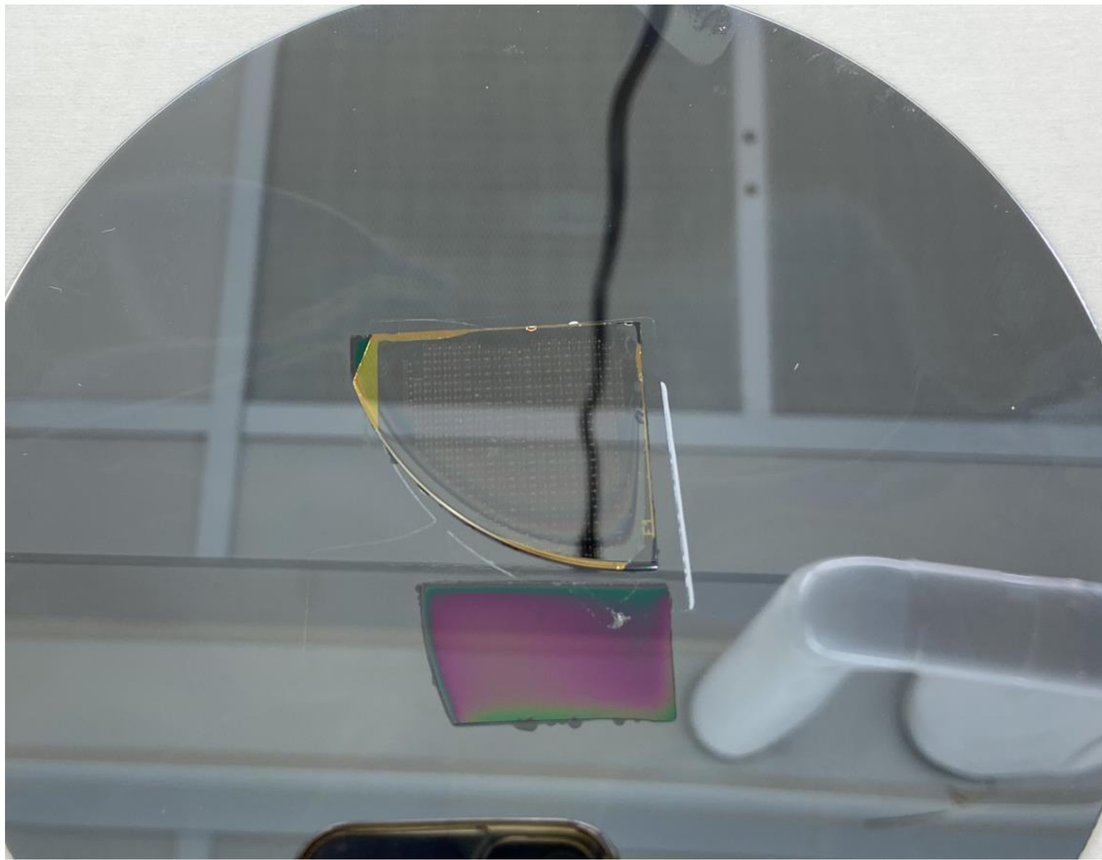

Figure 2.4 Flipped absorber sample at the end of CL-ICP mesa etch. As can be seen, rotating the sample with respect to the witness sample allowed for a better total uniformity in etch depths.

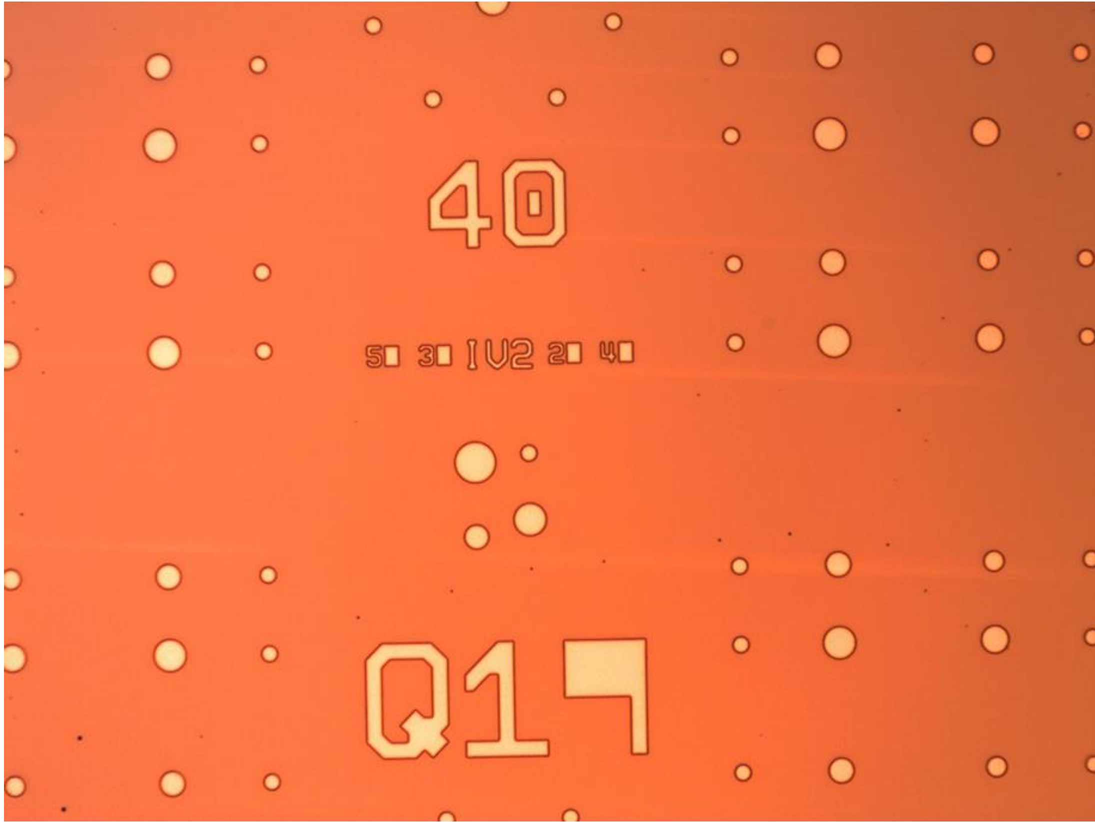

Figure 2.5. Flipped absorber sample after CL-ICP mesa etch.

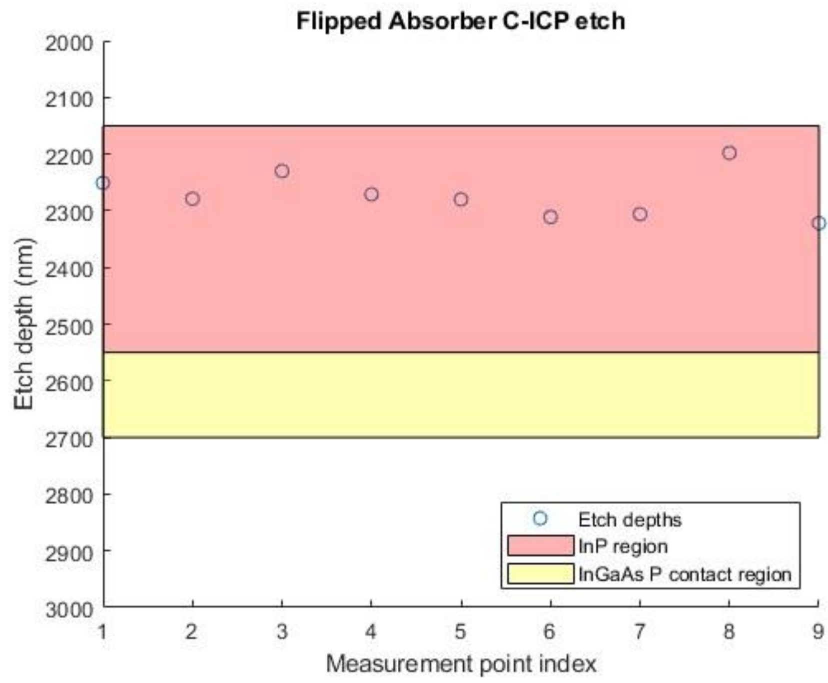

Figure 2.6. Stylus profilometer measurements taken after CL-ICP etch to indicate etch depths with respect to 400 nm electron blocking layer, and 150 nm P-contact region.

2.3 InP Wet Etch

Maintaining the same SiO2 hard mask from the ICP etch, the sample was put in a 1:3 solution of HCL and H3P04 assuming an InP etch rate of 7 nm/sec. A buffered oxide etch was then used to remove the hard mask, based on a referenced witness sample. One final stylus profilometer measurement was used to confirm that the completed mesas did in fact extend from N-contact to the top of the P-contact. Then, to add P-contact points to finished N-mesas, a new lithography pattern was added to the sample, followed by an evaporator deposition of Pt/Au/Ti and ultrasonic acetone bath to complete a standard P-well liftoff process.

Layer #	Material	Thickness	Recipe
1	Pt	0.2 kÅ = 20 nm	40
2	Au	0.5 kÅ = 50 nm	49
3	Ti	0.1 kÅ = 10 nm	38

Table 2.2. P-contact metal evaporation deposition.

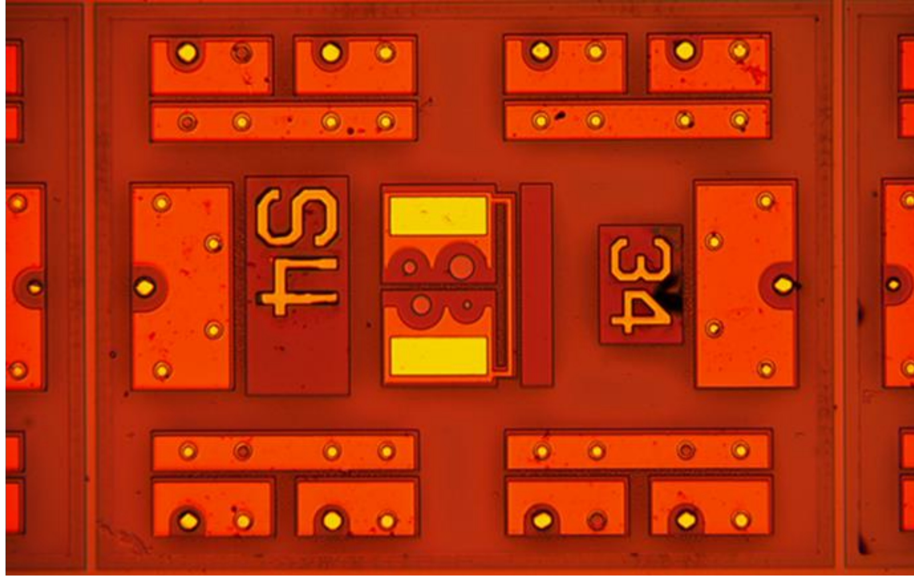

Figure 2.7. Flipped absorber device fabrication after liftoff process for P-contacts.

With the purpose of isolating devices through the substrate and thus reducing unnecessary junction capacitance, a SiO2 hard mask was deposited on the sample, and a third lithography pattern was added to outline the perimeters of each device. Lithography pattern features were again transferred to the hard mask using a F-ICP, and finally a CL-ICP was used to etch around each device into the substrate. Instead of removing this hard mask, contact points were added with an additional lithography pattern, and openings were then formed with a F-ICP. In this manner, the SiO2 hard mask serves as a later sidewall passivation.

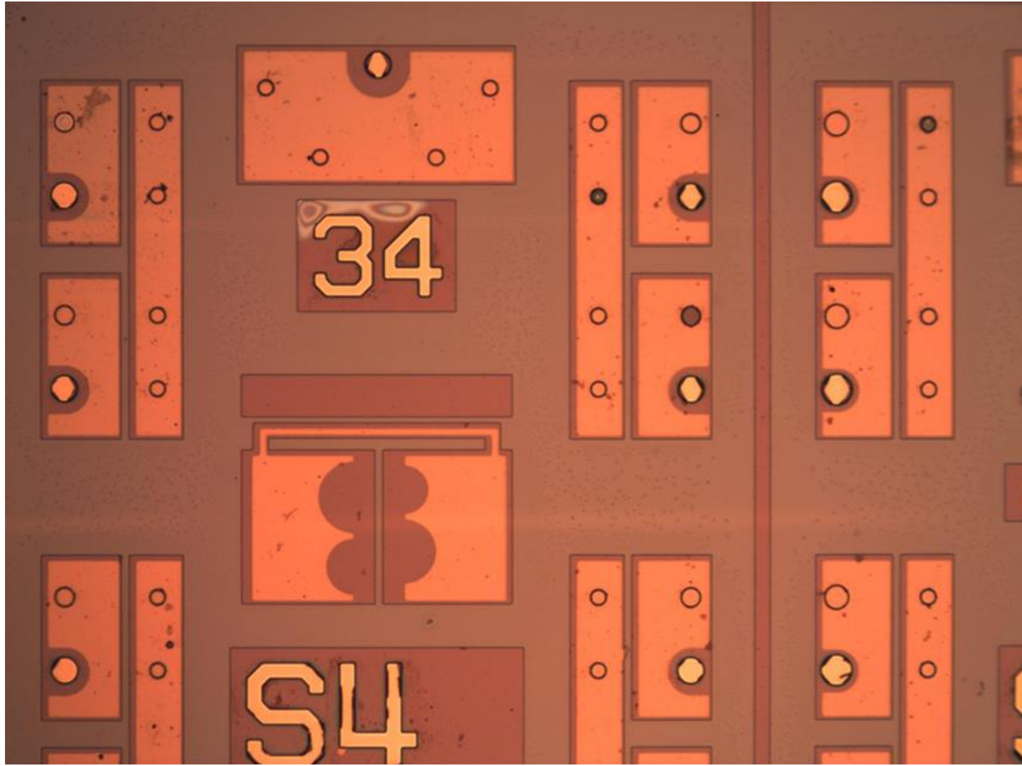

Figure 2.8. Flipped absorber device fabrication after a CL-ICP etch is made around the perimeters of each device.

2.4 Electroplating

To allow for electroplating adhesion, a seed layer of Ti/Au/Ti was first evaporated onto the sample. This seed layer is responsible for forming a complete circuit between the desired points to be electroplated and the anode metal connection placed on the outside perimeter of the sample. Because the sample at this point has surface topology, it is more ideal for an electroplating seed layer to be deposited via sputtering for a more conformal covering. However, an evaporation deposition was found to be suitable.

Layer	Material	Thickness
1	Ti	0.1 kÅ = 10 nm
2	Au	1.0 kÅ = 100 nm
3	Ti	1.0 kÅ = 100 nm

Table 2.3 Electroplating seed layer evaporator deposition.

Figure 2.9. Seed layer for electroplating consisting of Ti, Au, and Ti.

After the seed layer deposition and a Ti etch to reveal gold contact points, it was a challenge to determine a suitable electroplating rate. Electroplating rates are directly proportional to the source current, and inversely proportional to the active plating area. However, the sample's abnormal size and area at this stage made it not directly comparable to any previously plated MUTC sample. To address this problem, a test sample was made on a silicon wafer containing the same dimensions, seed layer, and electroplating lithography pattern as the actual sample. This test sample was then electroplated and measured for rate and height. Based on this information, it was possible to calibrate the electroplating current and time to match the irregular area of the real sample.

Final electroplating parameters of 0.28 mA for 5 hours were used on the real flipped absorber sample, based on the calibration process described above. On this sample, these parameters translated to a plating rate of one micron per hour, yielding a total of 5 microns. Importantly, this particular rate guaranteed a high quality plating, while the total 5 micron height made the bonding pillars correct for the flip chip bonding process. In this bonding process, too little plating height will not allow for a good bond. On the other hand, a plating height that is too high runs the risk of bonding pillars plating into one another and as a result shorting the device.

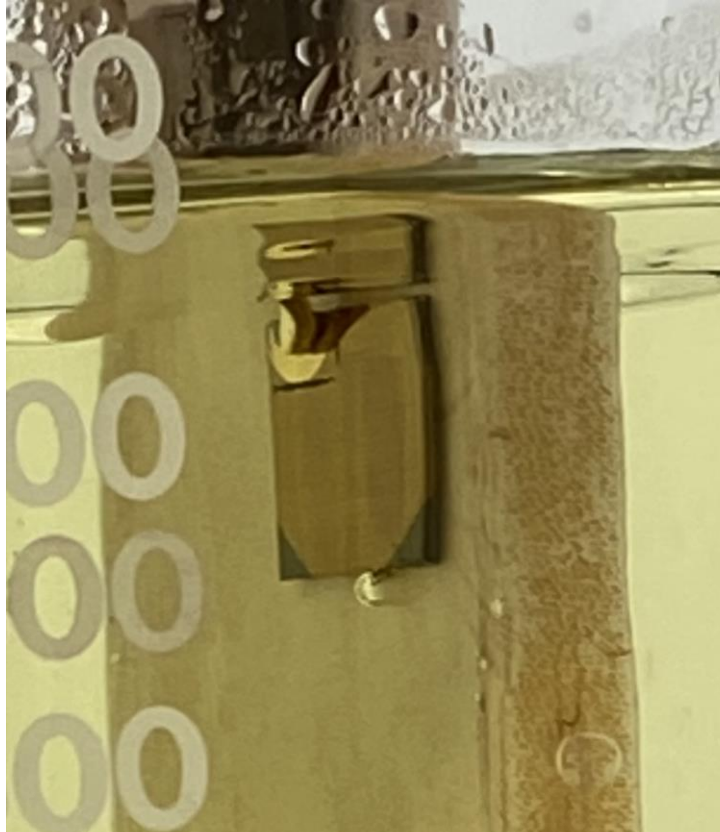

Figure 2.10. Electroplating 5 micron bonding pillars onto the flipped absorber sample. As seen, the gold patch in the top left section forms the anode connection.

Following the completion and measurement of the electroplating heights, the sample had its photoresist and seed layer removed through a series of wet etches. These etches were all timed visually with the importance of never going over the minimum possible metal removal. In the case of the gold seed layer removal etch, going over the minimum required time will result in an unneeded reduction in the gold bonding pillar heights. IV curves were then taken to verify good electroplating adhesion and complete photoresist removal.

Figure 2.11. Completed flipped absorber devices undergoing IV curve testing after electroplating to verify normal functionality.

2.5 Polishing

Essential to the responsivity of MUTC PDs and photodetectors in general is a minimization of scattering and Fresnel reflections on the back illuminated side. A high responsivity is not only essential for high power operation but is necessary for maximizing bandwidth as well. To start in this process, the backside of the sample was cleaned and stripped of any remaining gold from the electroplating process. To accomplish this, a gold etch was applied to the backside, being sure to not allow any onto the gold bonding pillar containing front side.

With a relatively clean backside, the sample had its front side bonded with crystal bond to a holding tool to prepare it for manual polishing. While systems are available to hold and automatically polish samples, the irregular shape and size of this sample made these impractical. With a large grit size polishing pad and coarse polishing solution, the polishing began with the goal of removing any metal and evening out any slope of the InP substrate to a flat surface.

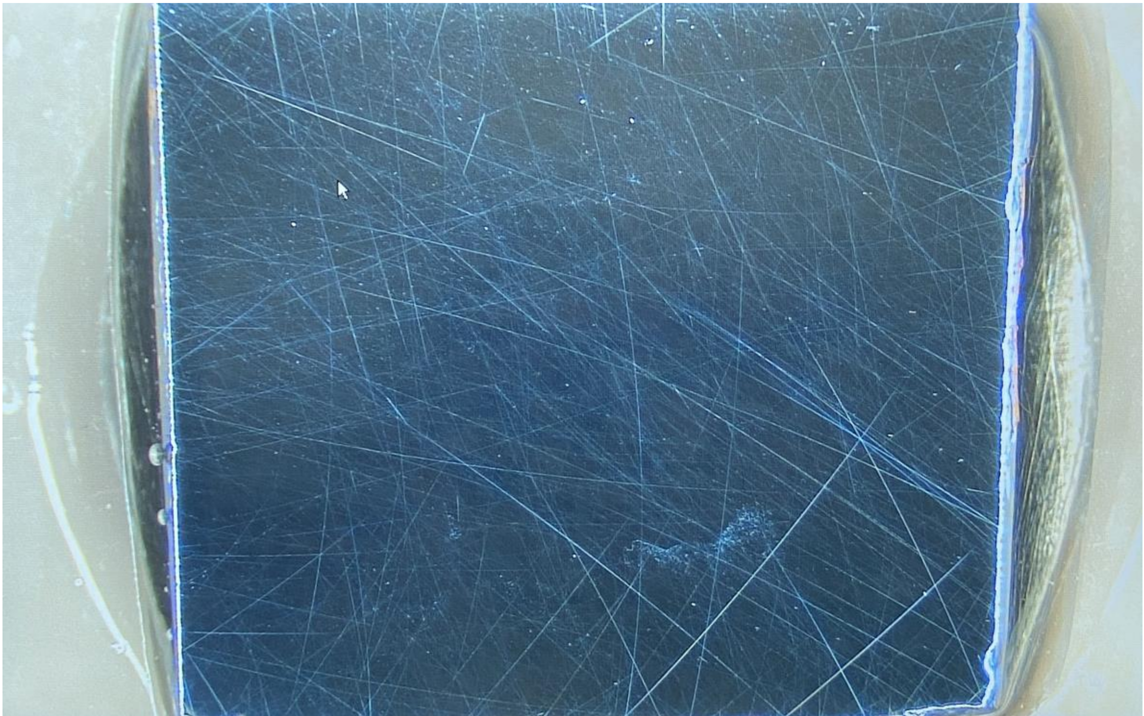

Figure 2.12. Backside polishing the flipped absorber sample.

After an extensive coarse polishing of the sample, the polishing pad and solution were changed to an intermediate grit size only after a microscope view revealed consistent and continuous roughness throughout. A continuous roughness is indicative that the backside of the sample has been polished to the same grit size of the

polishing pad. Using the same visual check, the polishing pad and solution were finally changed to the finest grit size.

With a transition from course to fine polishing complete, the sample was determined to be finished when the backside was entirely black and featureless under a microscope view. To the human eye, this polished backside appeared completely specular to any incoming light. While there are several tools available to characterize surface roughness at this stage, none were deemed necessary.

2.6 Antireflective Coating

$$d = \frac{\lambda_0}{4\eta_1}$$

$$\lambda_0 = 1.55\ \mu m, \eta_1 = 1.444\ (SiO_2)$$

$$d = 0.268\ \mu m$$

Equation 2.1. Thickness of backside antireflective coating.

With the completion of the backside polishing, a loss in responsivity due to backside scattering is mitigated. However, a backside polish will not address a reduction in responsivity caused by Fresnel reflections. These on the other hand can be addressed through a quarter-wave antireflective coating, described in equation 2.1.

A quarter-wave anti-reflection coating works by maximizing destructive interference of light traveling in the reflected direction. At the first air and AR coating

boundary, some relative fraction of incident light will be reflected. Some of the light that continues past this boundary is then reflected on the AR coating and substrate interface. Once this reflected light reaches the first air and AR coating boundary again, it has undergone a 180 degree phase shift because its total path length was two quarters or equivalently one half of its wavelength. This light destructively interferes with that reflected at the first air and AR coating boundary.

To apply a SiO2 antireflective coating, the most important consideration is getting the deposition thickness as close as possible to the antireflection satisfying condition, or in this case 268 nanometers. To ensure a deposition as close as possible to this figure, the deposition was first completed on a bare silicon calibration sample. The deposition on this sample was measured using a spectrometer, and the information was used to fine tune the actual sample deposition time to achieve the desired thickness.

2.7 Summary and Process Improvements

In the process flow covered, the flipped absorber wafer was fabricated into mesa-based backside illuminated photodetectors. Due to the constraints caused by the epitaxies relatively thin p-contact region, which must be the terminating region in these mesas, a combination of first an inductively coupled plasma etch and then a highly selective wet etch were used. Following these two etches, an evaporation and then liftoff process were used to apply the metal contact points at the bases of these mesas to make the second contact points on these two terminal devices.

After the completion of the two terminals on these devices, an inductively coupled plasma etch was used to isolate the devices through the substrate. Instead of removing the hard mask from this procedure, contact opening points were made within

it to turn the hard mask into a sidewall passivation feature. At these sidewall passivation openings, gold bonding pillars were applied on top of device n-mesas and around p-contact mesas to allow these devices to be flip chip bonded. Finally, these devices were backside polished and backside antireflection coated for best optical performance.

Most problematic in this fabrication process was the wet etch used to complete the final portion of the mesas. While the bottom portion of the mesas were etched correctly, there was a noticeable undercut in some top sections of the mesas. With this came along an unfortunate N-contact metal liftoff in some areas. In most cases, only an insignificant portion of N-contact metal came off, but there were some devices which lost all of their N-contact metal at this step.

In addition to the wet etch issues, variance across the sample in etch rate from the CL-ICP used made it more difficult than normal to target the desired etch stop location during the etch down to the electron blocking layer. To address this issue during the fabrication, the sample was rotated mid-way to get a better uniformity. In the future, it may be possible to vary carrier wafer locations or etch recipes to get a better uniformity.

Chapter 3

RESULTS AND CHARACTERIZATION OF DEVICES

3.1 Responsivity

$$R = \eta \frac{\lambda_0}{1.24}$$

Equation 3.1. A photodetector's responsivity in terms of its quantum efficiency and the incident wavelength [7].

The responsivity of these devices, defined as the zero-bias photocurrent per input continuous wave optical power was 0.65 A/W. This figure being similar to responsivities of other MUTC devices [3] would indicate that the 150 nanometer InGaAs P-contact region does not absorb enough optical power to be problematic. Additionally, the photocurrents attainable with this high responsivity guaranteed that these devices are not bandwidth limited by high transit times.

To measure responsivity, the flipped absorber chips were first flip chip bonded to aluminum nitride submounts and had their antireflective coatings cleaned with isopropanol. A low power 1.55 micron laser was measured using a calibrated power sensor to get its optical power level. Then, the flip chip bonded chips were placed underneath the fiber coupled laser on a three dimensional *x,y,z* adjustable stage.

With zero bias applied, a RF probe was put in contact with the submount coplanar waveguides to make contact with the device. With the current through this

coplanar waveguide being displayed on a source meter, the adjustable stage was moved arbitrarily until any noticeable current was measured on the source meter. From here, the several cycles of stage adjustment were made in each axis moving from x to y to z. After a relative maximum current was found in one axis, the next axis would then get maximized in the same way.

After several cycles of maximizing current in each axis, the process was stopped upon reaching a photocurrent on the source meter that could not be improved upon. This current level was then divided into the previously recorded laser optical power to give the responsivity stated above. As expected, there was a variance in responsivity from device to device, with the worst device having a value approximately 85% of the maximum, coming in at 0.55 A/W.

Earlier in the fabrication process, several flipped absorber devices were measured for responsivity before the polishing process and without an antireflective coating. At this stage, 28 micron devices were seen to have a responsivities of 0.05 A/W and bandwidths of 9 GHz. This test, which was conducted to give a general confirmation of photodetection reveals two interesting and important details of MUTC photodetectors.

First of all, this test demonstrates that reasonable optical coupling for backside illuminated MUTCs is not possible without the addition of polishing and antireflective coatings, considering the difference in responsivity is more than a full order of magnitude. Second of all, this demonstrates the fact that MUTC bandwidth has a massive dependency on photocurrent. At a responsivity of 0.05 A/W, it was not possible to get sufficiently high photocurrents, and for this reason the bandwidth

suffered. As will be demonstrated later, 28 micron devices with full responsivities had bandwidths much higher than 9 GHz.

Having a reasonably high responsivity is important in MUTC photodetectors for a variety of reasons, even though the focus of this work was power handling. As mentioned above, without a high enough responsivity for larger photocurrents, bandwidth suffers because of a increase in transit time. In addition to this, a low responsivity photodetector can never be a high power photodetector because there are always power limitations in fiber optic cables, meaning that the electro-optic conversion (responsivity) must be high to get high RF outputs. Lastly, even if no optical power constraints applied to fiber cables in a link, a photodetector with low responsivity would never allow the link to achieve a good link gain figure.

A responsivity of 0.65 A/W is consistent with UVA's model which first predicted exactly this figure. For this reason, it is unlikely that flipped absorber MUTC PDs in their current epitaxy could achieve better than this through fabrication changes such as improvements in the polishing process or the antireflective coating. When at the point where the simulated value matches the measured value, it is safe to conclude that Fresnel reflections at the photodetector's backside surface are insignificant.

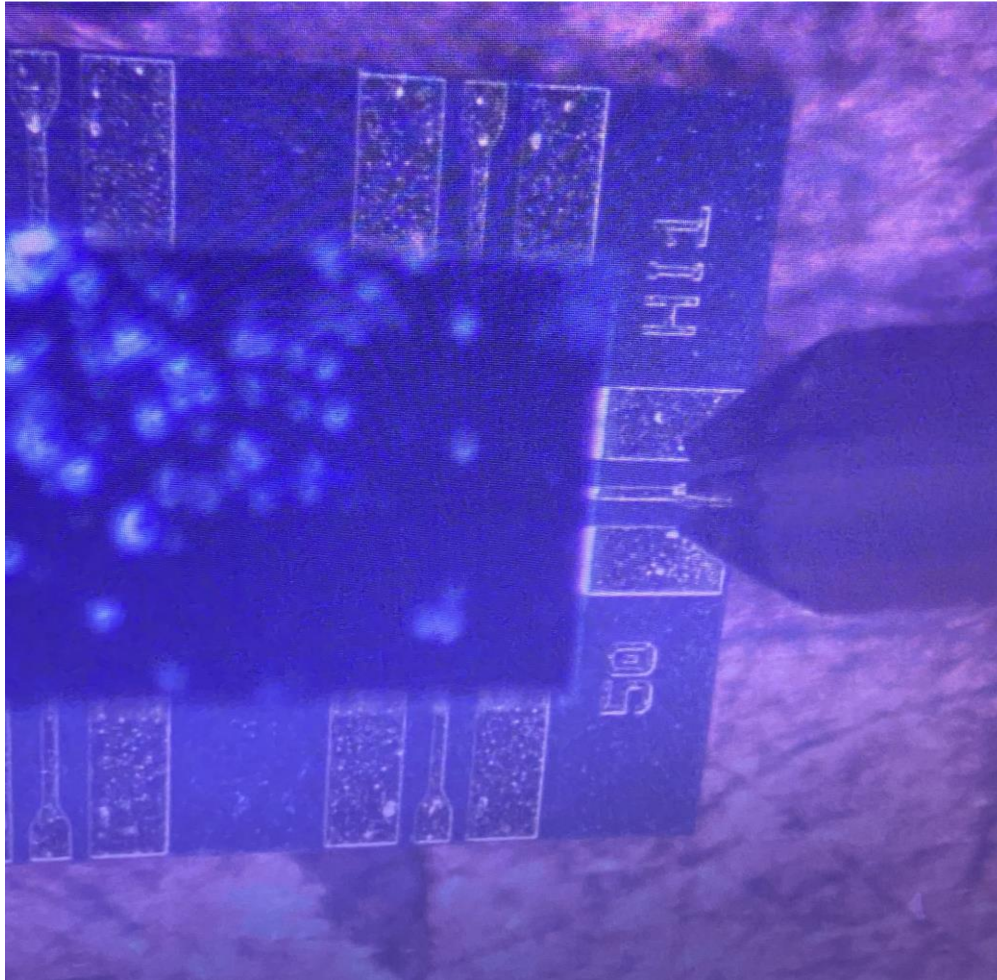

Figure 3.1. Flipped absorber chip is flip chip bonded to an aluminum nitride submount for optical testing. A radio frequency probe (right) touches the rightmost coplanar waveguide on the submount to test the rightmost device on the chip.

3.2 Bandwidth

For bandwidth measurements, two 1.55-micron lasers with independent temperature control were heterodyned by being set at slightly different temperatures and then combined over fiber. This temperature difference translates to a frequency offset that makes the lasers constructively and deconstructivity interfere at a difference

(beat) frequency. The 3 dB bandwidths for 22, 28, and 40 micron devices were 19, 17, and 10 GHz, respectively.

$$I(t) = I_1 + I_2 + 2\sqrt{I_1 I_2}\cos\,[2\pi(v_2 - v_1)t]$$

Equation 3.2. Intensity of two interfering monochromatic waves of different frequencies. The phenomenon is often referred to as optical mixing or optical heterodyning.

To measure bandwidth, the photodetectors were first checked to verify responsivity using the method described earlier, where their zero bias current is maximized under a source of known optical power. After doing so, the chips were left aligned at their positions of 100 percent response. Next, the low power source was replaced by the two lasers mentioned above, which were routed first through an EDFA (erbium doped fiber amplifier) and then connected to the same fiber termination previously aligned to a 100 percent response.

With the high power EDFA amplified lasers now aligned to the chip, a 5 volt reverse bias was applied using a bias tee, which isolates the DC bias from the RF output of the device. A photocurrent was then set to 50 mA at a beat frequency of 1 GHz using a laser controlling LabVIEW program. To obtain a set photocurrent, this program applies a baseline optical power, measures the photocurrent, and adjusts the optical power through a feedback loop until the set photocurrent is reached. To obtain the desired beat frequency, the program controls the TEC coolers on the two lasers. When the user inputs a beat frequency, the temperature of one of the lasers is adjusted, which changes its frequency relative to the second laser. This temperature is adjusted

through a feedback loop until the laser has a frequency offset relative to the first laser which matches the user's input beat frequency.

At a photocurrent set to 50 mA and a beat frequency set to 1 GHz, a new LabVIEW program was used which held the bias voltage and photocurrent level constant, while cycling the laser beat frequency continuously from 1 GHz all the way up to 20 GHz. While this occurred, an RF power meter connected to the chip through the bias tee recorded RF output power. This RF output power in conjunction with the frequency range tested are what define the frequency response reported, with the addition of a normalization factor.

As mentioned previously, photocurrent levels have an effect on bandwidth, as do biasing levels, which is why the bandwidth tests described above were repeated several times in a test matrix of various photocurrents and bias voltages. All of the devices tested required bias voltages and photocurrents much higher than the baseline 50 mA and 5 V to give their best frequency response. In the case of 28 micron devices, the best photocurrent and bias combination was 70 mA and 10 V, leading to the reported 3 dB bandwidth of 17 GHz.

In comparison to the frequencies typically obtainable for MUTC PDs, ranging all the way to 110 GHz [6], these results are certainly low. The limits in high frequency operation primarily come from the high series resistances seen in these devices, which will be more completely explained in the next section. Unlike responsivity, the low frequency characteristic of these devices is not critical to the goal of this project, which was high power operation.

While the lower frequency characteristic of these devices comes from their series resistance, it is worth noting that the flip chip bonding process does have a

minor impact on how ideal (flat) the frequency response was within these bandwidths. Because the flip chip bonding process includes a metal on metal bond, it is easy for such a bond to add unwanted capacitance. Earlier in the bandwidth testing process, bonding parameters with lower force, temperature, and time were used, which lead to several peaks at dips at low frequencies. Simply by increasing these three bonding parameters, the response flattened. For this reason, it would make sense for flipped absorber devices to eventually have their own dedicated flip chip bonding process.

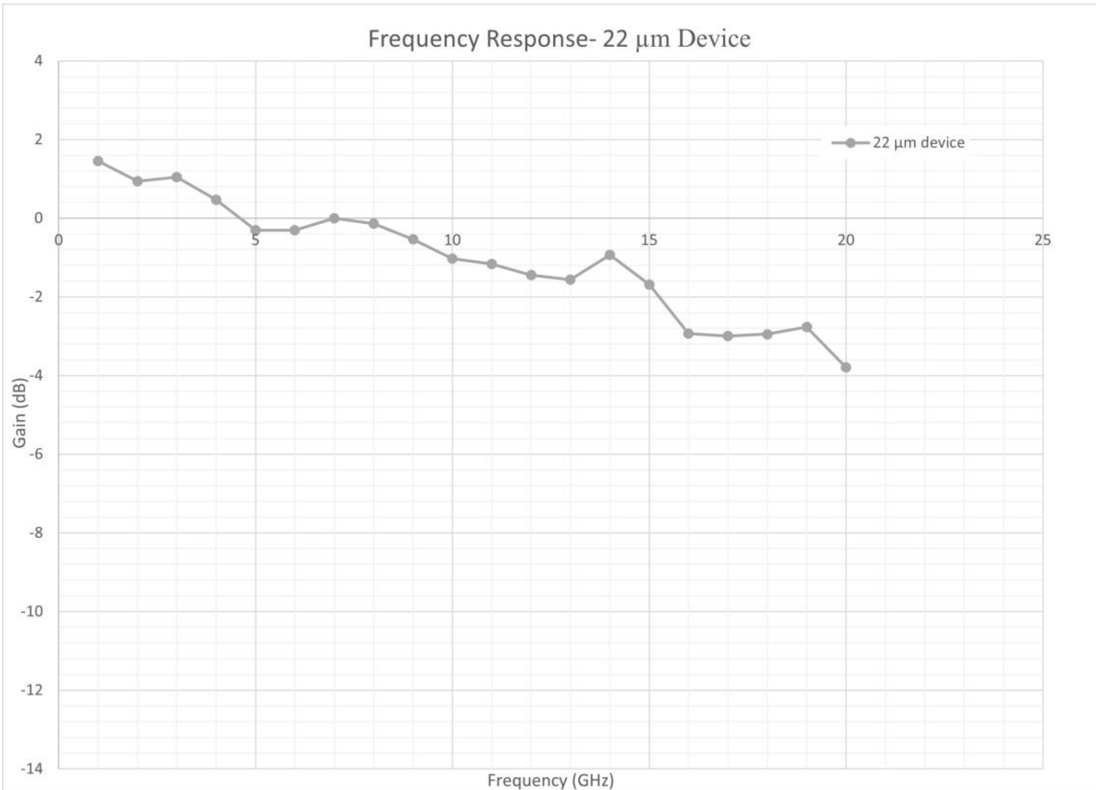

Figure 3.2. Frequency response for a typical 22 μm device.

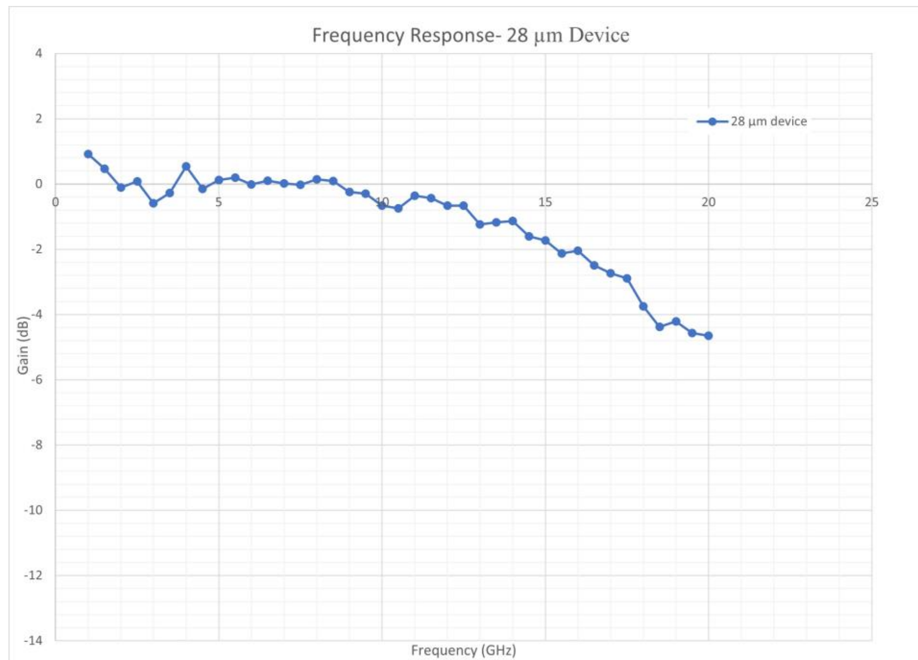

Figure 3.3. Frequency response for a typical 28 µm device.

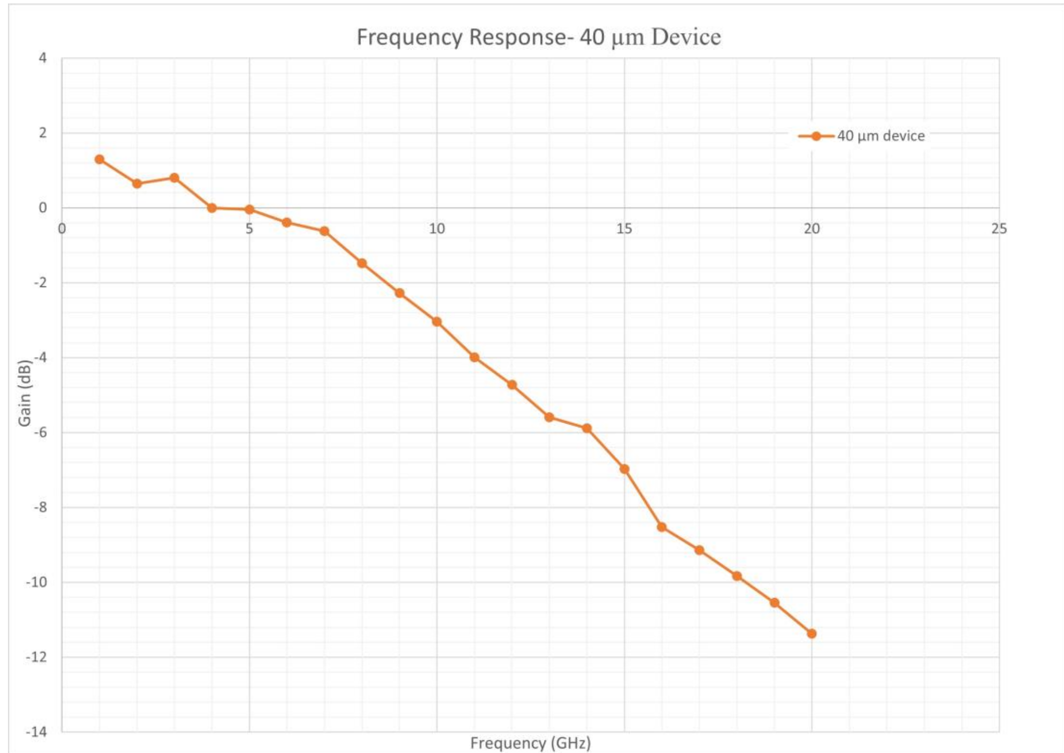

Figure 3.4. Frequency response for a typical 40 μm device.

3.3 Dissipated Power

In terms of impact factor, the dissipated power of these devices at their failure point is the most important, as it determines whether or not this epitaxy has the improved thermal properties that UVA's simulations predicted. Dissipated power at failure is defined as the bias voltage multiplied by the photocurrent that the detector operated (unsaturated) at before the occurrence of any damage to the device. The dissipated powers of these devices at failure are shown below, compared against record dissipated power figures for MUTC PDs from UVA [3]. As seen, these figures are very comparable, especially for the smaller device sizes.

Device Size (μm)	Bias (V)	Photocurrent (mA)	Dissipated Power (W)
22	13	50	0.65
28	10	102	1.02
40	15	100	1.5

Table 3.1. Flipped absorber dissipated power records (TEC cooled).

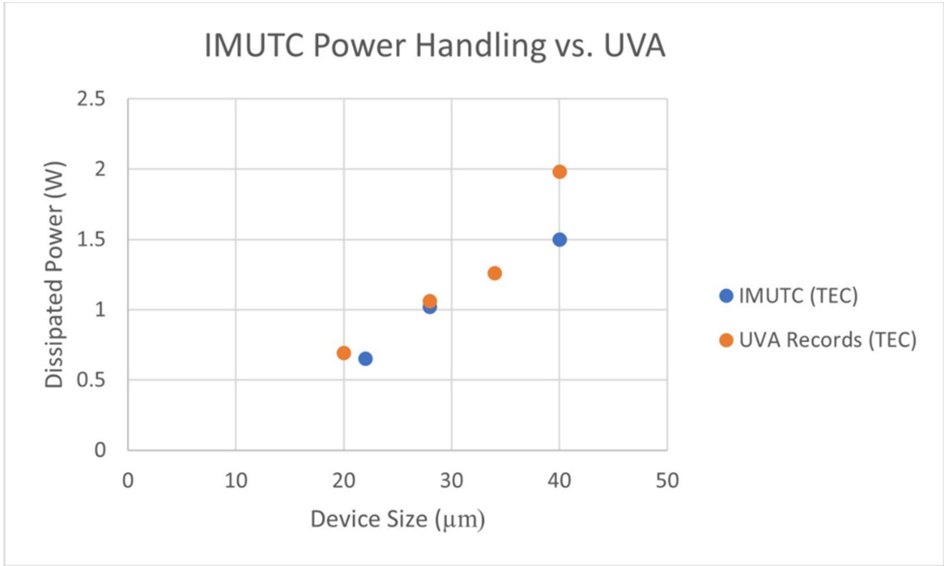

Figure 3.5. Flipped absorber devices a.k.a. inverted MUTC (IMUTC) are compared against various literature released from The University of Virginia for general MUTC dissipated power records. All of tests presented were done using thermoelectric cooling (TEC).

To measure dissipated power, the devices were first checked for responsivity and bandwidth using the methods described earlier. Then, the standard chip stage was replaced with a thermoelectrically cooled stage. Because backside hot spots tend to cause premature failure in MUTC PDs, the chips were then aligned to a responsivity of 50 percent their maximum value. To accomplish this, the chips were first aligned to a 100 percent response, and then were backed out to 50 percent only using height adjustments. By defocusing to 50 percent only in the z axis, it was guaranteed that no hot spots were formed on the backside. Additionally, a heat sinking paste was applied in between the base of the chip submount, and the TEC surface.

With the chip aligned at 50 percent responsivity on top of the TEC, it was then critical to fully enclose the testing area and fill it with nitrogen gas. At the TEC operating temperature (-10 C) any water in the air will condense on the TEC surface and thus the device itself. For many reasons, including shorting testing equipment and shorting the device itself, this cannot happen. Nitrogen on the other hand will not condense, which is why filling the entire testing area with it solves all of these problems. After making sure that the entire testing area was filled with nitrogen instead of air, the TEC was then set to -10 C and the test was started.

To most accurately measure the best obtainable dissipated power, a new LabVIEW program was used which gave the ability to hold the laser beat frequency constant while continuously increasing photocurrent and thus RF output power. This was accomplished by putting a variable optical attenuator (VOA) in line with the EDFA. After the EDFA and thus optical power is set, the lab view program steps through from maximum attenuation to no attenuation, giving nearly continuous increasing photocurrent.

With a reverse bias set to 5 volts, the LabVIEW program kept the beat frequency to 1 GHz and then continuously decreased the VOA attenuation to give a ramp in photocurrent. For the first testing, the photocurrent was ramped from zero to 50 mA, while RF output power as a function of photocurrent was plotted. Checking this plot, it was easy to see whether saturation was occurring at the high end of photocurrent. If saturation occurred, the test would then get redone with an increased bias voltage. If no saturation occurred and the device had not been degraded, the test was redone with the same bias voltage and an increase in final photocurrent. This cycle, which gradually increases dissipated power, was continued until permanent damage to the device was observed.

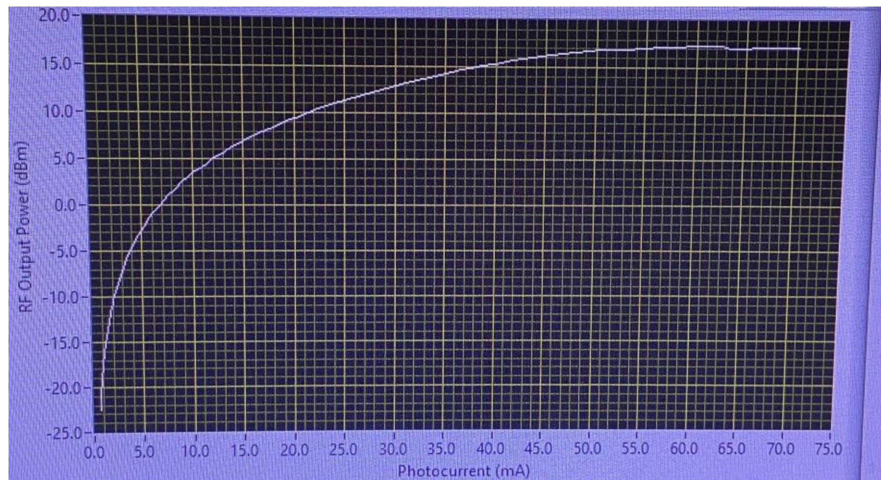

Figure 3.6. Device becoming saturated at high photocurrents during dissipated power testing.

After many cycles of increasing bias voltages and photocurrents as described above, a dissipated power figure was determined by checking for which cycle the detector operated unsaturated at with the highest combination of photocurrent

multiplied by bias voltage. As such, a combination of photocurrent and bias voltage that included saturation or device degradation was not counted. These are the figures reported in figure 3.5.

In terms of improvements that could be made to this measurement of dissipated power, the main issues came from complications associated with the TEC and nitrogen environment. Even with precautions taken to seal the test environment away from the exterior air, there were still many occurrences where condensation was able to develop on the device. When this happened, the devices were damaged very quickly, and the data was invalidated.

As mentioned previously, all dissipated power figures reported previously involved tests that were completed at 50 percent responsivity. Although this was the normal procedure throughout the testing, several devices were also tested for dissipated power at 100 percent responsivity. Doing so revealed an interesting characteristic of these devices, in the fact that their dissipated power was unaltered. An unaltered dissipated power tolerance suggests that these devices were not failing from backside hotspots and must have had a different damage mechanism. This is consistent with understanding that these devices are dissipated power limited by the series resistance of their P-contacts, which will be discussed later.

3.4 Dissipated vs. RF Output Power

While dissipated power at failure best summarizes the thermal performance of these devices, it is not dissipated power, but instead the power delivered to an external load (RF output power) that truly describes the usefulness of these devices. These devices required much higher bias voltages than are typical to remain unsaturated, meaning that the RF output power (proportional to current squared) was never as high

as the dissipated power (bias voltage multiplied by current). This unfortunate problem of these devices comes from the fact that they have high series resistances, which increases their minimum bias condition.

In comparing flipped absorber devices to record devices from UVA, flipped absorber 40 micron devices failed at a 15 volt bias, 100 mA of photocurrent, leading to 1.5 W as seen above. 40 micron devices from UVA failed at an 11 volt bias, 180 mA of photocurrent, leading to 1.98 W of dissipated power [3]. In comparing these figures, it is seen how flipped absorber series resistance translates to an undesirably high biasing voltage requirement.

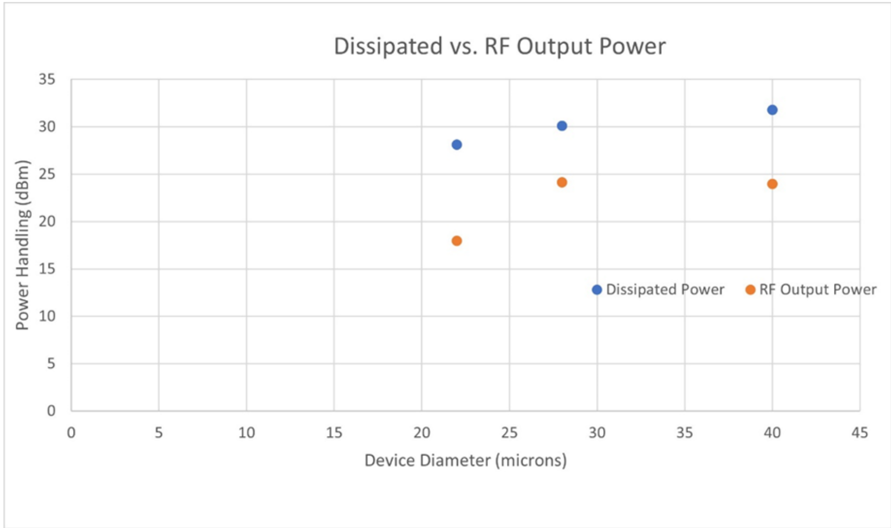

Figure 3.7. Dissipated power records for flipped absorber devices are compared with their corresponding RF output powers at the dissipated power record photocurrents. As seen, dissipated powers are significantly higher than the RF output powers, because dissipated powers take into account a high bias voltage.

3.5 Series Resistance

In terms of series resistance, this quantity was defined by looking at the device resistance under forward bias and making a linear approximation in a region beyond

the turn on voltage, i.e. between positive 1 and 3 volts. The lowest series resistance devices were 40 microns in diameter with contact separations of 10 microns, leading to a resistance of 35 ohms. 40-micron diameter devices with 20 micron contact separations had resistances of 76 ohms, which clearly demonstrates that the resistance of these devices comes from the sheet resistance of the P-contact region, and not from high contact resistance. High contact resistance would not explain the short separation devices having roughly half the resistance of long separation devices.

Besides the inherent sheet resistance of the flipped epitaxy's p-contact region, there are several other possible ways that MUTC PDs can take on series resistance. A few of these include metal contacts with added resistance, poor metal deposition during the application of these metals, and contamination. While it is difficult to point to an exact cause, the flipped absorber samples did take on added series resistance somewhere in between their second contact metal deposition and the finished device characterizations. A minimum of 35 ohms for 40-micron short separation devices was increased to a minimum of 45 ohms.

To address this issue of added series resistance, these devices were put in a rapid thermal anneal system containing a nitrogen environment for one minute at 400 C. After this, it was observed that the devices were immediately restored to their original series resistance, i.e. a minimum value of 35 ohms. After this restoration, no other additional tests or experiments were carried out.

Because of the fast and easy improvements that is has shown, it would be wise to incorporate systematic series resistance checks and rapid thermal annealing in future fabrication of flipped absorber devices. For a device where series resistance is

so dominating, these checks become very significant. Additionally, as demonstrated, this quantity can vary significantly across the various fabrication processes.

In terms of varying contact metals, there are possibilities in terms of using a gold germanium alloy as a replacement to the platinum and gold n-contact layer that was previously used. Lower resistance may be attainable with this option. However, there are significant risks to this change. Because this process uses an InP wet etch during the mesa formation step, it is difficult to predict what the impact will be in this step from changing the n-contact metal. The risk of having a liftoff or other complications from the changed contact metal most likely outweigh the benefits of a marginal contact resistance decrease.

In regards to metal deposition quality, it is unlikely that any poor deposition is responsible for the observed series resistance. Often times, a anneal after a deposition can lower contact resistance due to a change in grain structure that happens at the elevated anneal temperature. However, as discussed, after an anneal was performed on these devices the series resistance only was reduced back down to the baseline level, and not lower. Had the series resistance gone below the first observed values, it would have been more indicative of a poor contact metal deposition.

3.6 Dark Current

The dark current, also referred to as the leakage current, is an important quality to a PD meant for high power applications in the way that it causes additional joule heating that is not necessary for the detection of the radio frequency signal within the modulated illumination. For MUTC PDs, and for InGaAs based detectors in general, the minimum reported dark current of 5 nanoamps is low. Dark currents must be compared against devices of the same absorber material, because it is the bandgap of

such a material that ultimately determines the relative quantities of electrons in the valance and conduction bands band at a certain temperature.

To test the device dark currents, the devices were probed with DC probes connected to a DC voltage source controlled by a LabVIEW program. Input into this program was a range in reverse bias values that were cycled through by the source meter. Precise micro positioners and a microscope assembly connected to a digital camera giving a live view made this possible. Additionally, this system was used to determine quantities such as the turn-on voltages and the forward resistances.

An interesting characteristic of these devices was that their low dark currents made it possible to see the effect of ambient lighting in the test environment. For a MUTC with dark current in the order of microamps, the quantity of ambient lighting at 1.55 microns is so insignificant that it will not make a noticeable impact on the devices observed dark current. However, in the domain of nanoamp dark current, ambient light becomes significant enough to see a noticeable impact. In other words, the photocurrent produced by ambient lighting sits above the noise floor of the detector, and the user is no longer actually measuring dark current.

To solve the problematic issues of ambient lighting, dark current measurements were performed in a room with no overhead lights and no microscope illuminator. This being said, not every source of ambient photocurrent could easily be addressed. If a user wanted the most accurate measurements of dark currents for these devices, more considerations would have to be made to the experimental setup.

In terms of the attributes that flipped absorber samples have that cause them to have low dark current, the most significant is their series resistance. Supporting this is the fact that the most resistive devices (22 micron) had the lowest dark currents, while

the largest least resistive 40 micron devices had the highest dark currents. Another aspect of these devices that may have aided this characteristic is the InP wet etch, which may have had a sidewall smoothening effect on the already mainly formed n-mesas.

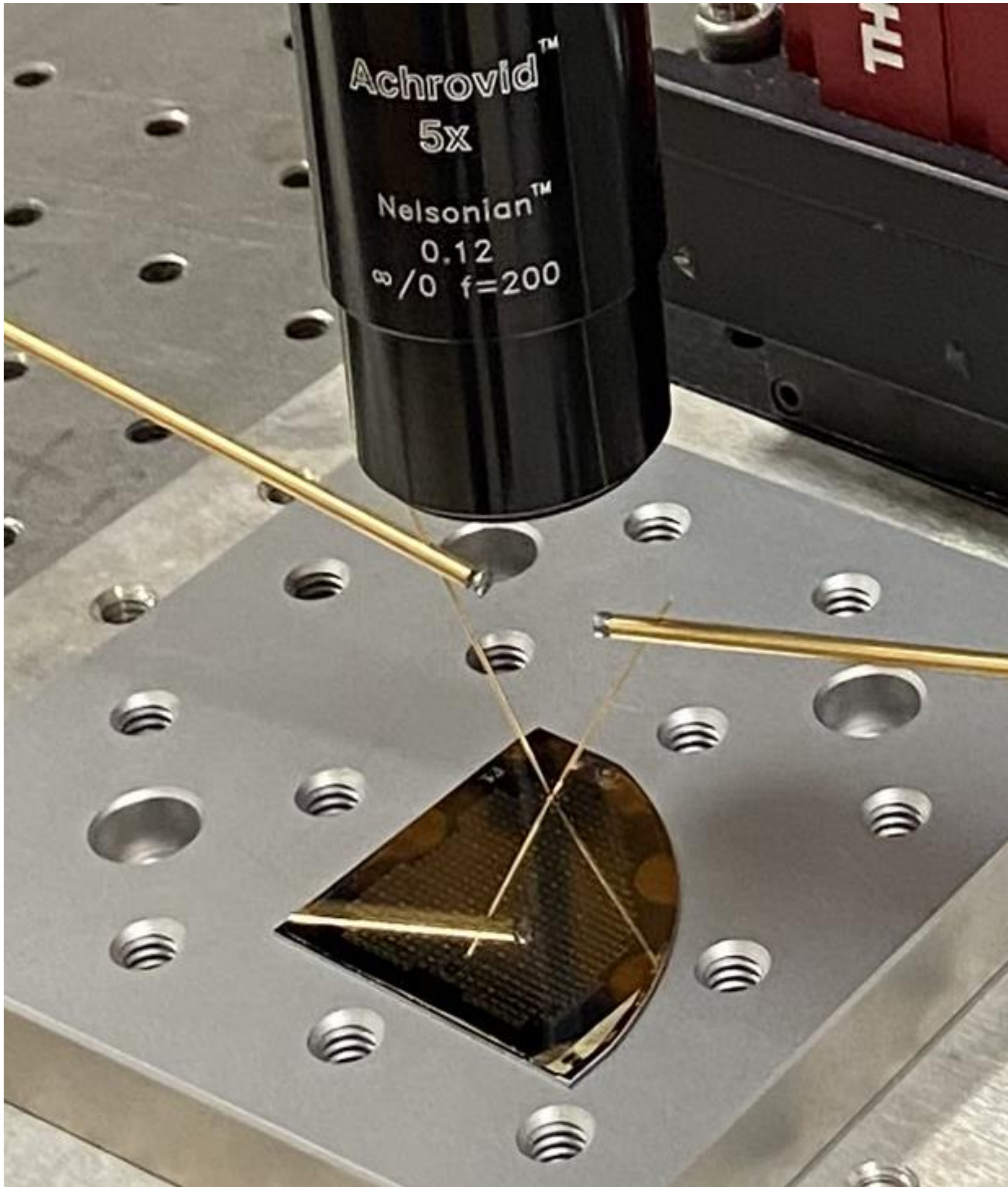

Figure 3.8. Testing flipped absorber devices for dark current.

Chapter 4

POTENTIAL IMPROVEMENTS IN DEVICE DESIGN

4.1 Device Improvements

To improve performance in these flipped absorber devices, the most important change would be to make the contact separation as low as possible. As mentioned previously, the series resistance of these devices is mainly dependent on contact separation, and series resistance is the biggest problem for device performance. A lower series resistance would lead to better dissipated power by reducing joule heating within the epitaxy, greater RF output power for the same dissipated power (by virtue of lowering minimum bias condition), and additionally would increase bandwidth by lowering device RC time constants. The only downside of reducing device resistance would be a marginal increase in dark current, which is currently as low as 5 nanoamps at -5 volts.

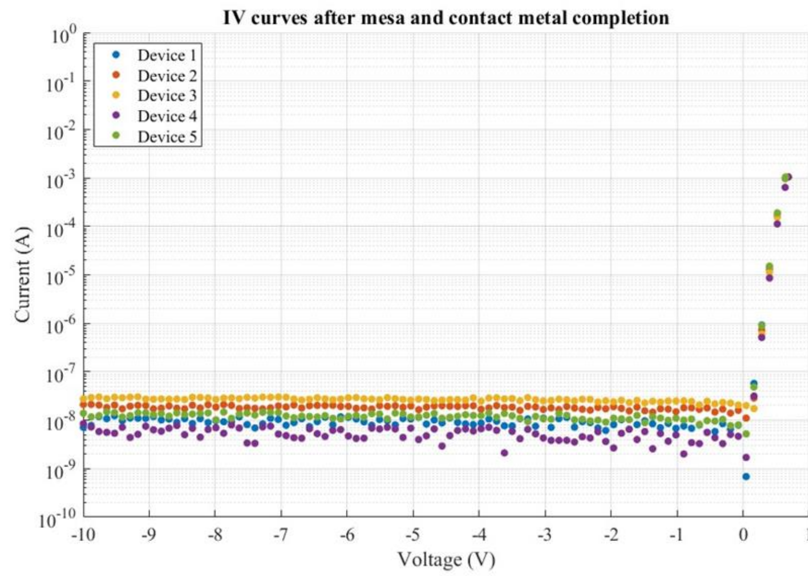

Figure 4.1. Dark currents are compared for 5 different flipped absorber devices. As seen, a typical dark current was around 10 nanoamps, with the best ones being as low as 5.

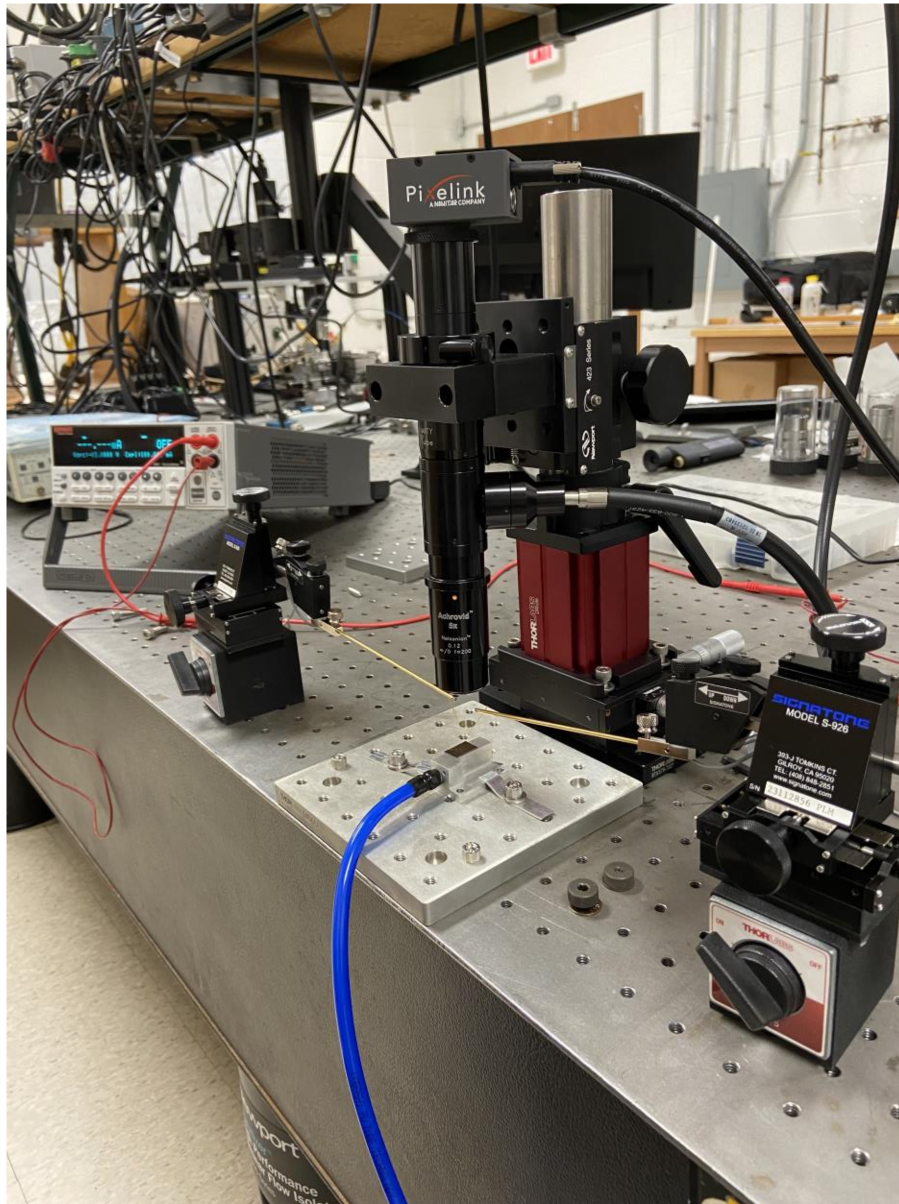

Figure 4.2. DC probing station used for measuring device dark currents which consists of a source/meter, microscope with CCD camera, DC probes, micro positioners, and a vacuum stage.

To make a reduction in contact separation, it is likely that alignment during fabrication steps will become a factor. A contact separation of 5 microns (as opposed to 10) should be easily attainable with contact lithography methods. However, to

achieve a contact separation as low as 2 microns, it is more desirable to use a laser writing system that has an automatic alignment feature.

In addition to contact separation reduction, it would be advantageous for future flipped absorber devices to have a larger P-contact metal area. During operation, the P-contact metal sinks heat from the P-contact epitaxial region into gold bonding pillars, which then sinks it into the submount. Because the P-contact epitaxial region undergoes significant joule heating in these devices, it is ideal for the P-contact metal to form a large area connection. Doing so should have a positive impact on dissipated power tolerances.

4.2 Future Design Introduced

In figure 4.4 below, the flipped absorber device design used in this work is shown. In figure 4.5, a new design is proposed that includes all of the added improvements that have been described above. For the current epitaxy, this improved design has the best chance of success.

First of all, it can be observed that the separation between the orange p-contacts and the blue n-mesa is reduced from 10 microns to 2 microns between the used design and the new proposed design. As mentioned previously, the problematic series resistance of the flipped absorber devices has been shown to be a sheet resistance property of the p-contact region. Therefore, the resistance of this region is linear function of the device distance across it. Reducing this distance by 80 percent will also reduce the device series resistance by approximately 80 percent.

In addition to contact separation reduction, it is seen in this new design that the p-contact (orange) is significantly larger. In the finished device, this orange region defines an area of metal that sits directly on top of the p-contact epitaxial layer.

Because the p-contact epitaxial layer experiences the greatest joule heating of any region in these devices, having a wide area heat sinking pathway is more ideal. This size increase does not have any significant setbacks in terms of device performance.

In the same way that an increased p-contact area improves heat sinking, the addition of more bonding pillars seen in the new design also makes an improvement. During fabrication, these bonding pillars start off as n-mesas just like the center n-mesa. The later electroplating step then completely covers them on all sides, which allows them to be shorts to the p-contact metal. These gold pillars become the connections between heat sinking submount and the p-contact metal, which is why it is ideal to have many of them.

The last two components seen in the two drawings are the enclosed circles for the contact opening etch and the electroplating. No significant additions were made in these two areas, which are more motivated by fabrication considerations than by actual device performance. Both drawings are consistent in the fact the electroplating stays inside the n-mesa area to avoid shorting and goes outside and around the dummy mesas to form larger bonding pads. They are also consistent in the manner that the opened contact points must sit inside the n-mesas to allow for sidewall passivation, where in the case of the dummy mesas it is possible to have them larger.

In terms of fabrication considerations of this new design, the most significant component is the alignment of the p-contact within what will be an already formed n-mesa. A separation of 10 microns gives a large tolerance for alignment inaccuracy. 2 microns on the other hand does not. While a 2 micron alignment may be difficult through the use of contact lithography, automatic alignment systems exist for common laser writing systems.

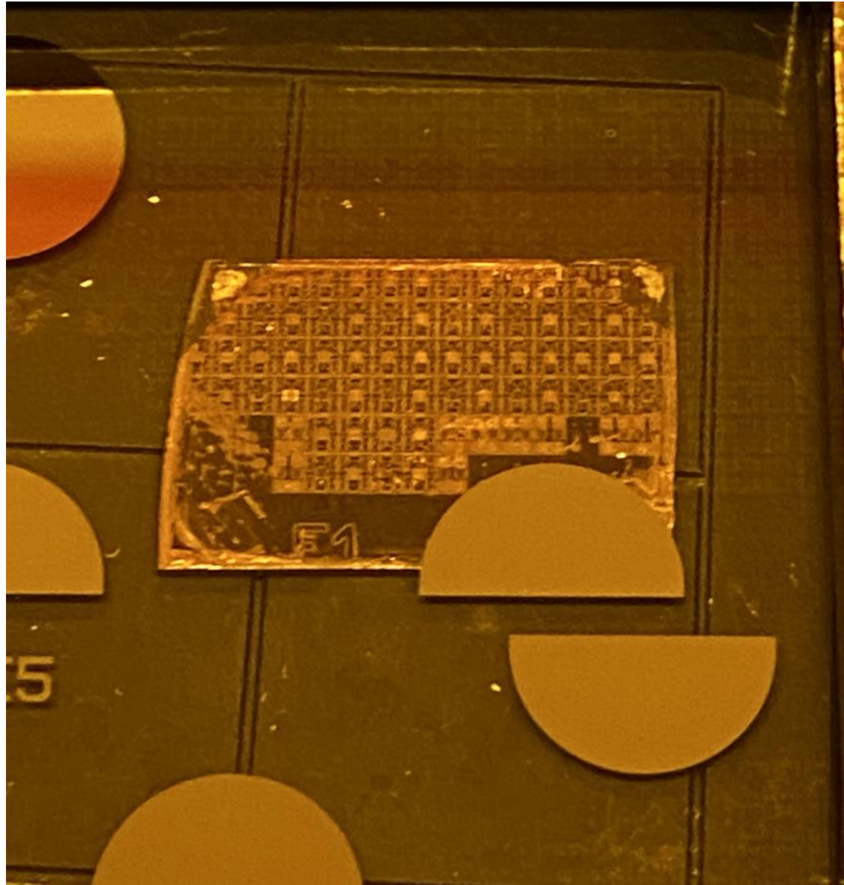

Figure 4.3. Flipped absorber sample during normal contact lithography alignment.

In a worst case scenario, some of the devices will become shorted in this step because their p-contact metal touches the n-mesa. While this may be an issue in terms of yield, the asymmetry of mask designs means that not all devices can be misaligned in the same way, and some will not be shorted. Thus, this may be a possible production problem, but will not likely be a research problem. In summary, other than the discussed p-contact alignment considerations, this new mask will follow the same general process flow as before, and for this reason it is unlikely that there will be any new complications introduced.

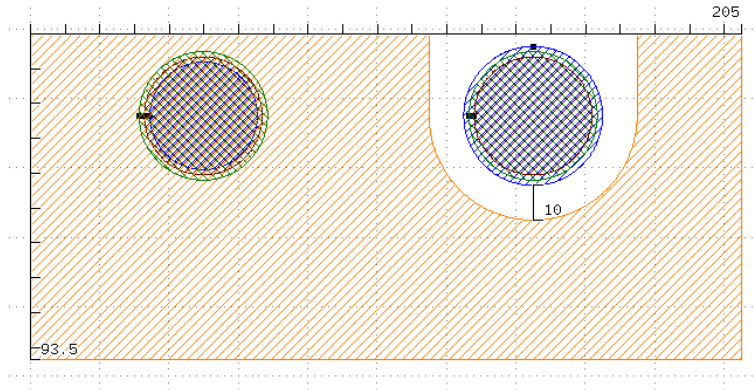

Figure 4.4. Flipped absorber 40 micron design (top down view) used in this work. N-mesa is indicated by the right blue circle, which sits inside a rectangular p-contact (orange). As seen, the separation between the two is 10 microns, and the p-contact dimensions are 205x 93.5 microns. The black and green circles around the two mesas show the locations of the contact opening etch and the electroplated pillars, respectively.

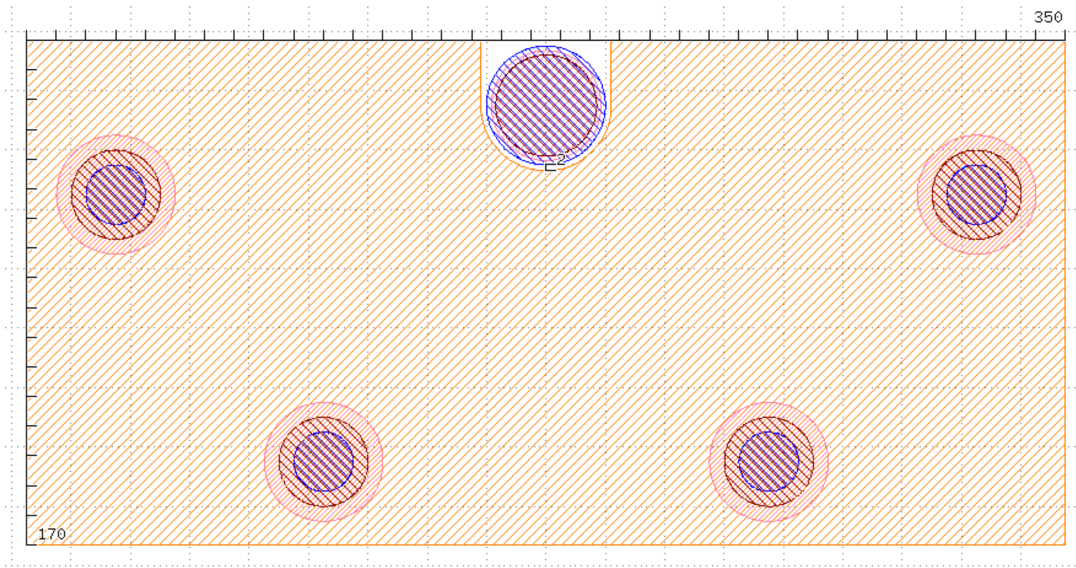

Figure 4.5. Improved flipped absorber 40 micron design (top down view) including a contact separation reduced to 2 microns and a p-contact area increased to 350x170 square microns. Additionally, it can be seen that this design includes three additional electroplated bonding pillars, which will help in heat transfer to the submount.

4.3 Sidewall Passivation

One final consideration for flipped absorber device improvements would be an upgrade in sidewall passivation material. At first glance, sidewall passivation is simply a dielectric mesa protectant to keep out contaminants and maintain device structure. However, previous testing on MUTC devices as will be detailed below has shown that mesa sidewalls are often a failure point under high power levels and high temperatures. For this reason, it would be ideal for flipped absorber devices to eventually use a sidewall passivation with improved thermal properties over the standard silicon dioxide, such as silicon nitride.

In this experiment, six standard MUTC PDs had their IV curves checked to verify typical operation. Then a forward bias was applied and continuously increased to each. Routinely throughout this increase in forward bias, the device IV curves were checked for an increase in dark current. At the point where the device's dark current reached or exceeded 5 mA at a -5 V bias, the forward biasing step was ended. These devices were understood to have been damaged thermally due to the excessive joule heating caused by the high forward bias current.

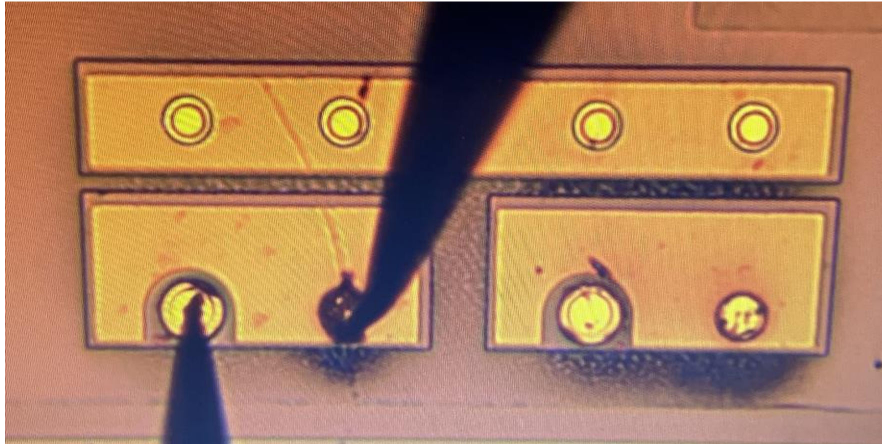

Figure 4.6. MUTC PDs damaged from excessive forward current.

Next in this process, the devices had their silicon dioxide sidewall passivation removed with a HF containing Buffered Oxide Etch. The IV curves were checked again, to reveal that no difference had been made. Finally, the devices were put in a weak piranha solution for 100 seconds, with the goal of removing a small section of InGaAs sidewall in this time period. What was discovered after this step was that the device IV curves returned to their original dark current levels, if not lower. A comparison of the IV curves at each stage of this experiment for one of the tested samples is shown below.

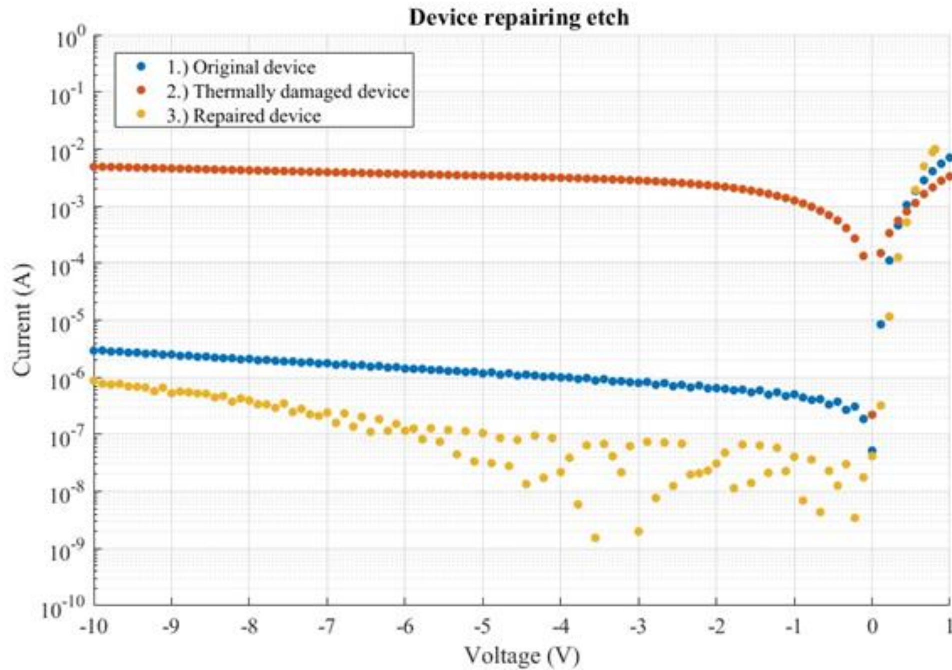

Figure 4.7. A MUTC PD's IV curves are compared from its original state to a thermally damaged state to a repaired state.

A reasonable conclusion from this experiment is that if removing a small section of InGaAs sidewall from the PDs has a repairing effect, then the thermal damage that occurred to the PD must have been located in the sidewall. Diffusion of a contaminant or the formation of an unwanted compound in the sidewall are both possibilities for the exact damage mechanism. Whether it is the first or the second, it is clear that the sidewall passivation must have some role.

Although the exact damage mechanism is not yet understood, a change to a passivation material such as silicon nitride is likely to increase MUTC power

handling, because it will have an effect on how easily damage can occur to the sidewalls. Silicon nitride has a much higher thermal conductivity than silicon dioxide, meaning that any heat related sidewall issue such as diffusion or unwanted compound formation can be mitigated. Additionally, because it is also a good insulator, it will not have any negative consequences on device dark current.

Chapter 5

POTENTIAL IMPROVEMENTS IN EPITAXY DESIGN

5.1 Epitaxy Improvements

As mentioned previously, the main setbacks in performance of flipped absorber MUTC PDs come from series resistance issues, which can be addressed in device design modifications. This problem can also be mitigated through epitaxy changes. In the original epitaxy, the thin 150 nanometer P-contact is responsible for the majority of the series resistance, and it is not necessary for it to be quite that thin. If this thickness was doubled to 300 nanometers, device resistance would be approximately quartered.

With this doubling in thickness will come a reduction in responsivity, but this is not necessarily a problem. As these devices stand currently, responsivity is 0.65 A/W, which is well beyond what is necessary for them to perform correctly. Thus, it would be wise to quarter the resistance even though it will come with a lower responsivity.

In addition to an increased P-contact thickness, this epitaxy would benefit from switching the P-contact dopant from zinc to beryllium. Under the high temperatures that come along with device fabrication, zinc is more likely to diffuse, meaning that dopant atoms are more likely to move out of the P-contact region into surrounding areas. This happening to any degree will lead to higher resistance of the P-contact region, which is unideal for the reasons mentioned previously. Thus, a switch to a beryllium dopant with a similar concentration is a more ideal choice for this epitaxy.

Chapter 6

CONCLUSION

6.1 Summary

All aspects considered, flipped absorber MUTC PDs have dissipated power tolerances that make them comparable to MUTC PD records before any optimization has been done to the epitaxy or the devices themselves. Considering that they currently have a minimum series resistance of 35 ohms, having a near record breaking dissipated power speaks to the high potential that they could have if their resistance was brought down to normal high power MUTC levels (as low as 2 ohms) [3]. While it is RF output power and not dissipated power that defines the end all usefulness of RF PDs, these two quantities approach each other when the minimum bias condition is lowered as a result of a lower series resistance. For this reason, a lower series resistance means that these devices have the potential to break records in both dissipated and RF output power with this improvement made.

In terms of what needs to happen to make flipped absorber PDs perform as best as possible, the next steps are relatively straightforward. The biasing contact points need to be moved as close as possible, even if new lithography methods are required for it. The P-contact metal needs to be expanded to improve heat sinking. The P-contact epitaxial thickness must be increased to a value that still maintains a sufficient responsivity. Finally, the P-contact dopant should be changed to a less diffusive element.

As mentioned previously, UVA first predicted a 110% improvement in dissipated power for the flipped absorber epitaxy compared to a standard MUTC epitaxy. However, at the time of this model, it was not understood just how significant the resistance of the P-contact region would be. Through the improvements mentioned, future flipped absorber devices could enter a domain where the P-contact joule heating becomes insignificant, as would be ideal. When this happens, these devices will more correctly fit the original model and reek the benefits that it has predicted.

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