# DESIGN, FABRICATION, CHARACTERIZATION, AND ANALYSIS OF WIDE BAND GAP GALLIUM PHOSPHIDE SOLAR CELLS AND GALLIUM PHOSPHIDE ON SILICON

by

Martin B. Diaz

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to my

## MOTHER and FATHER

# TABLE OF CONTENTS

LI LI A	ST ( ST ( BST)	OF FIGURES
$\mathbf{C}$	hapto	er
1	INT	RODUCTION
	1.1	The World's Energy Problem and a Solution
		1.1.1The Current Energy Situation11.1.2The Solar Solution4
	$1.2 \\ 1.3 \\ 1.4$	Approach    6      Objectives    7      Thesis Outline    6
<b>2</b>	LIT	ERATURE REVIEW
	2.1	Solar Cells
		2.1.1Single-Junction Solar Cells102.1.2Multi-Junction11
	2.2	GaP on Si
3	EX	PERIMENTAL METHODS
	3.1	Liquid Phase Epitaxy
		3.1.1 LPE System Configuration

		3.1.2	Preparation and Growth Procedure	17
	3.2	Analy	sis Techniques	19
		3.2.1 3.2.2 3.2.3	SEM	19 19 20
	3.3	Growt	h and Analysis of GaP on Si	20
		3.3.1 3.3.2 3.3.3 3.3.4	$\begin{array}{l} 1^{st} \mbox{ Generation Single Layer Growth and Substrate Analysis } \\ 2^{nd} \mbox{ Generation Single Layer Growth } \\ 2^{nd} \mbox{ Generation Second Layer Growth } \\ 3^{rd} \mbox{ Generation Single Layer Growth } \\ \end{array}$	20 25 27 29
	3.4	Summ	ary	30
4	SOI	ELL FABRICATION AND ANALYSIS	31	
	4.1	GaP 7	Гwo-Terminal Solar Cell	31
		$4.1.1 \\ 4.1.2$	Device Design	31 34
			4.1.2.1Preparation4.1.2.2LPE growth4.1.2.3Cleaning and Metalization	34 34 35
		4.1.3	Performance Analysis	37
			4.1.3.1       QE       QE	37 37
	4.2	GaAsl	P on Si Three-Terminal Device	39
		$4.2.1 \\ 4.2.2$	Device Design	40 42
	4.3	Device	e Summary	44

5	COI	CLUSIONS	5
	$5.1 \\ 5.2$	Summary	15 16
RI	EFEI	ENCES	9
A	open	lix	
FI	GUF	E REPRINT PERMISSIONS	1

# LIST OF FIGURES

1.1	World primary energy consumption [1]	2
1.2	World energy consumption by region, 1990-2035 (quadrillion Btu) [2]	3
1.3	Oil demand by region (450 scenario) [3]. $\ldots$ $\ldots$ $\ldots$	3
1.4	Primary energy use by fuel, 1980-2035 (quadrillion Btu) [2]	4
1.5	Global cumulative installed PV capacity by interconnection status [4]	5
1.6	Efficiency and cost projections for first- (I), second- (II), and third- generation (III) PV technologies (wafer-based, thin films, and advanced thin films, respectively) [8]. Reprinted with permission from Elsevier.	5
1.7	Structure and band diagram of <b>p</b> on <b>n</b> GaP solar cell on n-Si	7
1.8	N on p GaP solar cell structure on p-Si	8
2.1	Solar cell equivalent circuit diagram	10
2.2	Solar cell diode curve under illumination	11
2.3	A multi-junction solar cell system with each cell absorbing part of the solar spectrum	12
3.1	Liquid Phase Epitaxy System	17
3.2	Graphite boat cross-sections	18
3.3	$1^{st}$ Generation Single Layer SEM Image $\ldots \ldots \ldots \ldots \ldots \ldots$	21

3.4	EDS results of 1st generation single layer growth	22
3.5	DC RCs for p-type Si (111) shows the deviation along the horizontal direction	23
3.6	DC RCs for p-type Si (111) shows the deviation along the vertical direction	24
3.7	DCs RC for n-type Si (111) shows both the horizontal and vertical deviation	24
3.8	$2^{nd}$ Generation Single Layer SEM Image	26
3.9	SEM Image of Si peaks in $2^{nd}$ Generation Single Layer	27
3.10	$2^{nd}$ Generation Second Layer SEM Image	28
3.11	SEM Image of $3^{rd}$ Generation Single Layer	30
4.1	Optimization for the thickness of the base layer	32
4.2	Optimization for the thickness of the emitter layer	33
4.3	GaP solar cell structure	33
4.4	GaP solar cell fabrication process	36
4.5	QE of GaP solar cell (EQE corrected with the measured reflection to give IQE)	38
4.6	Comparison of the measured and simulated IQE for the GaP solar cell	38
4.7	J-V curve for the GaP solar cell	39
4.8	Optimization for the thickness of the base layer	40
4.9	Optimization for the thickness of the emitter layer	41
4.10	GaAsP/Si three-terminal solar cell device structure	42

4.11	Quantum efficiency of each device in the three-terminal system	43
4.12	Simulated J-V curve for each device in the three-terminal system $% \mathcal{A}^{(1)}$ .	43
5.1	Three-terminal double-junction solar cell efficiency as a function of the bandgap of the top solar cell with Si as the bottom solar cell	47
5.2	Selectively grown GaP solar cell on a Si solar cell $\hdots$	47
5.3	A GaAsP solar cell grown on a Si solar cell	48

# LIST OF TABLES

3.1	Composition of $1^{st}$ Generation Single Layer $\ldots \ldots \ldots \ldots$	22
3.2	Composition of $2^{nd}$ Generation Single Layer	26
3.3	Composition of $2^{nd}$ Generation Second Layer	28
3.4	Composition of $3^{rd}$ Generation Single Layer	29

## ABSTRACT

The cost of electricity generated by solar cells is an important factor limiting the competitiveness of photovoltaics in the energy economy. A reduction of this cost by increasing the conversion efficiency can be achieved with the application of multijunction structures composed of III-V materials grown on silicon (Si), because Si is a well developed technology and less expensive than III-V or Ge substrates. It has been found that gallium phosphide (GaP) is a good III-V material candidate for high quality epitaxial growth on Si due to its lattice matching with Si. The GaP material can serve as the top solar cell above a Si solar cell in a multi-junction system or a platform for subsequent III-V solar cell growth. In this work, liquid phase epitaxy (LPE) was used to grow GaP on Si (111) substrates. The epitaxial layers have been characterized by SEM and EDS. Using a systematic approach to improve the quality of the GaP epitaxial layers, semi-uniform layers with a 2-4% Si concentration have been achieved. These epitaxial layers should provide a good platform for further growth of III-V solar cells. Also, in this work, a GaP solar cell device with a  $V_{OC}$ of 1.56 V, a  $J_{SC}$  of 1.2 mA, and an efficiency of 1.04% under AM 1.5G without any anti-reflection coating has been designed and fabricated. A GaAsP/Si 2-junction three terminal solar cell device with an efficiency of 37% has also been designed in this work. Future work includes the incorporation of the III-V epitaxial growth on Si using LPE with these device designs to fabricate high-efficiency multi-junction device structures.

## Chapter 1

## INTRODUCTION

"Within **6 hours**, deserts receive more energy from the sun than humankind consumes within **a year**." -Dr. Gerhard Knies

## 1.1 The World's Energy Problem and a Solution

### 1.1.1 The Current Energy Situation

On March 11, 2011, Japan was struck by a magnitude 8.9 earthquake which led to the devastation of four nuclear power plants in Fukushima. This unfortunate situation has once again brought to light the dangers that exist with nuclear power. The unexpected shutdown of the nuclear plants also exposed the inconsistency in this form of energy that millions of people are relying on and resulted in the loss of 6.8 gigawatts of electric generating capacity. Due to these concerns with using nuclear power as an energy source, Japan and other countries have suspended, or even abandoned, plans for future nuclear power plants, while other countries are now planning on phasing out nuclear energy all together.

Also, with depleting oil fields and the environmental impacts of coal, oil, natural gas, etc., it is becoming more apparent that safe and renewable sources of energy must be developed. Figure 1.1 shows that the strongest growth of the



Figure 1.1: World primary energy consumption [1].

world primary energy consumption since 1973 was 5.6% in 2010 according to the BP Statistical Review of World Energy from June 2011 [1].

According to the U.S. Energy Information Administration (EIA) the world marketed energy consumption is projected to rise significantly by nearly 50% from 2009 through 2035 as shown in figure 1.2 [2].

Despite the forecast by the International Energy Agency (IEA) of diminished future oil demand according to the long-term plan of limiting the concentration of greenhouse gases in the Earth's atmosphere to 450 ppm of carbon-dioxide equivalent shown in figure 1.3, the demand of global energy continues to outpace the increase in supply [3]. Yet, environmental concerns and high energy prices are ultimately resulting in renewable sources leading the rise in primary energy consumption as shown in figure 1.4. The forecast shows the total fossil fuel share falling from 83% in 2009 to 78% in 2035 as renewables increase from 8% in 2009 to 13% in 2035 [2]. This reveals the opportunity for renewables to significantly impact the world's current energy crisis.



Figure 1.2: World energy consumption by region, 1990-2035 (quadrillion Btu) [2].



Figure 1.3: Oil demand by region (450 scenario) [3].



Figure 1.4: Primary energy use by fuel, 1980-2035 (quadrillion Btu) [2].

### 1.1.2 The Solar Solution

Because photovoltaics (PV) emit no pollution, harness the energy directly from the sun by converting the incident solar radiation into electricity, and have an energy payback of 1-4 years, solar energy is an excellent renewable energy source and solution to the world's energy problem [5]. According to the National Renewable Energy Laboratory (NREL), the total cumulative installed PV capacity represented in figure 1.5 grew nearly 75% from 2007 to 2008.

An important factor limiting the competitiveness of photovoltaics in the energy economy is the cost of electricity that the solar cells generate. This cost can be reduced by increasing the conversion efficiency. As depicted in figure 1.6, the high efficiency third generation photovoltaic technology will result in costs lower than previous generations [6]. However, single bandgap solar cells are limited in efficiency by the Shockley-Queisser limit [7]. Therefore, a straightforward method for increasing the efficiency is to increase the number of junctions in tandem solar cells resulting in more efficient absorption from the solar spectrum.



Figure 1.5: Global cumulative installed PV capacity by interconnection status [4].



Figure 1.6: Efficiency and cost projections for first- (I), second- (II), and thirdgeneration (III) PV technologies (wafer-based, thin films, and advanced thin films, respectively) [8]. Reprinted with permission from Elsevier.

## 1.2 Approach

This research involves the design, analysis, and fabrication of epitaxial gallium phosphide (GaP) on silicon (Si) through liquid phase epitaxy (LPE) for multijunction solar cell applications. The use of a multi-junction approach to improve cell efficiency is well understood and well established in several cell conversion technologies. The development of an effective top cell which could be directly deposited onto a crystalline Si bottom-cell would provide a substantial improvement in efficiency at a much lower cost due to the substitution of Si as the growth substrate.

The design of an effective top solar cell begins with the realization of an open circuit voltage (V<sub>OC</sub>) that is 60 to 100% greater than the open circuit voltage of the Si solar cell. Structures of III-V materials have a well-documented high Voc performance of  $\approx Eg/q - 0.4eV$  making III-V materials an excellent candidate for top cell structures [9]. GaP is the III-V semiconductor material of choice for the fabrication on Si in this work for the following reasons:

- Both Si and GaP based devices are well developed technologies allowing for a solid foundation upon which to build.
- The lattice constant of GaP and Si are 5.4505A and 5.4310A, respectively, resulting in a heterostructure with a lattice mismatch at the GaP/Si interface of 0.37%, allowing for good epitaxial growth.
- The high quality epitaxial GaP layer acts as an excellent buffer layer for subsequent III-V layer growth.

The fabrication method of LPE is used in this work because uniform, reproducible, and high quality growth layers can be achieved as the growth occurs at near thermal equilibrium. Along with a high growth rate, this technology is inexpensive and relatively easy to maintain and operate. The designs for this work include a GaP solar cell fabricated on a GaP substrate as well as a GaP solar cell fabricated on a Si substrate. The latter design involves two structures with a GaP buffer layer grown on a Si substrate followed by the growth of the GaP p-n junction layers. Figure 1.7 shows the structure involving an n-Si substrate and the subsequent p on n GaP structure with the accompanied band diagram. The band diagram reveals the ability of fabricating a solar cell on an n-Si substrate with both front and back contacts. Because the diffusion length is much lower in the n-type epitaxial layer than the higher quality p-type epitaxial layer, an n on p GaP structure solar cell structure was designed to achieve a higher performance [10]. Figure 1.8 shows the n on p GaP structure on a p-Si substrate.



Figure 1.7: Structure and band diagram of p on n GaP solar cell on n-Si

#### 1.3 Objectives

The use of wide bandgap solar cells in a multi-junction solar cell system is imperative to the goal of high efficiency. This research will focus on the design, fabrication, and analysis of GaP solar cells on Si using rigorous, quantitative, and predictive models. The specific objectives of this thesis include:

- 1. To design GaP solar cells on Si.
- 2. To grow an epitaxial GaP layer on a Si substrate through LPE.



Figure 1.8: N on p GaP solar cell structure on p-Si

- 3. To achieve <5% Si concentration in the epitaxial GaP buffer layer.
- 4. To design a GaP solar cell on a GaP substrate based on quantitative and predictive models.
- 5. To fabricate through LPE and analyze the performance of the GaP solar cell.
- 6. To design a GaAsP/Si three-terminal double-junction solar cell device based on quantitative and predictive models to be fabricated through LPE.

In this work, the development of wide bandgap GaP solar cell structures will be designed and fabricated for further analysis. The preliminary work towards transferring this design onto a Si substrate involving two structure designs will also be designed. The first structure includes a single-junction on a p-Si substrate with a p-GaP base, n-GaP emitter, and all front contacts. The second structure includes a single-junction on an n-Si substrate with a p-GaP emitter, n-GaP base, and both front and back contacts.

### 1.4 Thesis Outline

The design, fabrication, characterization, and analysis of the wide bandgap gallium phosphide solar cell on silicon is discussed in this thesis.

Chapter 2 will review the solar cell mechanism and literature for wide bandgap GaP solar cells, the growth of GaP on Si, and device structures involving the GaP on Si heterostructure.

Chapter 3 will discuss the experimental methods and results in this work. The procedures used for growing epitaxial GaP on Si using liquid phase epitaxy and the analysis of the epitaxial growth layers will be presented in this chapter.

Chapter 4 will describe the fabrication and analysis of the GaP solar cell device structure. The performance of the GaP solar cell will be analyzed and compared. This chapter will also present the design of a GaAsP/Si three-terminal double-junction solar cell device to be fabricated through LPE.

Chapter 5 will summarize this thesis and discuss the possible space for future work of epitaxial GaP on Si for multi-junction solar cell system applications.

# Chapter 2

## LITERATURE REVIEW

### 2.1 Solar Cells

## 2.1.1 Single-Junction Solar Cells

Since the conventional solar cell is basically a diode, it can be characterized by the ideal diode equation which describes the current as a function of voltage:

$$I = I_0 \left( e^{\frac{qV}{kT}} - 1 \right) \tag{2.1}$$

where  $I_0$  is the dark saturation current:

$$I_0 = qA\left(\frac{D_n}{L_n}\frac{n_i^2}{N_A}\theta_n + \frac{D_p}{L_p}\frac{n_i^2}{N_D}\theta_p\right)$$
(2.2)

Figure 2.1 shows the equivalent circuit diagram for a solar cell under illumination.



Figure 2.1: Solar cell equivalent circuit diagram

Under illumination, the diode equation becomes:

$$I = I_0 \left( e^{\frac{q(V+IR_S)}{nkT}} - 1 \right) - \frac{V + IR_S}{R_{SH}} - I_L$$
(2.3)

where  $I_L$  is the light generated current:

$$I_L = qG\left(L_n + L_p + W\right) \tag{2.4}$$

The ideal diode curve is shown in figure 2.2. Where  $V_{OC}$  is:

$$V_{OC} = \frac{nkT}{q} ln \left(\frac{I_{SC}}{I_0} + 1\right)$$
(2.5)



Figure 2.2: Solar cell diode curve under illumination

The solar cell conversion efficiency is defined as:

$$\eta = \frac{V_{OC}I_{SC}FF}{P_{in}} \tag{2.6}$$

where  $P_{in}$  is determined by the solar irradiance spectrum and FF is the fill factor:

$$FF = \frac{V_{MP}I_{MP}}{V_{OC}I_{SC}} \tag{2.7}$$

## 2.1.2 Multi-Junction

The conventional multi-junction solar cell is comprised of single-junction solar cells of different bandgaps arranged to absorb the different parts of the solar spectrum. As shown in figure 2.3, the solar cells are structured so that they form a stack with the highest bandgap solar cell at the top to absorb the high energy photons and the lowest bandgap solar cell at the bottom to absorb the lower energy photons. The below bandgap photons that pass through the wide bandgap solar cell will be absorbed by the lower bandgap solar cell while in a single-junction solar cell would be lost. As for the higher energy photons that are absorbed by the wide bandgap solar cell in the multi-junction solar cell, in a single-junction solar cell with a lower bandgap, the excess energy of these above bandgap photons would be lost due to thermalization and the photon would ultimately only be as valuable as a lower energy photon.



Figure 2.3: A multi-junction solar cell system with each cell absorbing part of the solar spectrum

Optimizing the bandgaps of each solar cell will increase the conversion efficiency of the multi-junction solar cell system such that the absorption of a wider range of the solar spectrum will occur. Increasing the number of junctions in the multi-junction solar cell system can also increase the performance of the solar cell up to the maximum theoretical efficiency of 86.8% for an infinite number of p-n junctions [11].

The lattice mismatch and current mismatch are two problems that limit the performance of multi-junction solar cells. In this work, as discussed in chapter 1,

the lattice mismatch between Si and GaP is only 0.37%, allowing for good epitaxial growth. Furthermore, a separate terminal structure design would eliminate the current mismatch problems.

## 2.2 GaP on Si

GaP on Si heterostructures have attracted much attention for device applications as the Si technology is well developed and a less expensive alternative to III-V substrates. Further motivation includes the ability to fabricate the subsequent GaP device structures on Si at lower temperatures that would not strongly affect the Si device structure below.

Various techniques have been used by others to grow or deposit GaP layers on Si. J. J. Cuomo *et al* employed the technique of electrolysis from a fused salt solution to grow epitaxial GaP layers on Si [12]. Evaporation and vapor phase epitaxy has been utilized for the application of GaP on Si by O. Igarashi and J. P. André *et al*, respectively [13] [14].

The growth method of liquid phase epitaxy, as used in this work, has been used by S. Huang *et al* to grow thin epitaxial GaP films on p-type Si (111) substrates. These films were analyzed using energy dispersive x-ray spectroscopy which showed a very high Si concentration of 15% within the film layers. However, it was observed that the phosphorous diffusion into the Si substrate formed an n-type doped Si layer at the interface resulting in a p-n junction. The photovoltaic effect was observed as a result of this Si diode junction which exhibited an open circuit voltage of 486 mV [15].

H. Beneking *et al* has also applied the technique of liquid phase epitaxy to grow GaP-Si heterostructures on Si substrates using Sn as the metal solvent, as used in this work. The epitaxial growth occurred at temperatures between  $850^{\circ}$  C and  $800^{\circ}$  C. The solubilities of GaP and Si in Sn was also investigated by Beneking at these growth temperatures. It was determined by Beneking that the cooling rate as well as the orientation of the substrate greatly affects the morphology of the epitaxial growth layers with the best results achieved on Si (111) substrates using a rapid initial temperature decrease followed by a lower cooling rate. It was also established that due to the use of Sn as the metal solvent, the growth layers were degenerately n-type doped with Sn and Si. Beneking was also able to grow a subsequent higher purity second layer using Ga or In as the metal solvent [16].

## Chapter 3

## EXPERIMENTAL METHODS

In this chapter, the experimental methods and results of this work are discussed. The procedures used for growing epitaxial GaP on Si using liquid phase epitaxy and the analysis of the epitaxial growth layers and substrates using scanning electron microscopy (SEM), energy dispersive x-ray spectroscopy (EDS), and x-ray diffraction (XRD) will be presented.

## 3.1 Liquid Phase Epitaxy

High quality, uniform, and reproducible epitaxial, single-crystal growth layers can be achieved with LPE as the growth occurs at near thermal equilibrium making this method of fabrication ideal for solar cell devices. This work benefits from the LPE system when compared to other industrial growth methods such as molecular beam epitaxy (MBE) and metal organic chemical vapor deposition (MOCVD), as the LPE system results in a high growth rate and is less expensive and easier to build, maintain, and operate. In addition to these advantages, LPE does not require a high vacuum during the growth procedure.

This technique incorporates the soluble growth material in a liquid metal solvent at elevated temperatures. As the temperature is lowered, the growth material precipitates out of the solution and onto the substrate surface driven by the supersaturation of this liquid-solid phase equilibrium eventually forming an epitaxial growth layer. This work uses the supersaturated ramp cooling approach for growing epitaxial layers. This involves the saturation of the solution at an elevated temperature and bringing in contact the substrate with the liquid solution only after slightly decreasing the temperature to create a supersaturated solution. This is followed by the ramp cooling over the substrate at a constant rate down to a specific temperature to achieve the desired layer thickness.

However, LPE is not the most suitable technology for large area growth layers or epitaxial growths requiring abrupt junctions or very accurate layer thicknesses.

#### 3.1.1 LPE System Configuration

The LPE system used in this work shown in figure 3.1 is a horizontal system composed of a sliding three-zone furnace controlled by a programmable Chino Model KP temperature controller. The temperature of the system is monitored with three K-type thermocouples, one at the front zone near the heating coils, one at the rear zone near the heating coils, and a central one situated in the graphite boat directly beneath the location of the substrate during growth encased in a small quartz tube. A larger quartz tube and sealable brass caps comprise the LPE growth chamber which houses the graphite boat with the substrates and solutions during growth. The front end has ports for the central thermocouple, the exhaust/vacuum valves, and a quartz push rod used for maneuvering the substrates during the growth process. The back end port is used for gas flow into the system. The removal of oxygen and other impurities from the growth environment is accomplished by purging the quartz tube with high purity Ar (99.999% purity) from a compressed gas cylinder. Ultra high purity  $H_2$  (99.99998% purity) from a compressed gas cylinder or from a Parker Balston hydrogen generator with a palladium membrane at a max flow of 300 cc/min is used for the growth environment.

A base, slide bar, solution well bar, well caps, and graphite pins comprise the high purity graphite boat shown in figure 3.2 used to hold the growth solutions and



Figure 3.1: Liquid Phase Epitaxy System

substrates. The slide bar houses the substrates and the solution well bar houses the growth solutions while the graphite pins hold the solution well bar securely in place as the slide bar is free to move back and forth with the aid of the push rod.

## 3.1.2 Preparation and Growth Procedure

Before the graphite boat with the growth materials and substrates can be placed into the quartz tube, the materials must be prepared and thoroughly cleaned of all impurities and native oxides in order to achieve high quality epitaxial growth.

Substrates are obtained from prime grade, single-side polished wafers by dicing to proper size to fit the divots of the slide bar. In this work, selectively patterned substrates are used as the seed substrates. A 500 nm thick layer of  $Si_3N_4$  deposited by plasma-enhanced chemical vapor deposition (PECVD) and patterned using photolithography acts as the growth mask layer. The purpose of this mask layer is to reduce the growth area and protect the far edges of the Si substrate from the growth solution during growth as Si will be vulnerable to some metal solvents, such as Ga,



Figure 3.2: Graphite boat cross-sections

used for subsequent III-V growth layers.

To eliminate all impurities and native oxides from the surface of the substrates, the following cleaning procedure is performed:

- Clean with a 1:1:5 solution of NH<sub>4</sub>OH (ammonium hydroxide) + H<sub>2</sub>O<sub>2</sub> (hydrogen peroxide) + H<sub>2</sub>O (water) at 70° C for 15 minutes for the removal of organic contaminants (RCA-1 clean).
- Dip in 5% HF (hydrofluoric acid) to remove the oxide layer formed by the RCA-1 clean until the surface is hydrophobic.
- 3. Clean with a 1:1:6 solution of HCl (hydrochloric acid) +  $H_2O_2$  +  $H_2O$  at 70° C for 10 minutes for the removal of metallic contaminants (RCA-2 clean).
- 4. Repeat step 2 to remove the oxide layer formed by the RCA-2 clean.

After cleaning, the substrates are dried using  $N_2$  and immediately placed onto the slide bar. The solution materials, including the metal solvent, growth material, wetting agents, and doping material, if any, are placed into the solution well bar and the graphite boat is inserted into the quartz tube which is then pumped down and purged. The pump down and purge process includes the system pump down to 50 mTorr using a vacuum pump followed by a purge with Ar gas for 3 times to thoroughly purify the growth chamber. This process is then followed by the flow of ultra high purity  $H_2$  into the growth chamber.

The growth procedure is then controlled with the programmable temperature controller and occurs in the H<sub>2</sub> environment at atmospheric pressure. The basic growth procedure begins with a ramp up in temperature above the melting point of the metal solvent to allow the homogenization of the growth solution. The temperature is then held at a constant value for 30-60 minutes after the source substrate is moved into contact the growth solution. This allows for the saturation of the growth solution with the source material. Once all desired materials are saturated in the solution, the growth solution is isolated from any other source materials and the temperature is slightly lowered by 2-10° C to create a super-saturated solution. This super-saturation approach aids with the nucleation on the substrate surface. To begin the growth, the seed substrate is moved to contact with the growth solution and the temperature is lowered to a specified temperature according to the desired thickness at a rate of  $\approx 1^{\circ}$  C/min.

## 3.2 Analysis Techniques

#### 3.2.1 SEM

A JEOL JSM-7400F SEM is used in this work to take electron imaging of the growth layer surface and observe the surface morphology. A current of 10 mA and an electron beam voltage of 3 kV was used to obtain the SEM images.

## 3.2.2 EDS

This technique operates by detecting the x-rays generated from the atoms by the electron beam and creating a histogram of x-ray intensity as a function of energy which is characteristic of the element which produced it as shown in figure 3.4 The JEOL 7400 SEM also has an EDS feature which was used to identify the elemental composition of the growth layers at an accelerating voltage of 10 kV in order to detect the relevant elements.

### 3.2.3 XRD

This technique yields the atomic structure of the growth layers and substrates. X-ray diffraction occurs when incident x-ray beams interfere with each other caused by the atomic planes of a crystal. A Philips XPert-MPD high resolution xray diffractometer (HRXRD) is used in this work to analyze the crystallographic structure of the substrates.

## 3.3 Growth and Analysis of GaP on Si

This section will discuss the procedure for growing GaP on Si using LPE and the analysis of the growth layers using SEM and EDS. The three key factors that determine the quality of the growth layers are the seed substrate, growth solution composition, and the programmed growth time/temperature profile. XRD is used to examine the orientation of the seed substrate and its affect on the growth layer. By primarily adjusting the growth profile, a systematic improvement of the growth layers is presented.

## 3.3.1 1<sup>st</sup> Generation Single Layer Growth and Substrate Analysis

The first generation growth of GaP on Si was selectively grown on a p-type Si (111) seed substrate patterned with a  $Si_3N_4$  mask. The growth procedure begins with a pre-bake step at 910° C. This allows for the homogenization of the growth solution which includes Sn (99.99%), crushed polycrystalline GaP (99.999%), and Mg (99.98%) all from Alfa Aesar materials supplier. Sn is used as the metal solvent because of its high GaP to Si solubility ratio. The crushed GaP provides the source

for the GaP growth layer. Mg is utilized for oxide removal from the Si substrates during saturation and growth. Bi is also incorporated into the growth solution to facilitate the wetting of the solution on the Si substrates. The mass ratio of these materials is  $\approx 2000 \text{ Sn}:100 \text{ GaP}:100 \text{ Bi}:1 \text{ Mg}.$ 

Next, the solution is saturated with Si at 750° C with an n-type Si (100) source substrate for 1 hour. This prevents the etching of the Si seed substrate during growth. This is followed by the 2° C super-saturation and then the growth at a cooling rate of .5° C/min for 1 hour.

First observation of the resulting growth layer using a profilometer revealed a smooth and continuous 3  $\mu$ m growth layer. After observing with SEM as shown in figure 3.3, the layer is confirmed as being smooth and continuous with few defects. The EDS analysis in Table 3.1 shows the material composition of the growth layer. Results reveal that this first generation growth procedure produces a good baseline 3  $\mu$ m smooth and continuous GaP growth layer with a 15-17% Si concentration.



Figure 3.3: 1<sup>st</sup> Generation Single Layer SEM Image

This same growth procedure was carried out on two 1/2 substrates simultaneously, p-type Si (111) and n-type Si (111). This experimental design will allow the comparative study of the effects on the growth layer due to the growth substrates.

Element	Weight%	Atomic%
Si K	10.03	15.44
ΡK	37.08	51.76
Ga L	52.88	32.79
Totals	100.00	

**Table 3.1:** Composition of  $1^{st}$  Generation Single Layer



Figure 3.4: EDS results of 1st generation single layer growth

The growth time was extended to 90 minutes and the mass ratio of the materials in the growth solution was  $\approx 1000$  Sn:100 Bi:20 GaP:1 Mg.

First observation of the two substrates after growth using the profilometer revealed a 3.5  $\mu$ m growth layer on the p-type Si (111) and a rough surface with no growth on the n-type Si (111). Further analysis using EDS confirmed the expected 15-20% Si concentration in the GaP growth layer on the p-type Si (111) seed substrate.

To establish a possible reason for the difference in growth results, XRD was used to examine the orientation of both the p-type and n-type Si (111) seed substrates. The double-crystal (DC)  $\omega$  rocking curve (RC) measurements were taken for 4 different azimuth positions for each sample. The RCs were done at  $\phi = 0^{\circ}$ , 90°, 180°, and 270° as shown in figures 3.5 - 3.7.



Figure 3.5: DC RCs for p-type Si (111) shows the deviation along the horizontal direction

From the XRD results, it is evident that the only significant deviation is in the vertical direction of the p-type Si substrate. By taking  $\frac{1}{2}$  of the deviation between omega 90 and omega 270, the miscut angle of the p-type Si (111) substrate is estimated to be  $\approx 4^{\circ}$  while the deviation in the n-type Si (111) appears to be



Figure 3.6: DC RCs for p-type Si (111) shows the deviation along the vertical direction



Figure 3.7: DCs RC for n-type Si (111) shows both the horizontal and vertical deviation

 $<0.2^{\circ}$ . These results suggest that the growth is preferential to substrates with a large miscut angle providing nucleation centers.

## 3.3.2 2<sup>nd</sup> Generation Single Layer Growth

In order to improve the quality of, and decrease the Si concentration within the epitaxial GaP growth layer, the growth procedure was altered. Because the concentration of Si in the growth layer remains high with the baseline growth procedure, the new procedure is aimed toward promoting the growth of GaP while limiting the growth of Si on the seed substrate.

For this procedure, the same source materials are used with the mass ratio of 1000 Sn:100 Bi:20 GaP:1 Mg. The significant alteration to the procedure is with saturation and super-saturation steps. The pre-bake step is also eliminated from this procedure in order to shorten the time of the overall growth process.

The process first begins with the saturation of the Si source substrate at 740° C for 1 hour. The Si source substrate is then removed and the temperature is increased to 750° C to saturate the growth solution with GaP also for 1 hour. This is followed by the 2° C super-saturation and then the growth at a cooling rate of  $\frac{1}{3}$ ° C/min for 90 minutes. The key features of this profile during growth conditions are:

- $\bullet\,$  The 8° C under-saturation of Si
- The 2° C super-saturation of GaP and
- The  $\frac{1}{3}^{\circ}$  C/min cooling rate for 90 minutes

This new temperature profile is designed to give the advantage to GaP growth while hindering the growth of Si. The slower cooling rate is expected to facilitate GaP growth at nucleation centers caused by the etching of the substrate due to the under-saturation of Si. First observation of the resulting growth layer reveals a uniform and continuous growth layer with 95% of the growth area covered. As shown in figure 3.8, SEM reveals a locally smooth layer, but the entire growth layer suffers from Si peaks shown in figure 3.9. The concentration of Si is significantly lower, 3.6%, in the regions void of Si peaks as shown in table 3.2. However, due to the Si peaks, the overall Si concentration of the growth layer reaches 10%. Results reveal that this modified growth procedure produces a 3.8  $\mu$ m uniform GaP growth layer with Si peaks leading to a 3-10% Si concentration.



Figure 3.8: 2<sup>nd</sup> Generation Single Layer SEM Image

Element	Weight%	$\operatorname{Atomic}\%$
Si K	2.10	3.66
РК	31.45	49.69
Ga L	66.45	46.64
Totals	100.00	

**Table 3.2:** Composition of  $2^{nd}$  Generation Single Layer



Figure 3.9: SEM Image of Si peaks in  $2^{nd}$  Generation Single Layer

# 3.3.3 2<sup>nd</sup> Generation Second Layer Growth

The previous procedure resulted in an epitaxial GaP growth layer with Si concentrations as low as 3%. This second layer growth is designed to eliminate Si from the growth layer by removing the Si source substrate from the growth process. By using the previous growth layer with 3-10% Si as the seed substrate, the saturation of the solution with Si becomes unnecessary as the Si substrate is protected by the GaP growth layer and the Si<sub>3</sub>N<sub>4</sub> mask.

The mass ratio of the materials in the growth solution is now reduced to 50 Sn:1 GaP, as GaP is less vulnerable to oxide growth and therefore does not require Mg. The growth of this second layer is carried out at a slightly lower temperature with the saturation of GaP at 720° C for 90 minutes. The remainder of the procedure remains the same with the 2° C super-saturation followed by the growth at a cooling rate of  $\frac{1}{3}^{\circ}$  C/min for 90 minutes.

As shown in figure 3.10, SEM reveals the second growth layer as non-uniform and with less areal coverage. EDS results in table 3.3 show a Si concentration consistent with the first growth layer. However, this second layer is void of Si peaks that plagued the first layer resulting in a Si concentration of 3-5%.



Figure 3.10: 2<sup>nd</sup> Generation Second Layer SEM Image

**Table 3.3:** Composition of  $2^{nd}$  Generation Second Layer

Element	Weight%	Atomic%
Si K	1.93	3.41
ΡK	30.12	48.24
$\operatorname{Ga} L$	67.95	48.35
Totals	100.00	

## 3.3.4 3<sup>rd</sup> Generation Single Layer Growth

A second growth procedure is designed to further decrease the Si concentration in the epitaxial GaP growth layer by preventing the growth of Si peaks as with the previous first layer growth. This is accomplished by increasing the degree of super-saturation with GaP while decreasing the degree of under-saturation with Si. The growth solution materials and source substrates are unchanged from the  $1^{st}$ generation single layer growth. The primary features of this profile during growth conditions include:

- The 2° C under-saturation of Si for 30 minutes
- The 8° C super-saturation of GaP for 1 hour and
- The  $\frac{1}{3}^{\circ}$  C/min cooling rate for growth

The resulting growth layer, after cleaning with RCA2, is 4  $\mu$ m thick but not as smooth as previous growth layers as shown by figure 3.11. Yet, the Si concentration of this first layer growth is lower than that of the previous generation. Table 3.4 shows the results of the EDS analysis. The overall concentration of this first layer growth is revealed to be 2-4%.

**Table 3.4:** Composition of  $3^{rd}$  Generation Single Layer

Element	Weight%	Atomic%
Si K	1.60	2.80
ΡK	31.66	50.19
$\operatorname{Ga} L$	66.74	47.00
Totals	100.00	



Figure 3.11: SEM Image of  $3^{rd}$  Generation Single Layer

#### 3.4 Summary

The experimental methods and analysis used in this work to improve the baseline growth procedure has been presented in this chapter. By adjusting the growth conditions of the LPE procedure and analyzing the growth layers and substrates using SEM, EDS, and XRD, the quality of the epitaxial GaP growth layers have been systematically improved over three generations by decreasing the Si concentration within the layers from 16 - 20% to 2 - 4%. From this set of experiments it is evident that the GaP must compete with Si to grow on the Si substrate and therefore must be aided during the initial growth stages by the super-saturation state of GaP and the under-saturation of Si in the growth solution. It is also revealed from this comparative study that the orientation of the seed substrate greatly affects the growth layer. The XRD analysis shows that the miscut of the seed substrate facilitates growth while a non-miscut substrate lacks the nucleation centers required to initiate growth.

## Chapter 4

## SOLAR CELL FABRICATION AND ANALYSIS

In this chapter, the GaP solar cell device designed, fabricated, and analyzed in this work is presented. The GaP device in this chapter is optimized based on the thickness of the epitaxial growth layers. As with the previous chapter, LPE is used to fabricate the GaP solar cell. The final device performance analysis is also presented and compared with modeled results. The design of a three-terminal GaAsP/Si solar cell device is also presented in this chapter.

## 4.1 GaP Two-Terminal Solar Cell

#### 4.1.1 Device Design

The GaP solar cell device fabricated in this work is designed with the aid of the one-dimensional semiconductor device simulator PC1D. By using the material properties and commonly reported values for GaP and solar cell devices with PC1D, the thicknesses of the epitaxial growth layers grown by LPE are optimized to give the best solar cell device performance.

For the PC1D simulation of the solar cell device, ideal values of parameters, such as the front-surface recombination velocity, are used to allow for the correct optimization of the thickness parameters though not likely achievable in this device fabrication. Doping concentration values for the n-type emitter and the p-type base are also held constant as the optimization is carried out. The doping concentration values used for the n-type emitter and the p-type base are  $1 \times 10^{18}$  cm<sup>-3</sup> and  $1 \times 10^{17}$ 

cm<sup>-3</sup>, respectively, as established by X. Lu *et al* [10]. The p-type GaP substrate is not expected to significantly affect the device performance and is therefore not incorporated into the simulation. The PC1D simulation is carried out using the AM 1.5G as the primary light source, which results in the following V<sub>OC</sub> versus thickness curves for the base layer and emitter layer shown in figures 4.1 and 4.2, respectively. The quantum efficiency (QE) of the GaP solar cell device is also simulated using PC1D and will be presented later in this chapter.



**Figure 4.1:** Optimization for the thickness of the base layer

The optimum p-type base layer thickness for this design is shown to be 8  $\mu$ m. As the base layer increases beyond 8  $\mu$ m, the Voc continues to decrease, yet due to the diffusion length, the maximum efficiency is reached as the increased thickness will no longer contribute to the current. The optimum n-type emitter layer thickness for this design is shown to be 0.8  $\mu$ m. The optimized device design is shown in figure 4.3.



Figure 4.2: Optimization for the thickness of the emitter layer



Figure 4.3: GaP solar cell structure

### 4.1.2 Fabrication

## 4.1.2.1 Preparation

The GaP device epitaxial layers are grown by LPE on a 500  $\mu$ m thick p-type GaP (100) substrate with a doping concentration of 1 x 10<sup>18</sup> cm<sup>-3</sup>. The source of GaP for the growth layer is from a source substrate that is also a 500  $\mu$ m thick p-type GaP (100) substrate with a doping concentration of 1 x 10<sup>18</sup> cm<sup>-3</sup>. Prior to loading the graphite boat with all growth materials, both substrates are cleaned with acetone, methanol, and isopropanol for five minutes each. The purpose of this cleaning procedure is to remove any organic contaminants on the surfaces of the substrates. This is then followed by the RCA2 clean and HF dip described in the previous chapter for the removal of metallic contaminants and the oxide.

All growth materials are then transferred to the graphite boat. The metal solvent used for the growth solution is Ga (99.99+%) from Alfa Aesar materials supplier due to its ability to wet the GaP substrate, which is baked at 910° C for 8 hours in a hydrogen atmosphere prior to the growth procedure. The baking of the Ga solvent before growth is essential in the removal of impurities and oxygen from the Ga. Zn is used as the dopant source for the p-type epitaxial layer and Sn is used as the n-type dopant source for the epitaxial emitter layer. The desired dopant concentration is achieved by incorporating the appropriate dopant amount into the growth solution dependent on the amount of Ga and determined from the phase diagrams according to A. S. Jordan and F. A. Trumbore *et al* [17] [18]. The desired dopant concentration of the p-type base layer and the n-type emitter layer is  $1 \times 10^{17}$  cm<sup>-3</sup> and  $1 \times 10^{18}$  cm<sup>-3</sup>, respectively.

## 4.1.2.2 LPE growth

The LPE growth procedure begins with the first growth solution saturation with the GaP source substrate at  $820^{\circ}$  C for 30 min and followed by a 5° C supersaturation cool. In order to achieve the desired epitaxial base layer thickness of  $8\mu$ m, the growth occurs at a cooling rate of 1° C/min for 65 min.

Next, the second growth solution saturation with the GaP source substrate occurs at 750° C for 30 min followed by the 2° C supersaturation cool. The desired epitaxial emitter layer thickness of  $0.8\mu$ m is achieved by cooling at a rate of 1° C/min for 10 min.

#### 4.1.2.3 Cleaning and Metalization

After removal from the furnace, the growth samples are cleaned in a diluted HCl solution before depositing the metal front and back contacts using electron beam physical vapor deposition. First, the back contact comprised of Pd (30nm)/ Zn (50nm)/ Pd (200nm)/ Ag (200nm) is deposited on the entire p-type back surface. A good ohmic back contact is formed by following the deposition with a 20 min anneal at 400° C in a hydrogen atmosphere. Because the front contacts will not cover the entire front surface, photolithography is used to pattern the n-type surface with a contact mask. Next, the front contact comprised of Pd (50nm)/ Si (80nm)/ Pd (100nm)/ Ag (200nm) is deposited on the selective n-type front surface. Before annealing the front contact at 500° C for 10 min in a hydrogen atmosphere, the metal that has been prevented from depositing onto the surface by the contact mask is lifted off. The complete fabrication process is depicted in figure 4.4.

This GaP solar cell does not have any anti-reflection (AR) coating. The performance of the solar cell can be further improved with an AR coating at the front surface, because less light is lost due to reflection. The AR coating is composed of a thin dielectric material layer with a specific thickness corresponding to the desired optimized wavelength. A single quarter-wavelength layer of optimum index of refraction can eliminate the reflection at one wavelength. A multi-layer coating can extend this elimination of reflection over a wider range of the spectrum. The additional interfaces created by the AR coating results in multiple reflected waves. The more out of phase these waves are with each other, the more they destructively



9. Anneal front contact & analyze

Figure 4.4: GaP solar cell fabrication process

interfere with one another. A total cancellation due to this interference results in zero net reflected energy. For the GaP solar cell in this design, a possible dielectric material choice for the AR coating is  $Si_3N_4$ .

## 4.1.3 Performance Analysis

In this section, the performance of the designed and fabricated GaP solar cell device is measured and analyzed. The performance analysis includes QE measurements as well as current-voltage (J-V) measurements under AM 1.5G one-sun illumination.

#### 4.1.3.1 QE

The QE of solar cell devices is the ratio of minority carriers collected by the solar cell device to the number of photons incident on the device as a function of the energy of the photons. The QE includes the external quantum efficiency (EQE) and the internal quantum efficiency (IQE). Unlike the EQE, the IQE does not incorporate the effect of optical losses from transmission or reflection. Figure 4.5 displays the measured QE curves as well as the reflection measurement used to obtain the corrected IQE curve.

The IQE curve generated from the PC1D simulation is shown in figure 4.6. The parameters used in this IQE curve fitting simulation are 0.2  $\mu$ m, 2.5  $\mu$ m, and 1 x 10<sup>6</sup> cm/s for the diffusion length in the n-type emitter layer, the diffusion length in the p-type base layer, and the front-surface recombination velocity, respectively.

### 4.1.3.2 J-V

The J-V curve of the GaP solar cell device is shown in figure 4.7 and is used to analyze the performance of the device in the dark and under AM 1.5G one-sun illumination. The diffusion lengths and the front-surface recombination velocity as determined by the IQE curve fitting simulation are shown to have great effects on



Figure 4.5: QE of GaP solar cell (EQE corrected with the measured reflection to give IQE)



Figure 4.6: Comparison of the measured and simulated IQE for the GaP solar cell

the performance of the GaP solar cell device. The high front-surface recombination velocity and low diffusion lengths seem to be the limiting factors of the device performance. Due to these limitations, the fabricated GaP solar cell has a  $V_{OC}$  of 1.56 V, a  $J_{SC}$  of 1.2 mA, and an efficiency of 1.04%. These results can be improved with the addition of an AR coating.



Figure 4.7: J-V curve for the GaP solar cell

## 4.2 GaAsP on Si Three-Terminal Device

In this section, the GaAsP/Si three-terminal solar cell device designed in this work is presented. As with the design of the GaP solar cell device, the onedimensional semiconductor device simulator PC1D is also used in this design. By using PC1D and the material properties and commonly reported values for GaAs and adjusting for the proper phosphorus concentration of GaAsP with the desired bandgap, the thicknesses and doping concentrations of the epitaxial growth layers grown by LPE are optimized to give the best solar cell device performance. This device design is then placed above a state-of-the-art Si solar cell device to simulate the performance of the entire three-terminal device.

## 4.2.1 Device Design

In order to optimize the device design, the properties and values of GaAs are modified to obtain values characteristic of GaAs<sub>0.69</sub>P<sub>0.31</sub>, which results in a bandgap of 1.81 eV. The absorption coefficient used in this design is that of GaAs shifted to the band edge of GaAsP. The following figures show the optimal values of the epitaxial layers for the GaAsP top junction device. Figure 4.8 shows that 5  $\mu$ m is the optimal value for the thickness of the p-type base layer. As the base layer increases beyond 5  $\mu$ m the Voc continues to decrease, yet due to the diffusion length, the maximum efficiency is reached as the increased thickness will no longer contribute to the current. The optimum n-type emitter layer thickness, that is reasonably achievable through LPE, for this design is shown to be 0.1  $\mu$ m as the performance decreases with increased thickness of the emitter layer thickness as shown by figure 4.9.



Figure 4.8: Optimization for the thickness of the base layer



Figure 4.9: Optimization for the thickness of the emitter layer

The doping concentration of each epitaxial layer is also optimized using PC1D. The established doping concentration values for the n-type emitter and the p-type base are 5 x  $10^{18}$  cm<sup>-3</sup> and 1 x  $10^{17}$  cm<sup>-3</sup>, respectively. This device design results in a single-junction solar cell with a V<sub>OC</sub> of 1.48 V and a J<sub>SC</sub> of 18.9 mA.

A state-of-the-art Si solar cell from the University of New South Wales (UNSW) is used as the bottom solar cell device in this three-terminal doublejunction solar cell system. In order to simulate the performance of the Si solar as the bottom junction solar cell, the thickness and the absorption of the top junction solar cell is considered. It is assumed that the photons unabsorbed by the GaAsP top solar cell will pass to the Si bottom cell. The three-terminal device structure is shown in figure 4.10. It is also assumed that the highly doped thin GaP buffer layer will not contribute to the absorption of any photons not absorbed by the GaAsP top cell.

Figure 4.11 shows the quantum efficiency for the UNSW Si solar cell and the simulated quantum efficiency of the designed GaAsP solar cell device. The performance of this three-terminal double-junction is simulated with the placement of the GaAsP solar cell as the top junction cell above the UNSW Si bottom solar



Figure 4.10: GaAsP/Si three-terminal solar cell device structure

cell device. Figure 4.12 shows the simulated J-V curves for each device in the three-terminal double-junction design. The final device design results an a three-terminal double-junction solar cell with an efficiency of 37%.

## 4.2.2 Device Fabrication and Analysis Procedure

As with the GaP device in the previous section, this three-terminal doublejunction GaAsP/Si device has been designed to be fabricated using liquid phase epitaxy. This section will describe the procedures to be used in the fabrication and analysis of this GaAsP/Si heterostructure device.

By fabricating this device structure using LPE, high quality epitaxial layers can be achieved. Also, because the substrate used in this growth procedure is a Si device structure, it is vulnerable to damage during the fabrication process. Yet, the temperatures involved in this LPE process are low enough to not significantly affect the Si device.

The LPE procedure is described in previous sections. For this device, a highly doped thin GaP buffer layer should be grown on the Si device as shown in figure 4.10.



Figure 4.11: Quantum efficiency of each device in the three-terminal system



Figure 4.12: Simulated J-V curve for each device in the three-terminal system

After this GaP layer growth, a  $Si_3N_4$  layer should be deposited and masked to allow for top contact deposition later in the fabrication process. The subsequent GaAsP growth layers are achieved as with the procedure described with the fabrication of the GaP device with the exception of the addition of GaAs to the growth solution to obtain the desired GaAsP composition. Once all epitaxial layers are grown, the  $Si_3N_4$  layer is removed and the deposition of the contacts follows, as described in the previous section.

The three-terminal design for this double-junction solar cell device not only eliminates the need for current matching during the design process, but also allows for the individual analysis of both the top and bottom devices separately. As presented in the design of this three-terminal double-junction device, separate J-V curves can be obtained by means of the bottom, middle, and top contacts to analyze the performance of the device.

### 4.3 Device Summary

In this chapter, a GaP solar cell device was designed and optimized using PC1D, fabricated by LPE, and analyzed with QE and J-V measurements. The quality of the epitaxial growth layers for this device is the limiting factor of this device. This results in low diffusion lengths in the epitaxial growth layers and a high front-surface recombination velocity. In order to achieve the simulated performance of the designed device from the PC1D simulation, the epitaxial growth layer quality must be improved to increase the diffusion length and decrease the front-surface recombination velocity. A second device structure is also designed in this chapter, which is a GaAsP/Si three-terminal double-junction solar cell device with an efficiency of 37%.

## Chapter 5

## CONCLUSIONS

### 5.1 Summary

The preliminary work toward a GaP solar cell device on Si has been presented in this work. Two GaP solar cell structures on Si have been proposed in this work. The GaP epitaxial layers in this work were grown on Si substrates by liquid phase epitaxy. A scanning electron microscope was used to characterize the surface morphology of the growth layers which showed to be uniform, smooth, continuous. Energy dispersive x-ray spectroscopy was used in this work to analyze the material composition of the growth layers. X-ray diffraction analysis has shown that the orientation of the seed substrate greatly affects the growth layer.

It has also been determined that GaP competes with Si during growth and by adjusting the growth conditions of the LPE procedure and analyzing the growth layers and substrates using SEM, EDS, and XRD, the quality of the epitaxial GaP growth layers have been systematically improved over three generations of epitaxial growths by decreasing the Si concentration within the layers from 16-20% to 2-4%. This work provides the basis for future research work toward further GaP and other III-V material growth on Si for photovoltaic applications.

Also, in this work, the design and optimization of a Gap solar cell device using PC1D was presented. The device was fabricated by LPE, and J-V and QE measurements were used to analyze the GaP solar cell device performance. In this work, a GaP solar cell device with a  $V_{OC}$  of 1.56 V, a  $J_{SC}$  of 1.2 mA, and an efficiency of 1.04% has been achieved. It has been shown that the quality of the epitaxial growth layers for this device is the limiting factor of this device. This results in low diffusion lengths in the epitaxial growth layers and a high front-surface recombination velocity. To achieve the simulated performance from the PC1D simulation for future device fabrications, the epitaxial growth layer quality must be improved to increase the diffusion length and decrease the front-surface recombination velocity.

The design of a GaAsP/Si three-terminal double-junction solar cell device is also presented in this work. This device design to be fabricated through LPE has been simulated and has a theoretical efficiency of 37%.

## 5.2 Future Work

Further improvement to the quality of the epitaxial GaP growth layers on Si must be achieved before continuing with subsequent III-V material growth for photovoltaic device applications. Once an acceptable GaP buffer layer is achieved, the design and fabrication of three-terminal double-junction solar cell devices may proceed. Figure 5.1 shows the efficiency of such a device as a function of the bandgap of the top solar cell. With a GaP solar cell as the top cell as shown in figure 5.2 and with a bandgap of 2.26 eV, the maximum theoretical efficiency of this device structure on a Si solar cell device is 38%.

J. C. Fan *et al* has predicted efficiencies over 30% under multiple suns for inexpensive two-cell tandem modules with Si as the bottom cell and GaAs-AlAs or GaAs-GaP system as candidates for the top cell with a bandgap of 1.75 to 1.80 eV [19]. Based on experimentally achieved open-circuit voltages and assuming a quantum efficiency of unity and realistic losses, a maximum efficiency of 32.1% under the AM1.5 global spectrum for a four-terminal system configuration consisting of a Si bottom cell and a top solar cell with a bandgap of 1.85 eV is predicted by M. Nell and A. Barnett [20]. This characteristic can be achieved in a solar cell device with



Figure 5.1: Three-terminal double-junction solar cell efficiency as a function of the bandgap of the top solar cell with Si as the bottom solar cell



Figure 5.2: Selectively grown GaP solar cell on a Si solar cell

the materials GaAsP or InGaP for the top cell. At the desired bandgap, the lattice constant of GaAsP is much closer to the lattice constant of the GaP buffer layer than that of InGaP, which makes GaAsP a more appropriate choice of material. This designed device structure is presented in the previous chapter and is depicted in figure 5.3.



Figure 5.3: A GaAsP solar cell grown on a Si solar cell

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## Appendix

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