HIGHER DEFINITION MID-WAVE INFRARED SCENE PROJECTORS VIA SHRINKING PIXEL PITCH

by

Miguel Angel Hernandez-Raya

A dissertation submitted to the Faculty of the University of Delaware in partial fulfillment of the requirements for the degree of Doctor of Philosophy in Electrical and Computer Engineering

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ABSTRACT

The role an infrared scene projector (IRSP) plays in the qualification of infrared (IR) detection systems is to provide realistic simulated scenarios in a lab setting. As IR sensors become ever increasingly complex, there comes a critical need for projection technologies to provide a means of testing. This method of hardware in the loop (HWIL) implementation reduces the cost and time of development. As a result, research and development (R&D) groups in industry and the military have a large interest in IRSP technologies. The IRSP technology to be discussed uses light emitting diodes (LED) to produce mid-wave infrared (MWIR) signatures. Going forward, IRSP systems need even higher resolutions coincident with increased projection speeds. A new read-in integrated circuit (RIIC) architecture is necessary to push this technology forward towards these higher resolutions. Using various very-large scale integration (VLSI) techniques, the new RIIC architecture is designed to be modular and scalable for emitters with different characteristics. The new RIIC architecture has be designed using the ONC18 process from OnSemiconductor. The base pixel has been made 4X smaller than the current state of the art RIICs for LED-based IRSPs. The principal reason for exploring a smaller pitch has been to test the theory of better light extraction from the Super-lattice LED (SLED) arrays. The SLED pixel is grown on a gallium-antimonide (GaSb) wafer using a cascade approach that increases aggregate light output. The RIIC pixel has been characterized using a testing platform that provides the digital patterns needed to drive the static logic, and the IV characteristics of every pixel were collected using a Keithley 24XX meter. The SLED pixel has been characterized using an indium-antimonide (InSb) detector. LIV curves have been generated to compare variable size parts. Hybridization of the prototype part has not been performed, however, controlling the SLED pixel with the RIIC pixel has been

demonstrated. LIV curves for these experiments were collected via the Keithley meter in conjunction with a forward-looking-infrared (FLIR) 6800 camera.

Chapter 1

INTRODUCTION TO INFRARED SCENE PROJECTORS

Figure 1.1: IRSP developed at the University of Delaware. 1. Scene generator PC, 2. Close Support Electronics (CSE), 3. IR LED emitter array mounted in a Dewar package, 4. FLIR camera

The academic, military, medical, automotive, and space industries, to name a few, have found many uses for infrared (IR) imaging systems. Such systems have sensors that capture wavelengths of light below that of the visible spectrum. Different types of wavelengths can reveal different information about the environment around us. This understanding has led to the development of many different systems using the IR spectrum. Some examples of systems that interpret IR light include things such as night vision goggles, IR cameras, communication systems and gas detectors.

When dealing with very complex and expensive systems, it becomes increasingly important to ensure that the IR components work as designed. Characterizing such components is a necessity for quality assurance of the system. For this reason, infrared scene projectors (IRSP) are of great interest in the field of system development. IRSPs

are tools that aid the testing and evaluation of complex IR systems by providing heat signatures needed to stimulate the sensors. More specifically, instead of performing costly field tests, the unit under test (UUT) can be tested in a laboratory setup using IRSPs. Using a hardware in the loop (HWIL) configuration, the IRSP can provide realistic projected scenarios to the UUT.

At the University of Delaware (UDel), we have developed a stable and reliable light emitting diode (LED)-based IRSP that has been used at different labs in various HWIL configurations. The current components that make up an IRSP system are shown in figure 1.1. Referring to the figure, a scene generation computer is the high-level interface that provides a graphical user interface (GUI) with all the necessary control functionalities[9]. Furthermore, the scene generation computer pre-processes and bit-packs all imagery to be displayed by the projector[10, 11]. The close support electronics (CSE) is the link between the output imagery of the scene generation computer and the display. The CSE contains all the hardware needed to process the data and put it into a format the read-in integrated circuit (RIIC) component of the display can interpret as an image[12, 13, 14, 15]. The display LED array, or hybrid, is housed in a commercial off-the-shelf (COTS) Dewar that allows us to run the system at 78 K. For in-house development purposes only, we use a FLIR Systems Inc. camera, model SC6800 or SC8200, to gather data for our IRSP research[16].

One of the oldest types of emitters is the resistor array. The way resistor arrays emit in the IR spectrum is fairly simple. Heat produces a wide range of IR wavelengths; by heating up the component, a small Microelectromechanical (MEM) resistor will produce heat, hence IR light. Honeywell was one of the first companies to make this technology commercially available, especially for military applications. This was the first type of IR projector that could produce dynamic imagery, which made it popular for testing systems equipped with IR detectors. Today there are many more technologies that can project in IR, including light emitting diodes, lasers, liquid crystal displays, and carbon nanotubes. However, they are at different stages of research and development (R&D).

1.1 Contributions and goals of this dissertation

1.1.1 My contributions

- Laid out foundations for future 4Kx4K resolution infrared emitter array.
- Created the first 12 μm pixel pitch RIIC architecture.
- Proposed novel design for super-pixel architecture.
- Designed wafer testing procedures for RIICs.

1.1.2 Goals

The work explored in this dissertation pushes the current limitations of LED-based IRSPs to create a path towards a future 4Kx4K emitter array. A need for higher efficiency arrays was the first goal of this project. The work explored a method for increasing light output of arrays via shrinking the pixel pitch. Another goal has been to create a path towards developing higher resolution arrays to make use of the smaller pixel size. Furthermore, I hope this dissertation helps develop the next generation of high definition IRSPs.

Chapter 2

BACKGROUND ON IRSP TECHNOLOGIES

In the IRSP field, there is only one well-known technology, the resistor array. However, there are other technologies trying to disrupt the market. This is a direct result of the shortcomings of the resistor array technology. Some of these technologies include liquid crystal display (LCD), carbon nanotubes (CNT) and LED arrays. Some of these are more mature than others, and each has its pros and cons. This chapter briefly describes the different technologies.

2.1 Resistor Arrays

The resistor array technology for IRSP systems is the only one being used commercially, as it was the first technology to successfully produce dynamic scenes in the IR spectrum. Working for Honeywell, Barrett E. Cole and Chien J. Han filed the first patent on the technology in 1994. The concept for the technology is very simple. An electrical current flows through a resistor and causes that resistor to heat up generating IR signatures. A single pixel is composed of a small serpentine resistor. The entire structure of the resistor is suspended over the pixel driver to avoid transmitting the heat down to the silicon structure of the driver[1]. Additionally, this structure avoids lowering the temperature of the resistor and increasing the rise time. Overall, this tuned cavity helps get more energy out of the resistor. In figure 2.1, both the physical structure of a resistor pixel and the schematic for it can be compared side by side. Resistor pixels are grown individually on top of a silicon read-in integrated circuit (RIIC) that uses complementary metal-oxide-semiconductor (CMOS) technology. The drive transistor is connected in series with the serpentine resistor, as the transistor controls

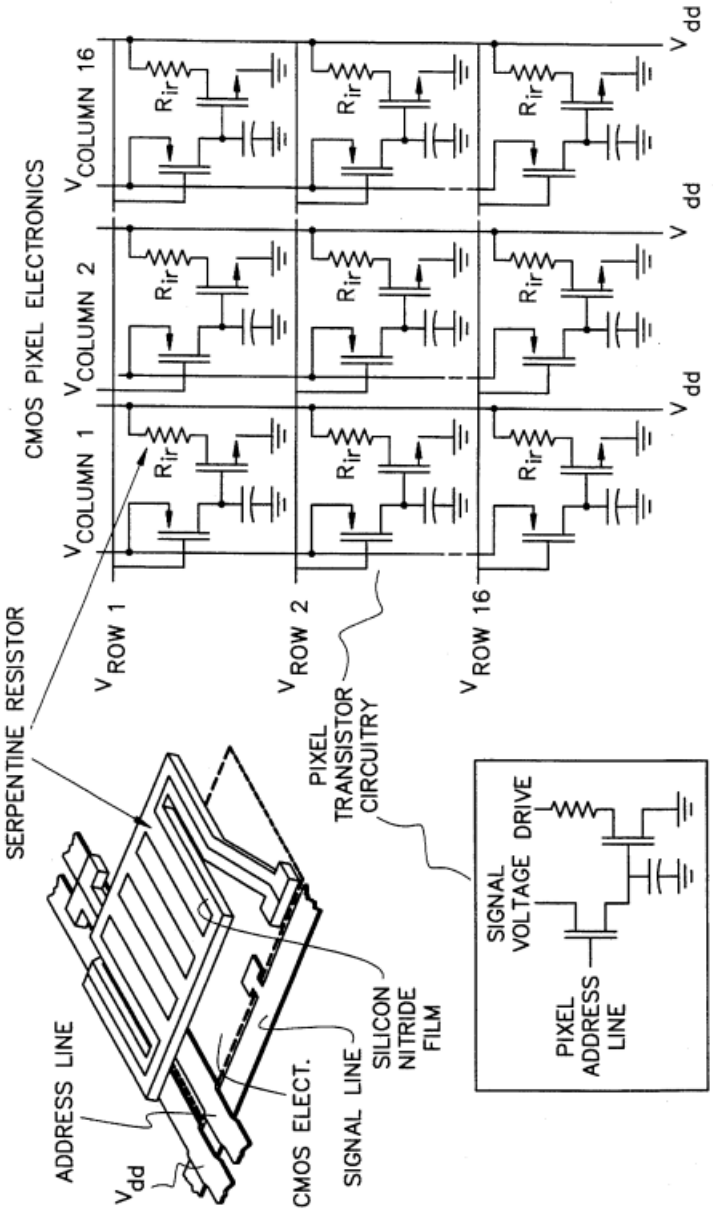


Figure 2.1: Structure of a resistor array for an IRSP[1]

the resistor's current flow. A second transistor acts as the address line and signal voltage for the main drive transistor[1]. The emitter array is formed by connecting many of these devices in parallel, effectively forming a square grid.

After Santa Barbara IR (SBIR) licensed this technology from Honeywell, they

became the only commercial producers of IRSPs [17]. In 1999, SBIR developed their MIRAGE projector. It was specifically designed for HWIL testing of missile seekers, IR cameras, and other tracking systems. Their first system was a 512x512 array that could produce apparent temperatures of 475 K. Their newest model, the MIRAGE XL has a resolution of 1024x1024 and an apparent temperature of up to 650 K[18]. Apparent temperature is measured in radiation density, and it is thermographically equivalent to the radiation a hot object, usually a blackbody, emits in the same spectral area of interest[19].

Resistor arrays proved that projection in IR has great value, however, in recent years there has not been any major improvements in the technology. The current pixel pitch in resistor arrays is 48 μm as SBIR has not successfully created an array with smaller pixels[20, 17, 18].

2.2 Liquid Crystal Display

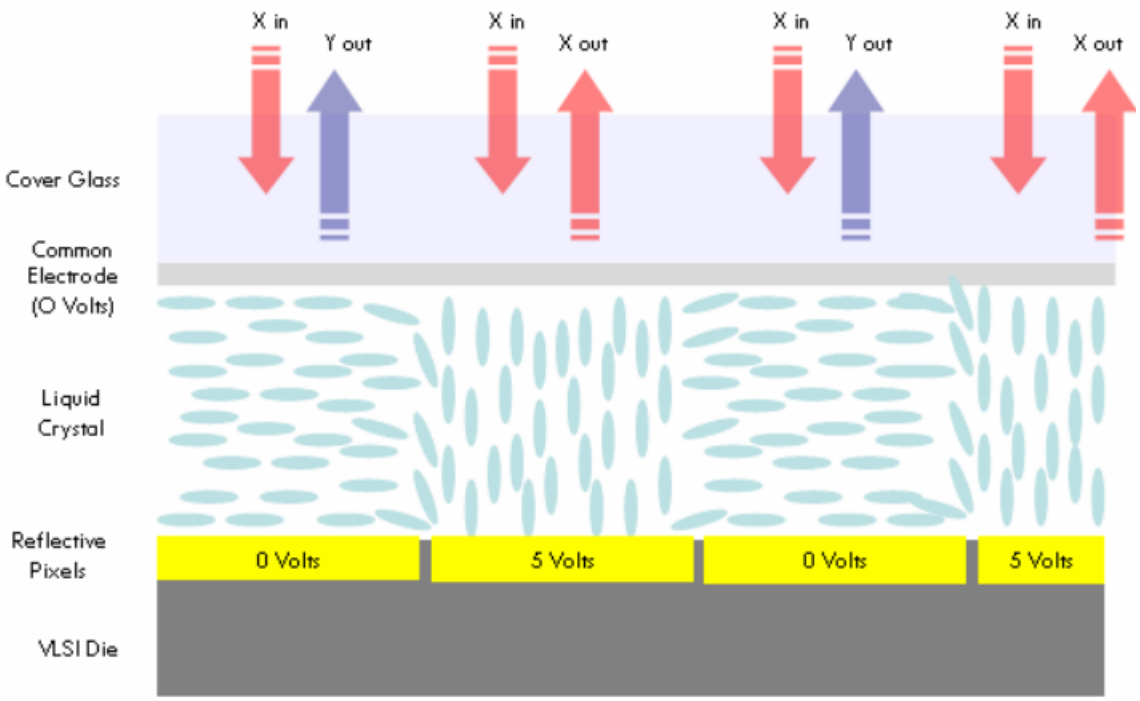


Figure 2.2: Structure of a resistor array for an IRSP

Liquid crystal display (LCD) technologies have also made an appearance in the IR projection business. LCD technologies work by having a very high power, broad spectrum back light providing the illumination. An example of this technology is the BAT IR 4300 projector made by Kent Optronics. The display resolution for the model is 512x512 pixels, which can run at 140 Hz with a resolution of 12 bits[21].

A more recent LCD technology is liquid crystal on silicon (LCoS). An LCoS uses the same concept as an LCD with the exception that the light doesn't initially come in via a backlight, but rather from a front source of illumination. After processing by the device, the light exits as a reflection through the front of the display. This is better understood by studying figure 2.2, where *X-in* represents linearly polarized light which travels down the structure. The second layer is a layer of conductive material that is very thin and transparent and acts as a common electrode. The liquid crystal layer is sandwiched between the electrode material and the silicon die. The silicon die is divided into many pixels, each plated with metal that provides the medium for changing the angle of the crystals and acting as a mirror that reflects the incoming light[22].

Unfortunately, LCD displays for IRSPs have a significant absorption disadvantage. LCDs rely on an external source of light to produce images, and this light is often very bright and a significant source of heat. When the light travels through the LCD structure, absorption begins to occur, leading to the heating of the display. Local heating in an LCD array is overlooked and not very crucial in the visible spectrum; however, when a device gets hots in the IR spectrum, undesirable IR signatures are generated. Other IR technologies are also affected by local heating.

The material used in LCDs is not the best choice for IR light. LCoS displays have also not achieved sufficiently rapid response times. For IR projection, the required thickness of the liquid crystal layer increases, thus reducing the response time of the display[22].

2.3 Carbon Nanotubes

A carbon nanotube (CNT) is a form of very thin carbon graphitic sheet that is rolled up into a needle-like tube. The fullerence used is C_{60}, as this forms the hexagonal lattice needed to form the cylindrical shape of the tubes. The growth process is done via arc-discharge evaporation and the structure grows on the negative end of a carbon electrode in an argon-filled vessel[23].

Recently CNT technology has been shown to have the capability of emitting in the IR spectrum. Different than an LED transistor configuration, where the participating carriers are injected into the LED via the source or the drain, researchers have claimed that single-walled semiconducting CNT can generate the carriers locally when a single type of carrier, either e^- or h^+, is accelerated under a high electromagnetic field[24]. However, the application of this technology is fairly novel in the field of IR projection. The concept has been proven at very small scales, and it will be some time before CNT can be compared to other projection technologies at the same level[23, 24, 25].

2.4 Light Emitting Diode Arrays

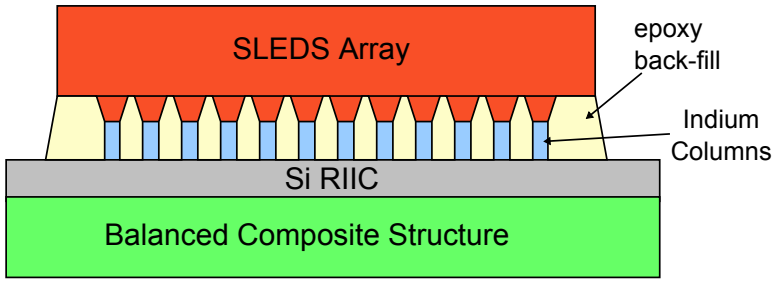


Figure 2.3: Composition of a SLED array hybrid

IRSPs that use LED arrays have been studied since 2008, beginning as a collaboration between the UDel and the University of Iowa (UIowa). An IR LED array has two parts to it, the RIIC, a chip that contains all the electrical pixels that control the radiance output of the LEDs and also provides communication to a system, and

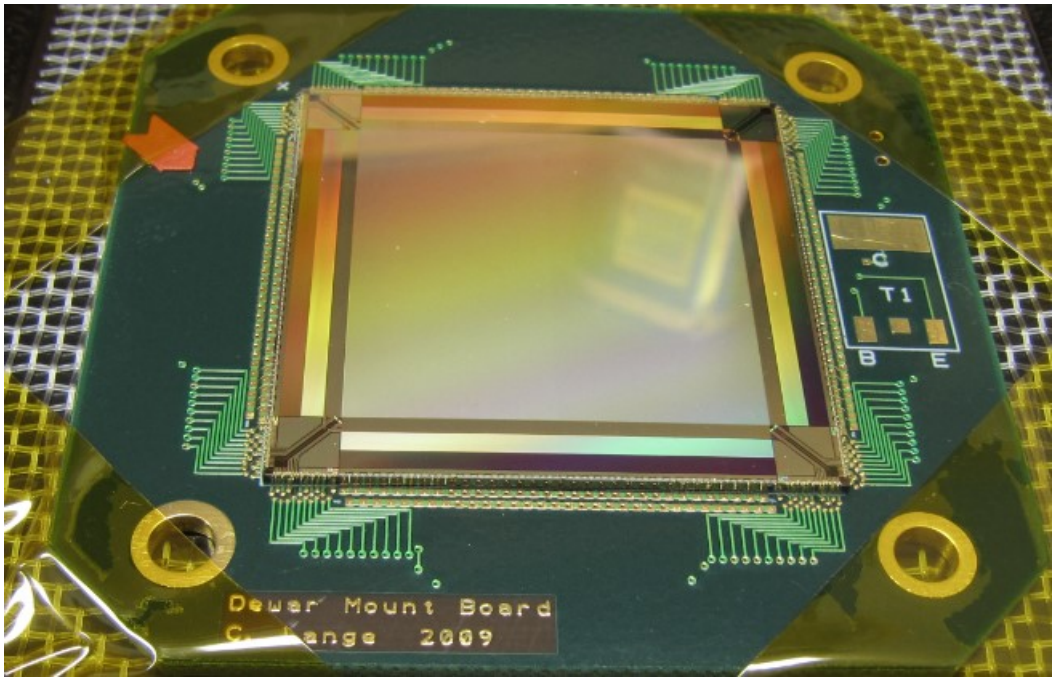


Figure 2.4: Hybrid after flip-chip bonding, and wire bonded to a carrier board

the Super-Lattice LED (SLED) array, grown on a gallium arsenide (GaSb) semiconductor wafer using Molecular Beam Epitaxy (MBE)[3]. The RIIC and the SLED array are hybridized together using flip-chip bonding, creating a single part called a SLED hybrid as shown on figure 2.3. The RIIC and the SLED array are mirror images of one another on the side that has the contacts. Indium bumps are placed on the metal contacts for both, and then the RIIC and the SLED array are pressed together. The final step is to add epoxy in the remaining gaps to add an extra reinforcement to the component. The epoxy does not affect in any way the optical coupling of the array.

The final SLED hybrid is shown in figure 2.4. The emission area of the hybrid is the innermost square; this is where the SLED array is bonded to the RIIC. It is important to notice that the RIIC is larger than the SLED array. This is because the RIIC also has to interface with the mounting printed circuit board (PCB), thus the extra space around the emission area contains all the pads necessary for wire bonding[26].

Chapter 3

EVOLUTION OF SUPER-LATTICE LIGHT EMITTING DIODE INFRARED PROJECTORS

3.1 Super-Lattice LED System

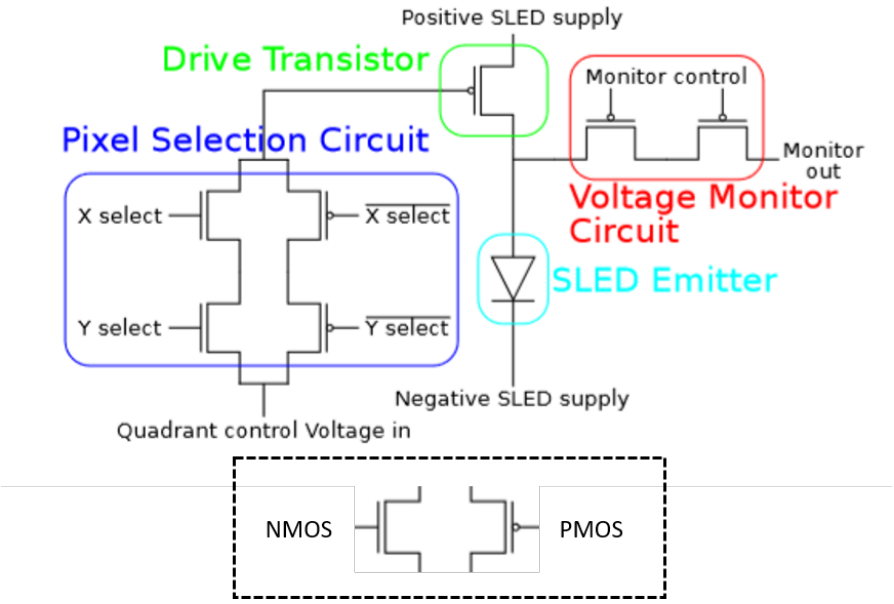


Figure 3.1: Schematic of a single SLEDS pixel. Different sections of the circuit are marked. The drive transistor, pixel selection circuit and the voltage monitor circuit are part of the RIIC. The SLED emitter is part of the SLEDs array.

In 2014, our team at the University of Delaware made the first successful IRSP system using IR LED technology. The emitter array had a 512x512 resolution with a 48μm pitch. We called our first LED IRSP the super-lattice LED system (SLEDS). The SLEDS uses the hybrid scheme approach described in section 2.4 to project light out of the IR LEDs. Figure 3.1 shows the schematic for a single pixel on the SLEDS

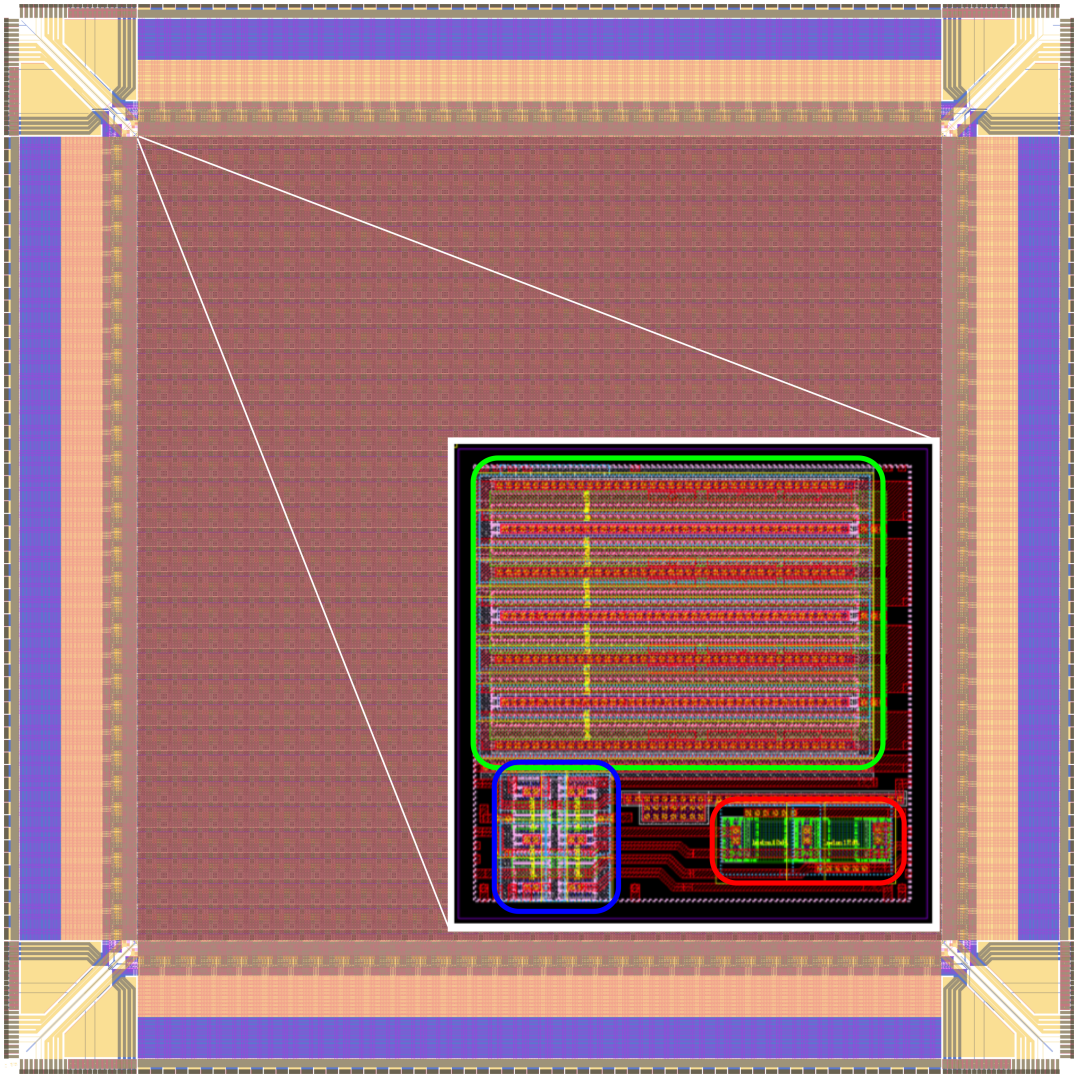


Figure 3.2: SLEDS RIIC layout and a zoomed-in single pixel layout. The colors in the zoomed in pixels highlight the different sections of the circuit shown in figure 3.1.

hybrid array, and figure 3.2 shows the SLEDS RIIC layout and a zoomed-in image of a single RIIC pixel.

Each individual pixel on the hybrid array has a dedicated circuit on the RIIC controlling when the pixel is on or off via a very simple double chain of transmission gates that act as the selection circuit. In a CMOS process, a transmission gate is formed when an n-type metal oxide semiconductor (NMOS) transistor is connected in

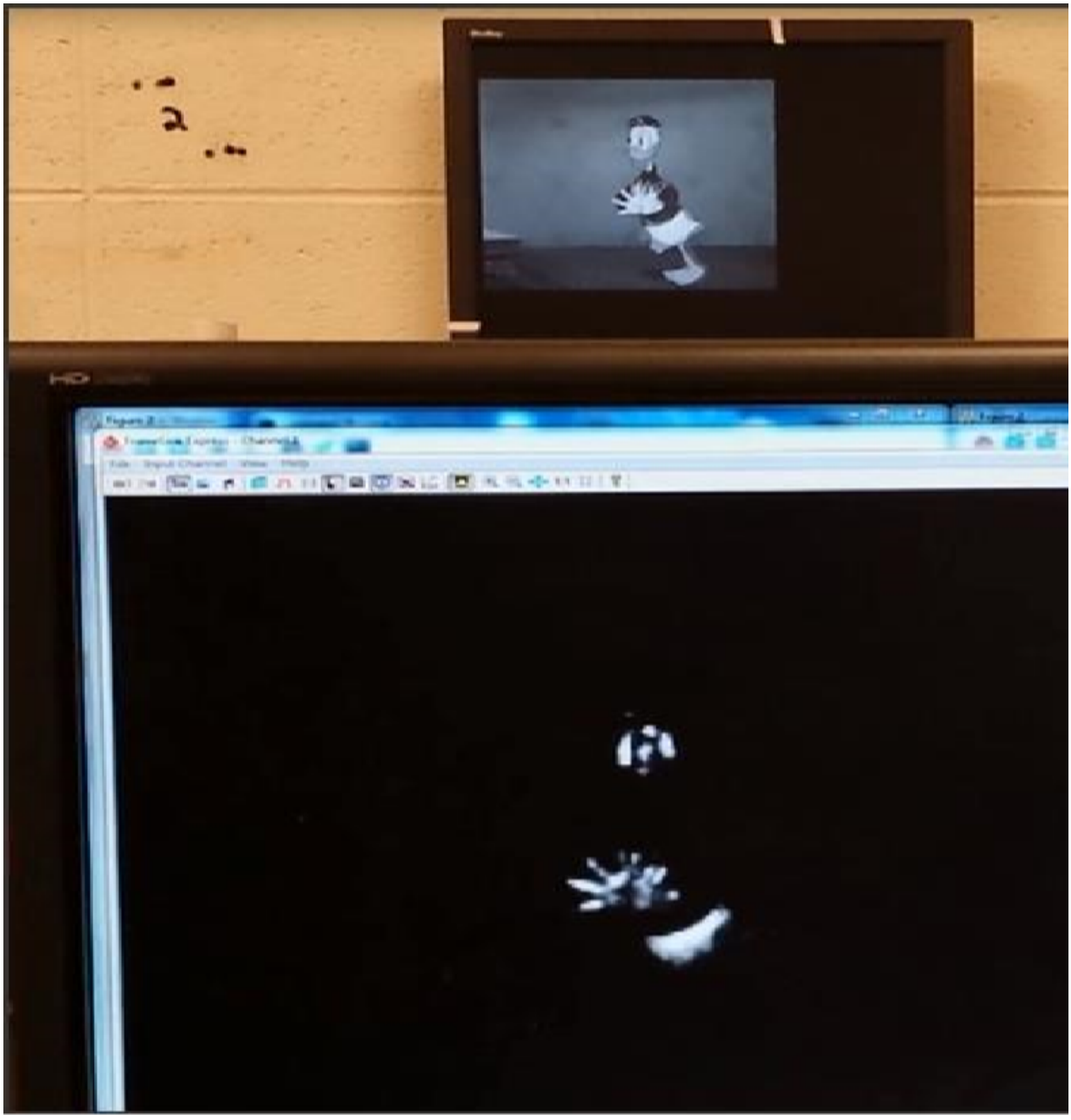


Figure 3.3: Donald Duck being displayed on the SLEDS.

parallel to a p-type metal oxide semiconductor (PMOS) transistor. The gates of both transistors are connected to a complementary signal. For example, if a signal A is applied to the gate of the NMOS transistor, then the signal $\overline{A}$ is applied to the gate of

the PMOS transistor. In simple terms, both MOS transistors will turn off at the same time and turn on at the same time, enabling or disabling the signal that passes through. The rest of the pixel circuit consists of a drive transistor and a monitor control. The drive transistor is controlled by the *Voltage in* signal and provides a path for current to flow to the LED. The PMOS monitor control chain allows us to verify the pixel is functional by monitoring the voltage going to the LED[26, 27, 28].

To get a better perspective, the various pieces of the circuit have been encircled with different colors in figure 3.1. In figure 3.2, the zoomed-in layout for a RIIC pixel has also been marked with the same colors to make a good correlation between the two. However, the LED is not shown on the layout because it is a separate entity on the SLED array.

The early SLEDS had many successes, including being tested at different laboratories in the country, running at 100 Hz, and generally demonstrating that the technology is possible. However, given the prototype nature of this first projector, the SLEDS did not have the linearity and dynamic range necessary to produce very realistic test scenarios[29, 30]. This limitation results from the drive transistor having been designed to accept large current loads to make the LEDs as bright as possible. The downside of this is that the transistors have curves of a seemingly digital nature, almost like a clock pulse, between the off-state of the PMOS driver and the on-state. This results in all of the output imagery being binary, either full-on or full-off, with little to no grayscale in between. Figure 3.3 is a perfect example of what would be seen projected on the SLEDS array. The top image on the small monitor is the actual video input fed to the SLEDS projector, and the bottom screen shows the output captured by a mid-wave infrared (MWIR) camera. On the output image, only the white parts of Donald Duck are visible, while everything else is very dark or completely off[27, 26].

3.2 Two Color SLED Array

After the development of the SLEDS, a number of modifications have been proposed and investigated. One of these is the two color SLED array or TCSA. The

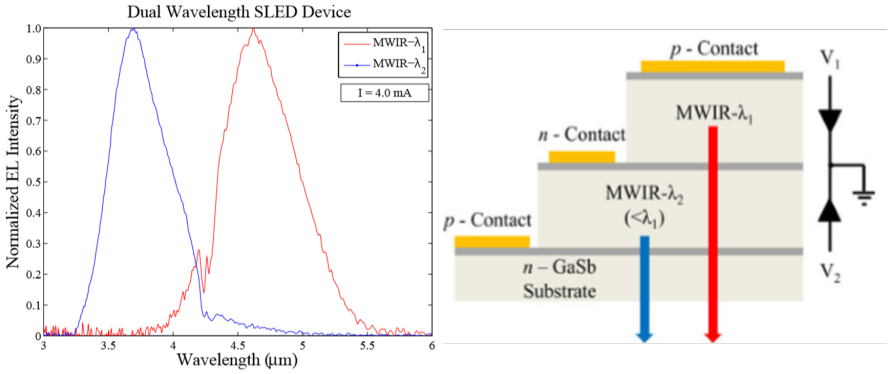


Figure 3.4: TCSA pixel wavelengths are shown on the left[2]. The shorter wavelength (MWIR-λ_2) is refer to as blue, and the longer (MWIR-λ_1) is refer to as red. The stack structure for the TCSA pixel is shown on the right[3, 4].

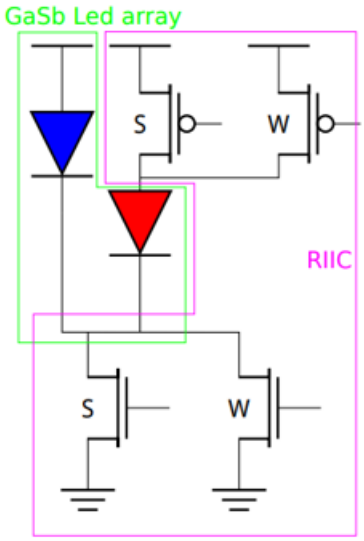


Figure 3.5: TCSA drive circuit with two gears per color. The red LED is driven by a pair of PMOS transistors and the blue LED by a pair of NMOS[2].

goals of the TCSA project were to develop a system able to display in two different wavelengths in the MWIR region and to increase the dynamic range missing from the SLEDS.

The TCSA system has introduced the first LED-based IRSP to use dual emission in two different wavelengths from a single SLED structure[31, 32, 3, 8]. Additionally,

in the TCSA system, we changed the pixel circuit on the RIIC to improve the dynamic range over the SLEDS. The SLEDS has only one, very strong, drive transistor. In the TCSA, a second, smaller transistor has been added. We refer to the differently sized transistors as gears, the smaller transistor being the weak gear and the larger transistor being the strong gear. These two sizes allow better control over the grayscale for background imagery, and hot objects can be drawn using the stronger of the two. Because the TCSA has two colors per pixel, each of the individual colors uses a pair of drive transistors. Figure 3.5, shows a simplified version of the pixel circuitry of the TCSA. Note that because of the structure of the TCSA pixel stack, the λ_2 (refer to as blue for simplicity) LED uses a pair of NMOS drive transistors, and the λ_1 (refer to as red) LED uses a pair of PMOS drive transistors. This results in the red LED not being independently driven as it also depends on the NMOS transistors to have a path for current flow[14, 33, 34, 2].

3.3 Night Glow SLED System

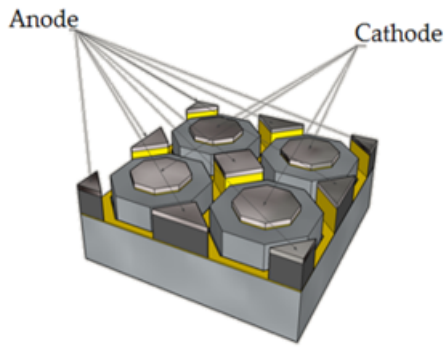


Figure 3.6: The NSLEDS super-pixel consists of 4 pixels sharing a common anode contact[5].

The gap between the resolution of the Focal Plane Arrays (FPA) and the resolution of projectors used to test them has been increasing. A 512x512 resolution IRSP is not enough to test a 1Kx1K FPA. Ideally, multiple IRSP pixels would map to a single FPA, not the other way around. The Night Glow SLED System (NSLEDS) is part

of the third generation of IRSPs, which tries to meet the performance criterion that FPAs require for accurate testing[35]. The NSLEDS uses a single color array in the 3-5 μm wavelength range. This new generation of emitter arrays has a reduced pixel pitch of 24 μm, effectively reducing the pixel area by a factor of four compared to the TCSA pixel. As a result, the total resolution of the array is increased from 512x512 to 1Kx1K[5].

The NSLEDS RIIC pixel has also changed; the drive circuit consists of two NMOS transistors. Similar to TCSA, one drive transistor is bigger and can output larger currents, and the other is much smaller in size, providing smaller currents for the grayscale of background objects. Unlike TCSA, there are no PMOS drive transistors, as they are less efficient and require more space.

In addition, the SLED pixels have been grouped in fours. An ordinary LED pixel requires an anode and a cathode contact to function. Since in the NSLEDS array the pixel area has been reduced, to maintain a high emission area on the LED, we want to reduce the space needed by the metal contacts. Therefore, each group of four pixels shares a common anode centered between them, as shown in figure 3.6. Additionally, there are pieces of anode contacts for every group of four pixels. These smaller anode contacts form complete contacts when tiled to others. We refer to this structure as a super-pixel[5].

3.4 High Definition IR LED

Five NSLEDS arrays have been produced to date. Each of these has had slight variations during the assembly process to test different features and obtain the best emitters possible. The High Definition IR LED (HDILED) system is an extension of NSLEDS. Both the HDILED and the NSLEDS arrays can be considered to be of the third generation of LED-based IRSPs. Just as in NSLEDS, the HDILED pixel pitch is 24 μm, and HDILED uses the same RIIC pixel to drive the SLED pixel. HDILED modifies the SLED super-pixel slightly. HDILED retains the center common anode

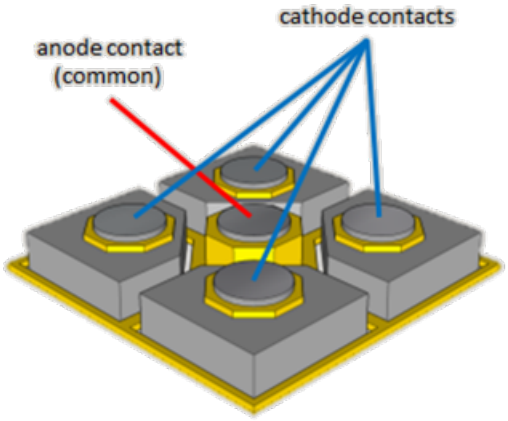


Figure 3.7: In HDILED, the super-pixel has only one common anode in the center[6]

contact per every four cathode contacts, however, the outer smaller anode contacts that the NSLEDS' super-pixel uses are removed to give more area to the cathodes[6, 36].

The HDILED system is the first IRSP to have reached a resolution of 2Kx2K pixels. This is a great leap forward in closing the gap between FPAs and emitters. As of today, two HDILED systems have been completed[37]. One is at our laboratories at the University of Delaware and the other is in a lab facility at the University of Florida hosted by the US Air Force.

3.5 Future IR LED systems

We have demonstrated that LED-based IRSPs are a feasible solution to the requirements of the Test and Evaluation (T&E) phase of IR system development. However, development continues, and we need ways to improve the current technology, as IR systems become harder to test as they become more complex[36]. Developing any sort of IRSP with a resolution of 2Kx2K or more is very complicated and costly using current methods, such as using a Molecular Beam Epitaxy (MBE) machine to grow the SLEDS. Development is also complicated by the poor yield of RIIC parts beyond squared-inch size[38, 39]. Though our HDILED systems are operational, they are not yet capable of meeting the requirements for realistic T&E testing of IR systems. To achieve higher resolution IRSPs in the future with more cost-effective high operability,

several other projects are exploring alternative approaches to achieving these goals. This dissertation discusses a method of increasing the resolution of the arrays by moving to a smaller pixel architecture. Another project with the same ultimate goal is explained in the following subsection.

3.5.1 AIREA

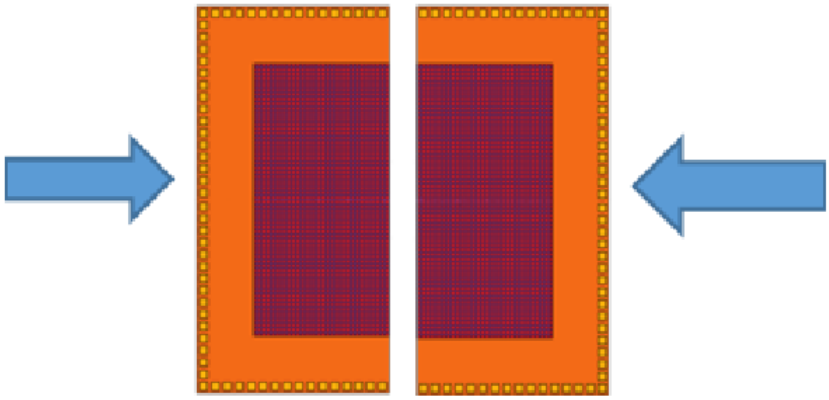


Figure 3.8: Architectural overview of the AIREA arrays[7].

One way to increase the maximum resolution of our IR LED arrays is to combine multiple arrays into one bigger one by abutting them. The Advanced Infrared Emitter Array (AIREA) project grows rectangular RIICs and SLED arrays with a pixel pitch of 24 μm and a resolution of 1Kx2K. After processing, two rectangles are abutted together as closely as possible to create a 2Kx2K single array, as shown in figure 3.8. This process might seem straight-forward, but to achieve the correct etching and alignment of the two arrays has proven to be very difficult. At this time, the abutment has not been achieved successfully[38, 36, 7, 40]. Further details on the AIREA project can be found in Josh Marks' dissertation [17].

Chapter 4

INTRODUCTION TO NEW A RIIC ARCHITECTURE TO INCREASE DENSITY AND EFFICIENCY OF ARRAYS

The Advanced RIIC Technologies to Increase Density and Efficiency of IRLED Arrays (ART-IDEA) project has been funded by the Guided Weapons Evaluation Facility (GWEF) at Eglin Air Force Base (AFB). ART-IDEA is a Small Business Innovation Research (SBIR) phase 1 program, and has been the product of a partnership between the University of Delaware, Chip Design Systems (CDS) limited liability company (LLC), the University of Iowa and Firefly Photonics.

4.1 Motivation for ART-IDEA

A large gap exists between the resolution of FPAs used on IR systems and the resolution of IRSP systems used for T&E. The remainder of this dissertation describes a high risk, high reward effort that looks to develop more efficient arrays with smaller pixels. The prototype parts that have been developed in this effort are SLED chips with various pixel sizes, including 12 μm pitch, and a RIIC chip with a 12μm pixel pitch.

Gordon E. Moore predicted that the number of circuits on a given surface area would double approximately every two years, as verified by the data in figure 4.1. With smaller transistors, there is a possibility of decreasing the size of the RIIC pixel and thus increasing the number of pixels for a given area. The current pixel pitch used by our arrays is 24 μm, and in an area of one square inch, we can fit 1Kx1K pixels. With the proposed architecture of the ART-IDEA RIIC, the goal is a 12 μm pixel pitch with 2Kx2K pixels in our square inch. For all previous generations of RIICs, we have used AMIS500 CMOS technology, where the smallest feature, the minimum allowed length

for a transistor, is .6 μm. For ART-IDEA, we have moved to a smaller transistor technology, ONC18, which has a .18 μm minimum feature size for a transistor.

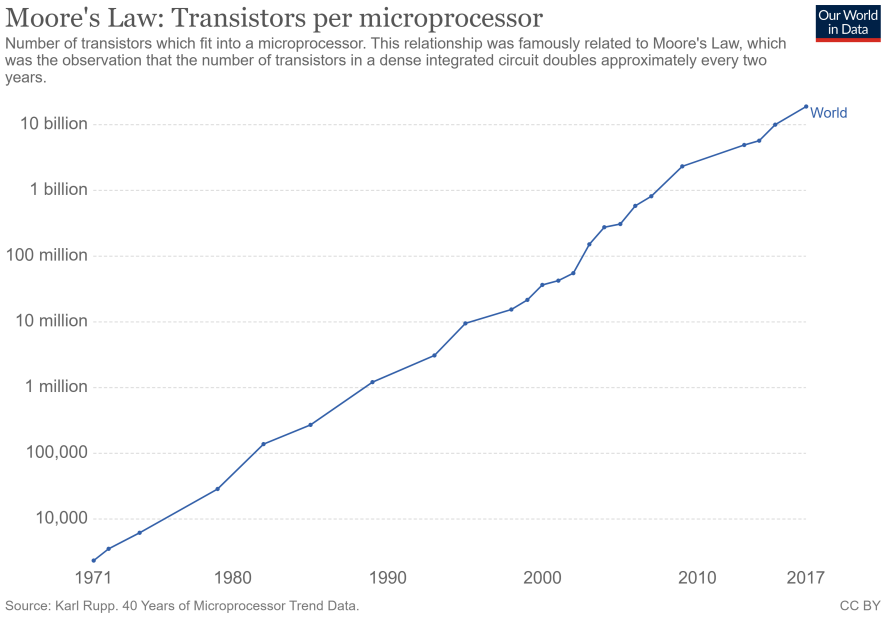


Figure 4.1: Moore's Law data collected over 40 years, showing the expected behavior

4.2 Wafer Yields for RIICs

One of the primary reasons to pursue smaller RIICs is the increase in the number of working parts per wafer. In semiconductor fabrication, the yield of functional chips per wafer is a function of their surface area, human error, design flaws, processing error, contaminants, and individual yields of the various layers. Over time, the fabrication process for semiconductors has been refined to the point where, for many modern wafer processings, the yield may be more than 98%[41, 42, 43]. With the current fabrication technology, most of the issues that cause lower yields become insignificant, leaving only the surface area of the chip as the dominant factor for lower yield[41, 42, 43]. The advantage of smaller chip size is illustrated on figure 4.2, which shows three different 8" wafers we have designed and fabricated at OnSemiconductor. The wafer on the far

left shows a typical TCSA or NLEDS RIIC wafer, the middle wafer has AERIA RIICs, and the right wafer has the HDILED RIICs.

During the early stages of research and development (R&D) of our infrared systems, we had to fabricate and test the different versions of RIICs for the various programs. The RIICs have telemetry that can be configured to access most pixels on the RIIC and measure the drive transistor's output current for both gears. From the wafer testing phase, we could identify those chips that didn't perform as expected.

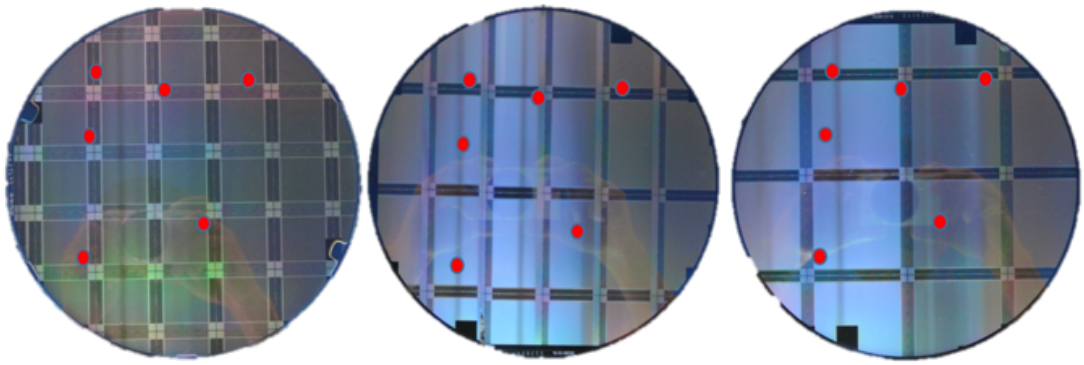


Figure 4.2: NSLED (left), AIREA (middle) and HDILED (right) RIICs on an 8" wafer. The larger chips are more affected by random defects (red dots) on a wafer

4.2.1 Wafer Testing Methodologies

The RIIC is designed to have all digital logic located on the corners of the chip. This logic includes buffers, communication circuitry, bias circuits, shifters, address decoders, and control circuitry. Each of the corners is identical except for being rotated 90 degrees relative to their adjacent corners. The corners are not able to communicate with each other within the remainder of the RIIC circuitry. The carrier printed circuit board (PCB) the RIIC is mounted on must enable such internal communication. As a result of the design, the RIIC is divided into four individually controlled quadrants where each corner's logic controls a quarter of the pixels. To get a better understanding, we can refer to figure 4.3, as it shows exactly the partitioning of the RIIC.

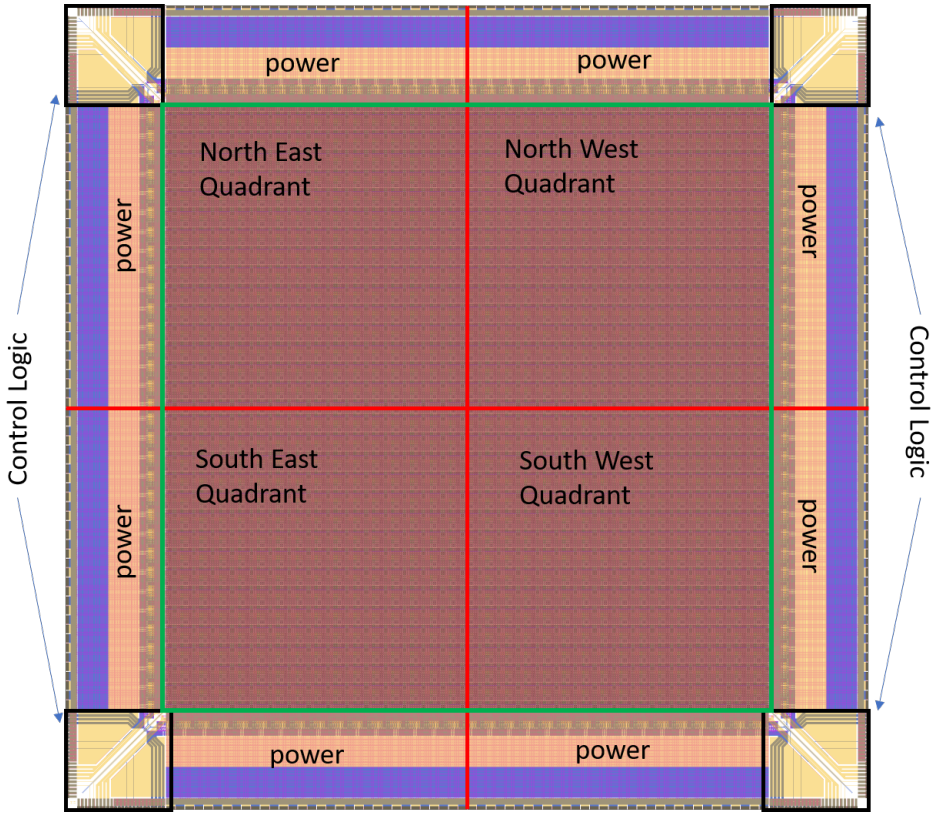


Figure 4.3: Breakdown of the RIIC chip; each of the quadrants is controlled by the appropriate corners containing its digital logic. The rest of the perimeter provides the high power voltage rails and return paths

The RIIC architecture has been designed such that a pixel's data write speed can be controlled by the number of channels active. A channel is simply a path that delivers analog data to a pixel, setting its brightness. A total of seven modes have been implemented in the RIIC architecture, six of them are parallel, and one is serial. The parallel modes activate channels by powers of two. For example, mode-one writes 1 pixel per write cycle, mode-two has two channels active and writes 2 pixels per write cycle, mode-three writes 4 pixels at the time, etc., to mode-six, which uses 32 channels per write cycle. In other words, mode-six is 32X faster than mode-one, but this also requires 32 inputs, whereas mode one only needs one. Apart from the analog inputs, when used in a parallel mode, the RIIC brings all other signals required when writing to a pixel, such as addressing lines, using parallel inputs[16]. Dealing with many signals

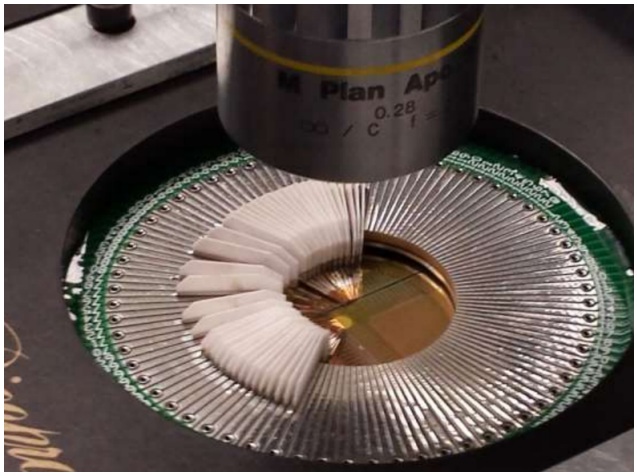


Figure 4.4: Custom probe card used to test RIICs on wafers

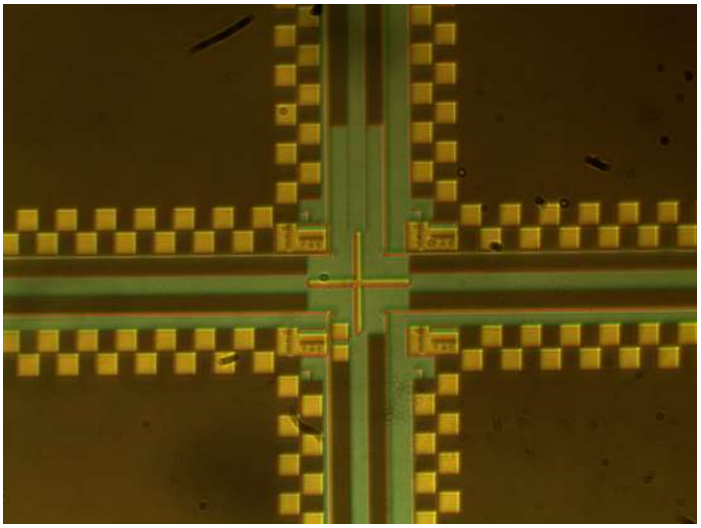


Figure 4.5: RIIC corners under a microscope

makes it extremely hard to test RIICs on a wafer. For this reason, serial-mode has been incorporated on the RIIC. Serial-mode uses the Serial Peripheral Interface (SPI) protocol and combines all the signals required to run the RIIC in parallel mode one into a single stream of serial data[44, 39, 45]. This greatly reduces the speed at which one can write to the RIIC, but during wafer testing, the focus is on determining the

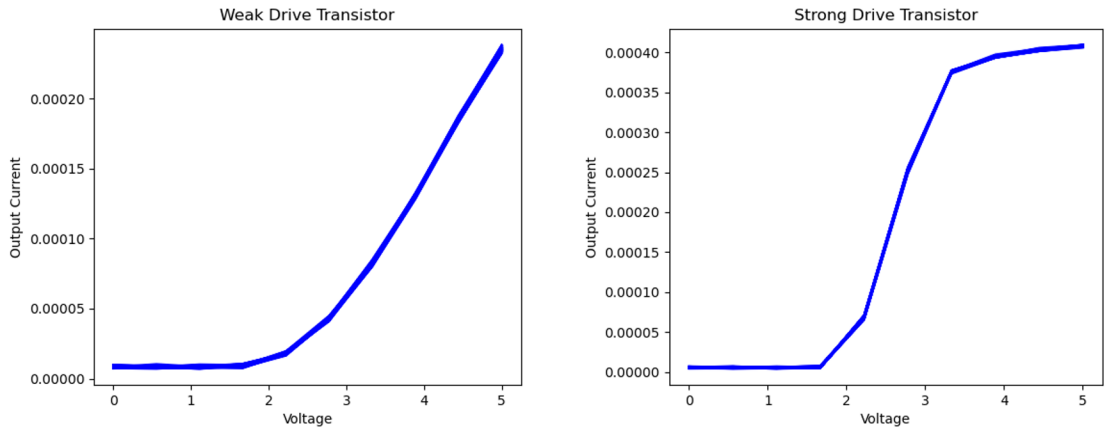


Figure 4.6: Sample curves collected during wafer testing to check if the RIIC chip appears functional

yield of the chips, thus speed is not important.

As shown in figure 4.4, we have designed a custom probe card that allows us to specifically select the RIIC pads required to run the chip in SPI mode. The probe card is a DC Multi-Contact Wedge (MCW) card. The probes are routed to four 26-pin dual row connectors with .1 inch pitch. The probes are separated by a distance of 150 μm in a zig-zag pattern[46]. Figure 4.5 shows an area of the wafer where four RIIC chips meet. The probe card only contacts one corner at a time; if we wish to test a different corner of the same chip, we must rotate the wafer to match the orientation of the probe card. To test all RIICs on a wafer, we 1) pick a corner of the chip, align the probe card and make contact. Then we perform a continuity test on certain points on the card to test for good contact. 2) Test all of the power rails for shorts against ground or other power rails. 3) Use the SPI features of the RIIC, program the chip to sweep the first ten drive transistors in weak gear, then in strong gear. The sweeps run from 0 V to around 5 V, depending on the chip, in ten increments. The current output of the drive transistors is measured, collected with a Keithley 2400 meter and plotted, as shown in figure 4.6. 4) If the RIIC appears good, we use a pseudo-random pattern to sweep 1 of every 10 super-pixels in the quadrant under test for both their

weak and strong gears. 5) Once finished with a RIIC, we test the same corner of all other RIICs. 6) Rotate the wafer 90 degrees and repeat steps 1-6 until all corners have been tested[45, 39, 44].

4.2.2 Results of Wafer testing

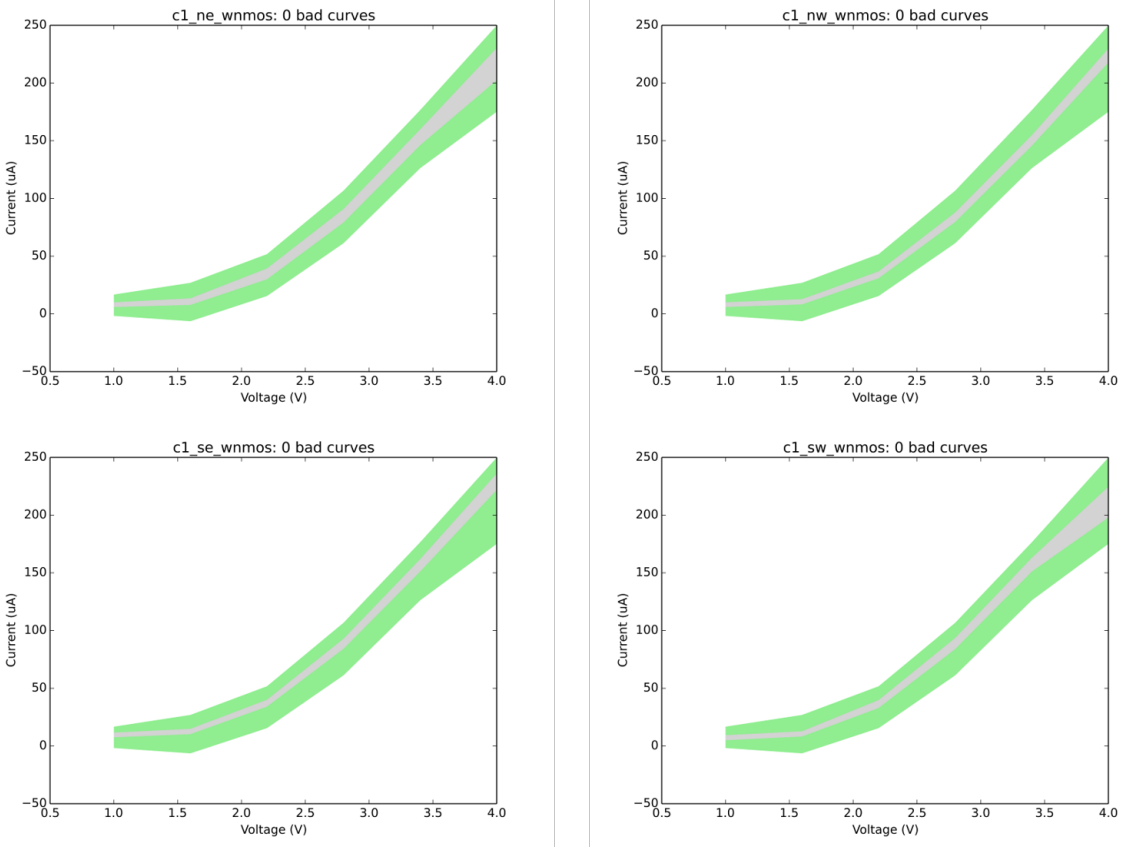


Figure 4.7: Example of NSLEDS transistor yield, candidate for hybridization. Curves represent the current output of the transistors as a function of voltage applied at the gate.

The results obtained during wafer testing are logged and compiled into a database for analysis to guide the selection of the best-performing RIICs. Given the novelty of the architecture design, there are no guidelines or standards as to what constitutes a "best-performing RIIC". We only have simulation data to base our initial conclusions upon. After collecting data from the first wafer, we have made certain observations.

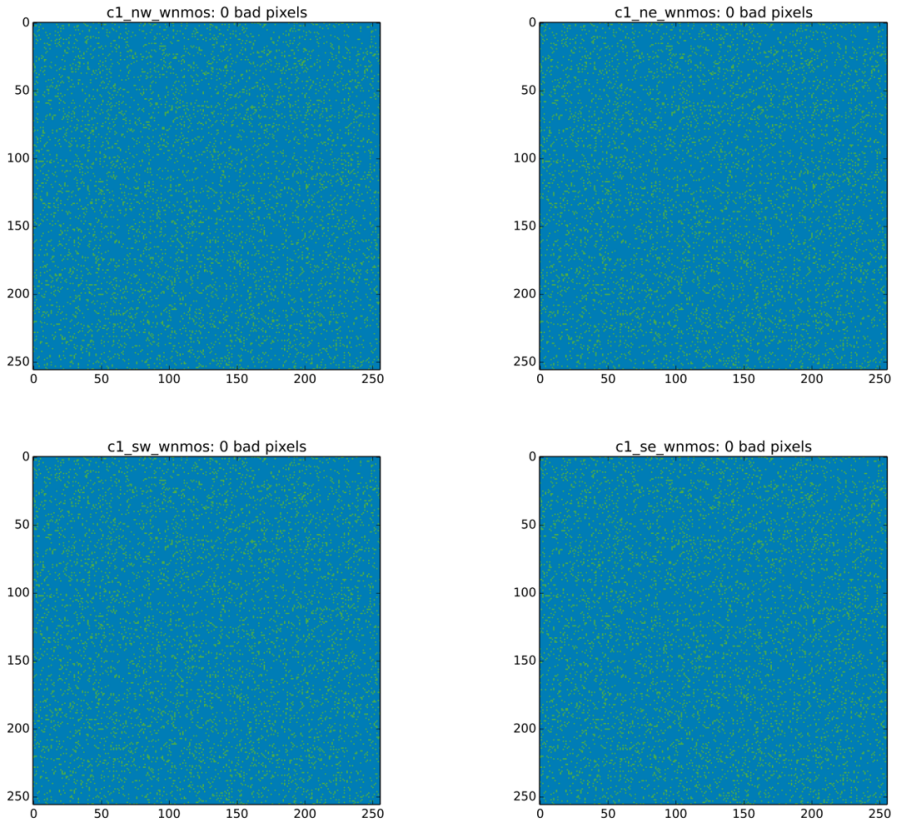


Figure 4.8: Pixel maps for all quadrants of the NSLEDS RIIC shown in figure 4.7; the pixels are mapped one-to-one to their actual locations on the RIIC

A RIIC's performance can vary from quadrant to quadrant, and the current output of the drive transistors can vary slightly in some RIICs. For our final assessment of a RIIC's performance, we have chosen to compare curves within their corresponding quadrants. For a set of curves, the median has been picked as the reference point. The choice of the median has been made because many data points show significant clusters of outliers that would skew the mean of the set. From the median curve, a quantum range has been chosen based on a number of standard deviations. This range is smaller for those points near 0 V, as there is almost no variation, but larger on the higher end where the transistors' output varied more[44]. Figures 4.7 and 4.9 are examples of the visual output our analysis has produced. The green area encompasses the area in

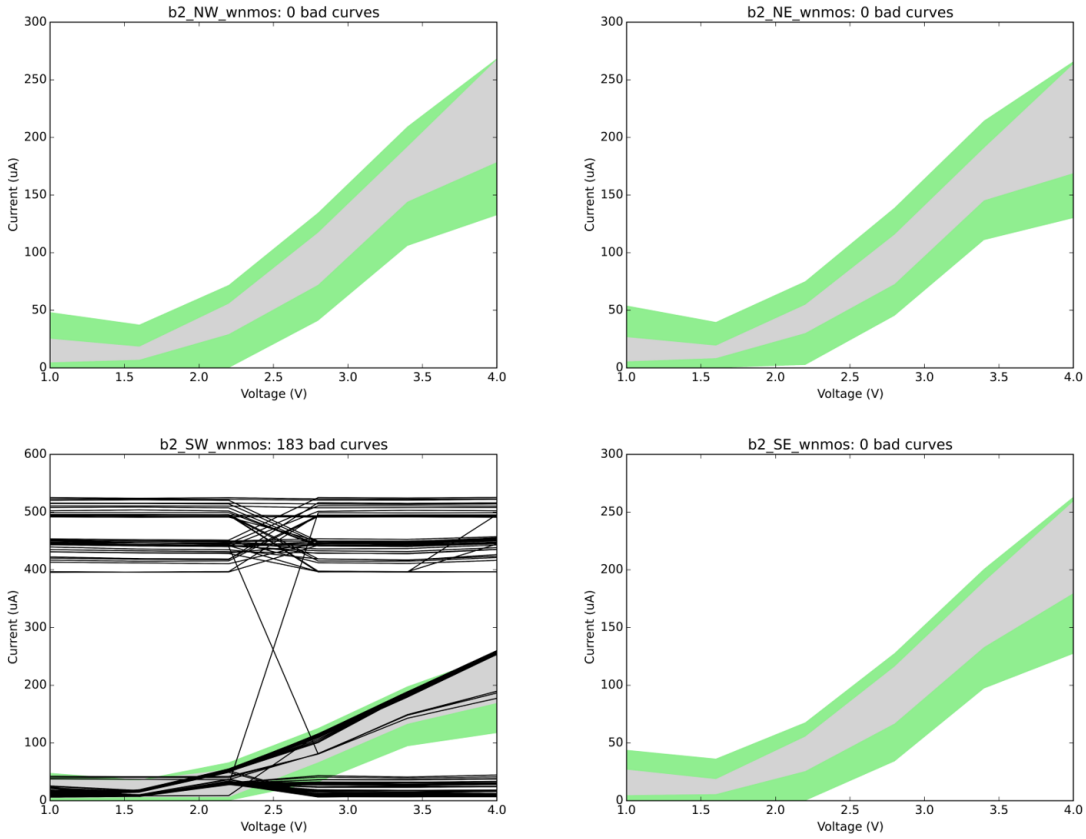


Figure 4.9: Example of HDILED transistor yield, candidate for hybridization. Curves represent the current output of the transistors as a function of voltage applied at the gate. Because of the low yield of such a big chip, parts that had "bad" pixels are considered for hybridization as long as the number is below 1%

which a curve can be considered "good" for the functionality of the RIIC; if a curve goes outside the green area, it is labeled "bad" and thus incapable of driving an LED pixel in a predictable manner. The gray areas on the same figures represent the curves that fall within the given range and are considered "good". The black curves are those that go outside the boundaries of the green area and produce undesired output. For this example, some of the best performing RIICs for NSLEDS and HDILED projects have been chosen[44].

In an NSLEDS or TCSA wafer, it is common to find a few die where 100% of the

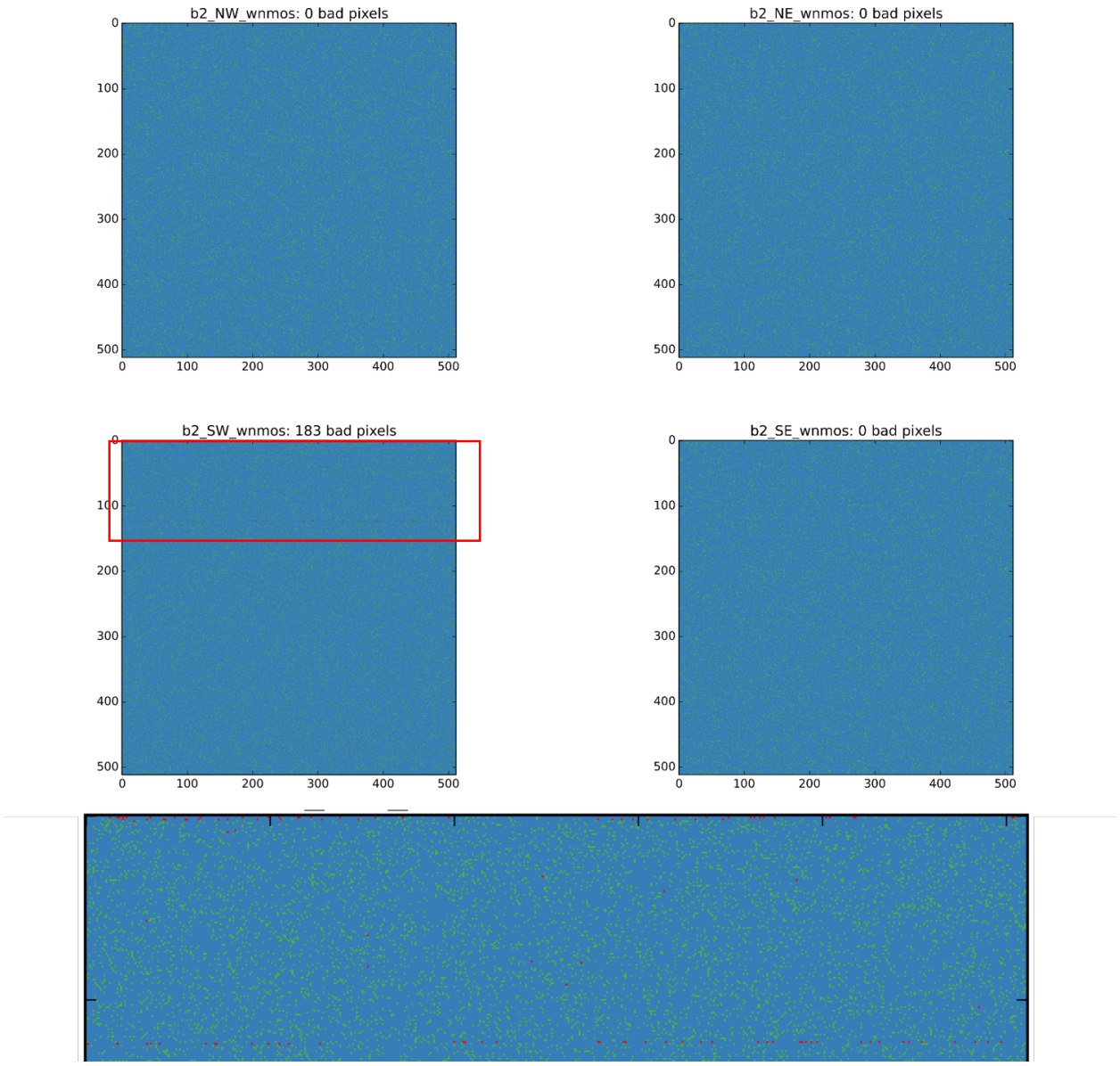


Figure 4.10: Pixel maps for all quadrants of the HDILED RIIC shown in figure 4.9; the pixels are mapped one-to-one to their actual locations on the RIIC. A zoomed-in portion marked by the red rectangle is shown to illustrate where the bad pixels are located. Most of them lie near the to edge, a second row can be seen further down.

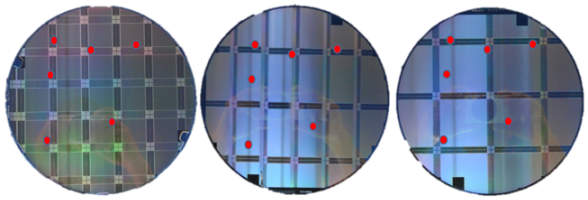
tested transistors output the expected curves. However, for our HDILED or AIREA wafers, this has not been the case. The HDILED set shown in figure 4.9 has a total of

183 detected "bad" curves, representing about .6% of the total curves collected. This is not ideal, but due to the low yields of the HDILED chips, we may choose such dies for hybridization. Figures 4.8 and 4.10 display the exact locations of all the pixels tested. Green pixels are all those labeled "good", yellow are those labeled "bad", the remainder are those pixels not tested by our psudo-random pattern. The scale for the pixel map images is the x-by-y dimensions of the super-pixels. For instance, an NSLEDS RIIC has a resolution of 1024x1024 pixels, so each of its quadrants is 512x512, and since a super-pixel is the grouping of 4 pixels, the scale on the image is 256x256 for each quadrant. The same applies to the HDILED image with the exception that the original resolution is 2048x2048 pixels.

4.2.3 Summary of Yield of RIICs

We know that IRSPs have to reach higher resolutions to keep up with large-format FPAs. Higher resolution means bigger RIICs and SLED arrays. But given the massive drop in wafer yield of the 2Kx2K HDILED, we have chosen to explore other options to increase yield. Lower yields increase the cost of making hybrids, as more wafers need to be fabricated, and more time and resources are allocated to testing them. For NSLEDS wafers, we have found at least 4 RIICs per wafer usable for hybrids; in AIREA wafers that number is 1 per wafer, and in HDILED, only one acceptable RIIC has been found in testing six entire wafers. The architecture for these three RIICs is the same, the only differentiating factor is size. On an 8-inch wafer, 19 NSLEDS RIICs can be grown, 8 AIREA RIICS, and only 4 HDILED RIICS. Figure 4.11 shows the cost per part to obtain a single RIIC. As of 2020, the largest-resolution IRSP in the world is at the University of Delaware, an HDILED system still under development. However, some FPAs would benefit from an even higher-resolution IRSP, but the cost of such a part with the current LED technology would be too high. Maintaining the same architecture would result in a RIIC 4X larger than the current HDILED; fitting only one part per wafer, and dropping yield exponentially[46].

Generation➔	TCSA	NSLED	AIREA	HDILED
Physical size	1"x1"	1"x1"	1"x2"	2"x2"
Cost per die	$1K	$1k	$5k	$30k
Resolution in pixels	512x512	1kx1k	1kx2k	2kx2k



TCSA/NSLEDS AIREA HDILED

Figure 4.11: Cost per part for different RIICs. For the 24 μm pixel design, a 4+ million pixel projector is costly

Chapter 5

DESIGN OF THE TEST CHIP

The goal of this research is to create a prototype that demonstrates the feasibility of increasing the resolution of IRSPs by shrinking the pixel area by a factor of four. There are various CMOS technology libraries that can be used to achieve this result. However, different technologies may have certain advantages or disadvantages with respect to others. The integrated circuit (IC) design to be described in this chapter, has been based heavily on static logic. Static CMOS logic has very low power consumption, and in near ideal conditions, this can be neglected and assumed to approximate 0 W. The only logic not static is that of the last stage of the pixel driver, which uses an analog circuit.

5.1 Picking the right tools for the job

Attributes	AMIS500 5V	ONC18 1.8V	ONC18 3.3V	ONC18 5V
Minimum Feature Size	600nm	180nm	340nm	600nm
Single Device Area	6.40µm²	1.68µm²	1.86µm²	3.66µm²
Metal Layers	5	6	6	6
Thick Metal Option	yes	yes	yes	yes
High Voltage Transistor	12V	15V	15V	15V

Figure 5.1: Comparison of various CMOS technology libraries

To be successful in increasing the number of pixels for LED-based IRSPs, we chose to reduce the pixel pitch of the RIIC and SLED pixel from 24 μm to 12 μm. From the RIIC perspective, there is now only a quarter of the area available for the circuitry as previously allotted. As previously mentioned, the circuitry architecture for all RIICs to date has been created using the AMIS500 technology library from

ON Semiconductor (OnSemi). The AMIS500's smallest-base CMOS is a 5 V with a minimum feature length of 600 nm and area[1] of 6.40 μm. The ONC18 technology library, also from OnSemi, offers more options for smaller transistors. The smallest process is a 1.8 V transistor, with a smallest feature length of 180 nm. A 3.3 V and a 5 V process are also offered, these have a smallest feature length of 340 nm and 600 nm, respectively. Table 5.1 shows a quick overview comparing the AMIS500 technology library to three of the candidate technology libraries offered by ONC18. The most important qualities I looked for when choosing the technology to use are the size of the components in terms of area and minimum feature length, and the range of high-voltage transistors available. The ONC18 1.8 V at first appears to be the best option for the design. However, after initial experimental design work, ONC18 1.8 V displays minor inconveniences that make the ONC18 3.3 V option more attractive[38].

One limitation of the ONC18 1.8 V CMOS process is that it does not contain any parts with a gate voltage of 1.8 V and a voltage drain-to-source (V_{DS}) greater than 1.8 V. The documentation for the ONC18 library specifies that a 1.8 V gate transistor with a V_{DS} of 5 V is available. This, however, turns out to be a typo in the documentation, as confirmed by OnSemi. Thus, to use the 1.8 V process for the design would require level-shifting circuitry to be introduced to the pixel to reach higher voltages and drive the larger transistors. Some disadvantages of using level-shifters include an increase in the total area needed for circuitry, the increase of power dissipation, and the possibility of error-prone operation. On the other hand, the 3.3 V CMOS process has a transistor with a gate voltage of 3.3 V and V_{DS} up to 15 V. The only disadvantage is that 3.3 V transistors are slightly bigger by default than their 1.8 V counterparts, but the small difference is manageable, and negligible if more circuitry were to be introduced. Therefore, I have chosen to proceed with the design using the 3.3 V process.

[1] Refers to the area of the smallest transistor allowed by the process

5.1.1 N-type laterally diffused high power transistor

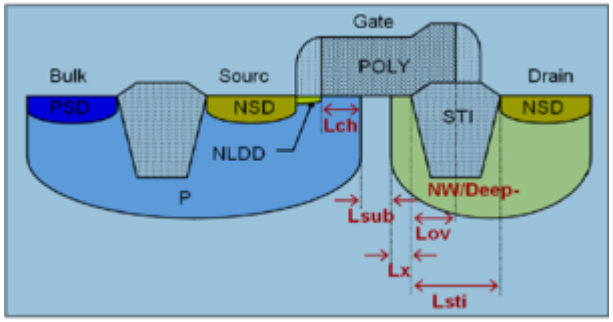


Figure 5.2: NLDMOS structure for the 3.3 V process

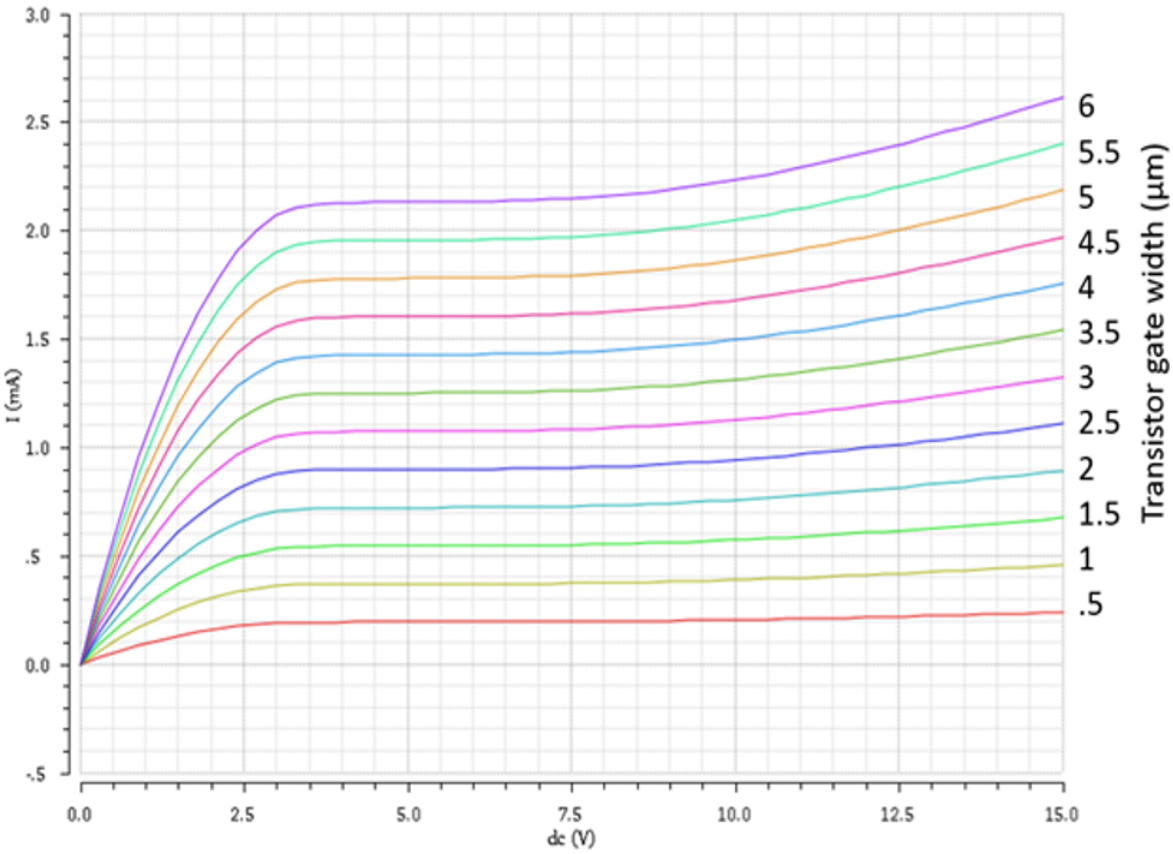


Figure 5.3: IV curves for NLDMOS transistors of various physical sizes

As previously mentioned, the 3.3 V process has a very attractive N-type laterally diffused MOS (NLDMOS). The NLDMOS found in the ONC18 technology library is shown in figure 5.2, and the NLDMOS has an asymmetric structure that helps lower the ON-resistance. The channel of an NLDMOS is characterized by its source diffusion, drain diffusion and gate length. This type of transistor is widely used for radio frequency (RF) applications, as they can provide a higher gain for amplifier applications, and overall can handle higher voltages and currents without extra circuitry[47, 48]. For the purposes of the first prototype 12 μm RIIC pixel, the NLDMOS offers great flexibility for the type of LED that might be used on a potential future hybrid. During the design phase, it has been difficult to predict how a 12 μm pitch IR LED will behave, or if it will work at all. Thus an adaptive RIIC that allows different current and voltage levels is required. As shown in figure 5.3, using the transistors available on the 3.3 V process makes it possible to achieve that flexibility. Using a parametric DC sweep simulation, it is possible to obtain transistor IV curves where the gate is at 3.3 V, the source tied to GND and the drain swept from 0 to 15 V, the full range of operation for these devices. The other variable is the actual size of the NLDMOS. The curves shown are for sizes starting at .5 μm, the smallest available size for NLDMOS, up to 6 μm. Anything larger would require too much of the RIIC pixel area space. The fact that the current holds very steady for a good portion of the curves, regardless of drain voltage, makes it ideal for designing a RIIC that can drive different SLED parts with different turn-on voltages.

5.1.2 VLSI techniques relevant to the project

Very large scale integration (VLSI) is the process used by industry to create very complex integrated circuits (IC). This design is at the semiconductor level in hardware. The basis for any IC is the transistor; the candidate technologies to make the first ART-IDEA prototype RIIC are based on CMOS transistors. CMOS transistors are comprised of two types of transistors, NMOS and PMOS. From these two device types, millions of combinations can be arranged to create simple circuits that can be combined

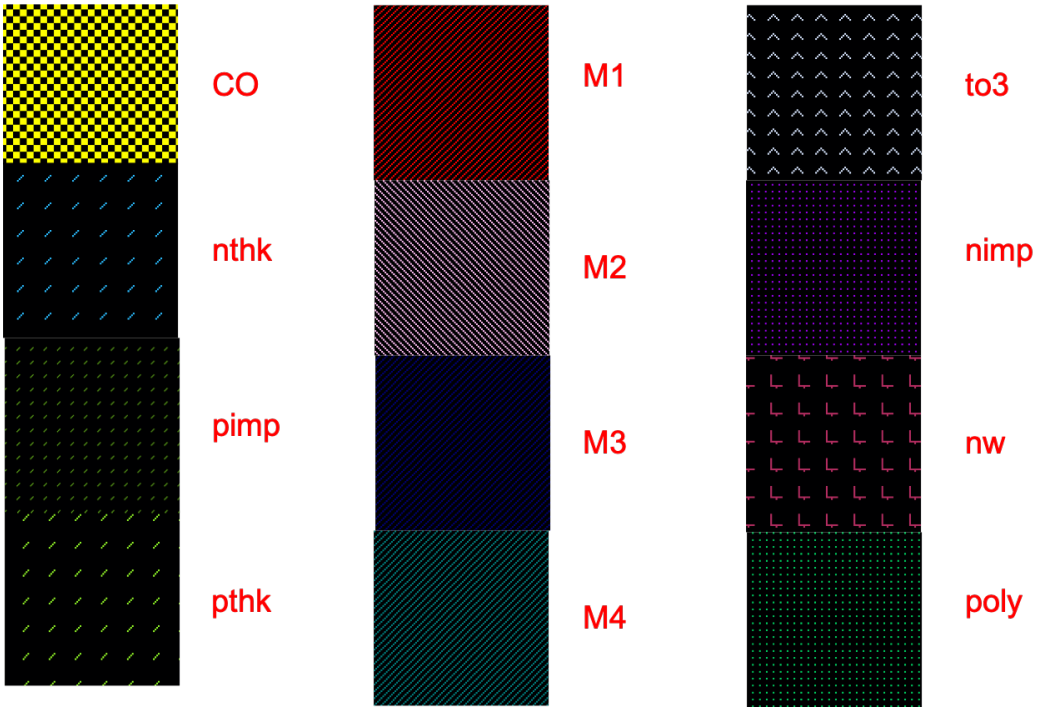


Figure 5.4: Most important mask layers in Cadence (version 6), a software used to create VLSI projects. CO: contact hole, nthk: drain extension for thick oxide n-channel devices, pimp: p-implant, pthk: drain extension for thick oxide p-channel devices, M1-M4: metal layers 1 through 4, to3: thick gate oxide for 3.3 V, nimp: n-implant, nw: n-well, poly: polysilicon

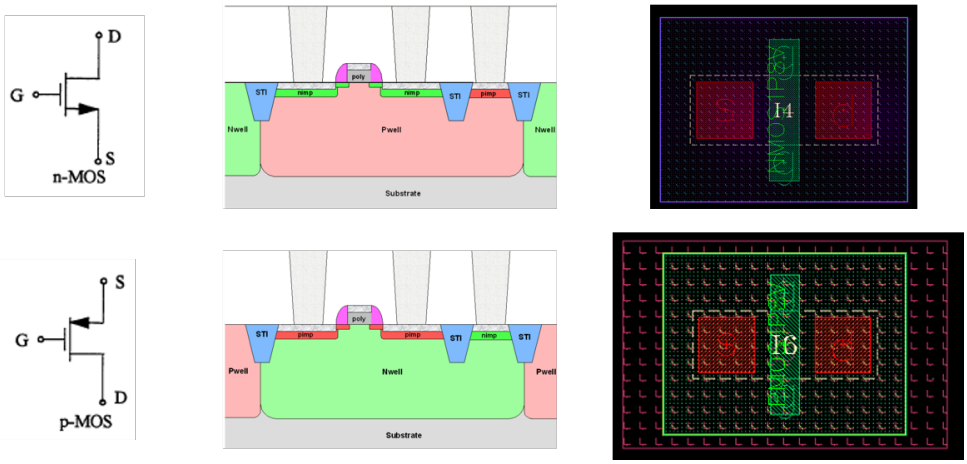


Figure 5.5: VLSI CMOS transistors, NMOS (top) are grown on a p-well, and PMOS (bottom) are grown on an n-well

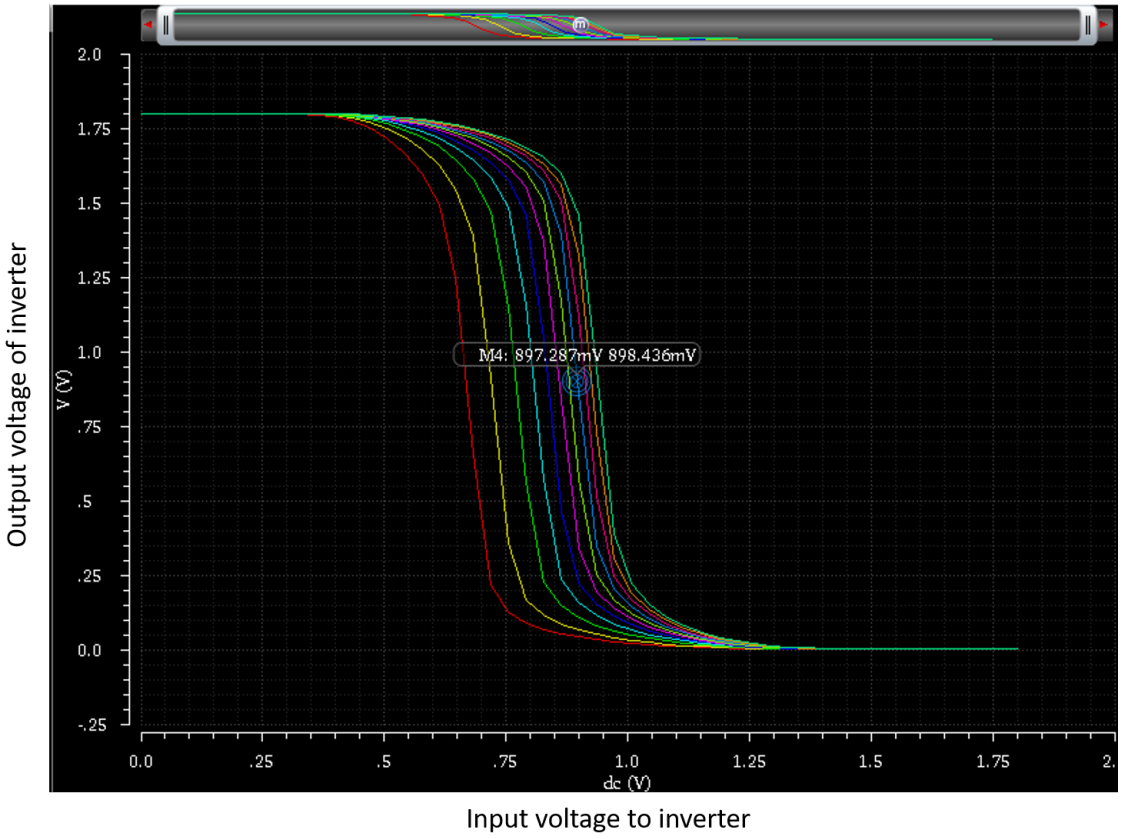


Figure 5.6: In some scenarios, it might be beneficial to have a faster rise time and a slow fall time, or vice versa. Ideally the charge-time of the PMOS pull-up network and the discharge-time of the NMOS pull-up network should be equal. The simulation shown is a DC sweep of the input of an inverter where the size of the NMOS transistor is kept constant at 420 nm while the PMOS size varies from 250 nm to 2000 nm in 11 steps. For the ONC18 process, the best match for no skew is when the PMOS is around 1400 nm, about 3X the size of the NMOS

to produce very complex ICs. CMOS transistors behave similarly to a capacitor at the gate where there is a dielectric between the polysilicon and the body of the transistor. For the transistor to turn on, the voltage at the gate has to be $V_{thres} \leq V_g$ for an NMOS or $V_{thres} \geq V_g$ for a PMOS. For an NMOS transistor, both the source and drain regions are negatively doped, creating diodes where the body acts as p, and source or drain are the n. Similarly, these diodes are also formed on the PMOS, but with reverse polarity, as the source and drain are positively doped.

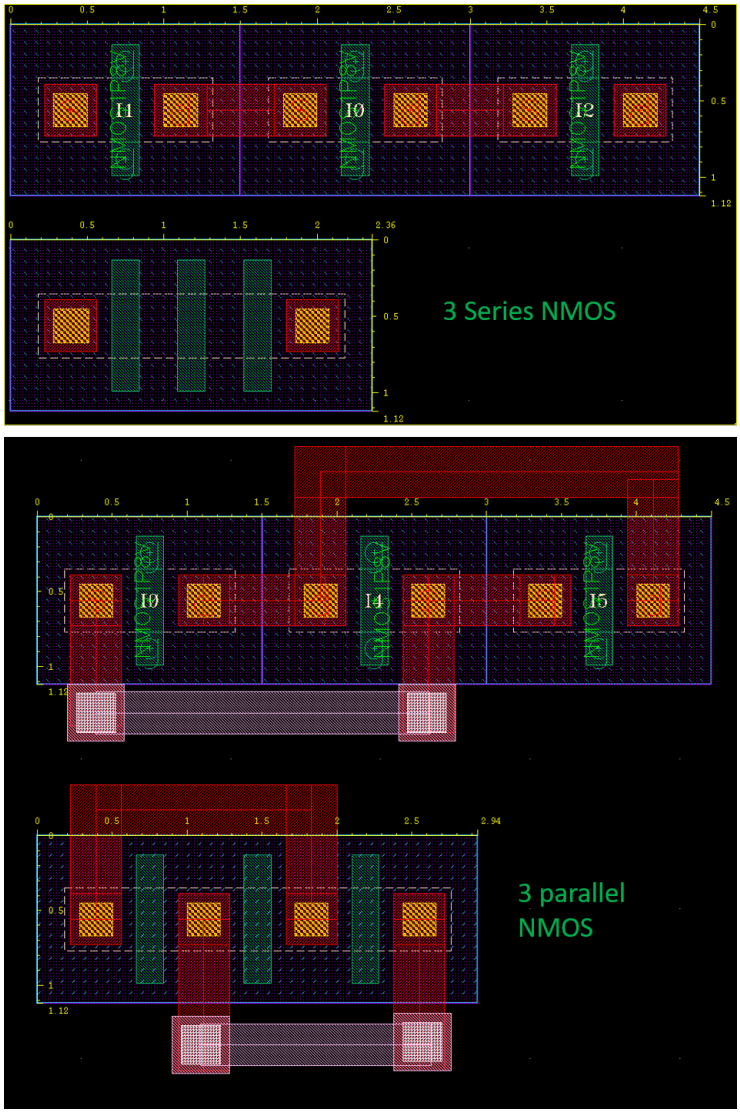


Figure 5.7: Top: Sample shows how to use the techniques discussed to maximize area of series CMOS. Bottom: Same techniques applied to a parallel network of 3 CMOS

In Cadence, the software used to design the IC, there are several mask layers used to draw transistors. These layers are listed in figure 5.4; additionally, when drawing a transistor, the *active-area* is chosen by drawing a dashed white-line boundary over the transistor. By examining figure 5.5, we can observe the schematic symbol, semiconductor-level diagram and Cadence representation for NMOS and PMOS transistors. In Cadence, an NMOS transistor is drawn by first laying out an *nthk* rectangle;

next an *nimp* rectangle is drawn right on top of it. Next, an *active-area* is drawn, this is the area where the drain and source contacts are drawn using a *CO* square and an *M1* square on top. The gate of the transistor is drawn using the *poly* layer, and it is represented by a green rectangle between the source and drain metal contacts. Finally, if the device is a 3.3 V transistor, a *to3* square is drawn over all the other layers (not shown on the figure to allow visibility of other layers). A PMOS device is drawn in the same manner, however, the *nthk* and *nimp* layers are replaced by the *pthk* and *pimp* layer, respectively. Additionally, an *nw* layer encompasses the entire structure.

In VLSI, a simple inverter is made from only two transistors, an NMOS and a PMOS, where the source of the NMOS is tied to ground (GND), the source of the PMOS is tied to voltage drain drain (VDD), the gates of both are tied together and serve as the input, and the drains are also tied together and become the output. The simple inverter is an important circuit, because it allows us to easily understand certain characteristics about static logic. There are four states possible in a static logic circuit. The first occurs when only the pull-up network is ON, resulting in a straight path to VDD. The second state holds when only the pull-down network is ON, resulting in a straight path to GND. These two states are the most common and give high noise immunity to the output(s) of the logic. The third state is called the Z state, this happens when the pull-up and pull-down networks are OFF simultaneously creating a very high impedance state. The fourth state is referred to as crowbar or X. The crowbar state happens when the pull-up and pull-down networks are ON simultaneously, creating a shorted path from VDD to GND, therefore, this state is undesirable.

A unit-inverter is an inverter with equal fall-time and rise-time; to achieve this the time constant (RC) must be the same when the pull-up network is ON, as when the pull-down network is ON. In any CMOS process, same-size PMOS and NMOS transistors have the same capacitance, but the equivalent resistance of the PMOS is

greater than the equivalent resistance of the NMOS[49, 50].[2] For back of the envelope calculations, it is assumed that an NMOS transistor has an equivalent resistance of R and a PMOS of 2R. R is inversely proportional to the size of the transistor, while capacitance (C) is directly proportional to the size of the transistor. We represent the size of the NMOS in an inverter as 1. Then, to equalize the equivalent resistance, the size of the PMOS has to 2[49]. This results in RC_{NMOS} = RC, and RC_{PMOS} = (R)(2C) = 2RC. The rise time and fall time are given by the resistance and capacitance along the path of current. When the pull-up network is ON, the current path includes the equivalent resistance of the PMOS, the capacitance of the PMOS, and the capacitance of the NMOS, giving a rise time of 3RC. When the pull-down network is ON, the current path includes the equivalent resistance of the NMOS and the capacitance of both transistors, giving the same 3RC for the fall time. The ratio of the equivalent resistance between the PMOS and NMOS varies according to the process. In the ONC18 process, this ratio is close to 3. Running a parametric simulation, where the size of the NMOS is kept constant while the size of the PMOS varies, is the best way to determine the size ratio as shown in figure 5.6

A very powerful technique that can be used in VLSI is combining several transistors by fusing common shared areas. Using this technique, we can save valuable semiconductor layer area by condensing all logic into compact blocks. It works as follows: Whenever two or more transistors of the same type are next to each other, their wells can be joined and shared. Whenever two or more transistors of the same type are connected in series, all of the inner contacts can be removed. Whenever two or more transistors of the same type are connected in parallel to each other, common metal

[2] The difference in equivalent resistance derives from the mobility (μ) of electrons and holes. The μ of electrons in a Metal Oxide Semiconductor Field Effect Transistor (MOSFET) is greater than the μ of holes. Mobility is the speed at which carriers can move through a material when an electric field is introduced. In a MOSFET process, mobility degradation and speed saturation affect the carrier μ. As a result, a smaller μ_{eff-n} and μ_{eff-p} are used to represent carrier μ for NMOS and PMOS devices respectively[49, 51, 52, 53]

contact points can be paired into a single metal contact. Figure 5.7 provides a basic example of how techniques can be used to greatly minimize the semiconductor area needed for a CMOS circuit. In the example, three minimum-size NMOS are connected in series and then in parallel. Ignoring the metal traces for the parallel connections, separately each of these configurations requires an area of 4.5 μm x 1.12 μm = 5.04 μm^2. When these two configurations are condensed, the semiconductor area for the compacted series circuit is 2.36μm x 1.12 μm =2.64 μm^2, and the parallel compacted circuit area becomes 2.94 μm x 1.12 μm =3.29 μm^2. This equates to 52% and 65% of the original area, respectively. Taking these methods and applying them to millions of transistors helps decrease the total area for the chip significantly[54, 49].

5.2 Building upon the NSLEDS design

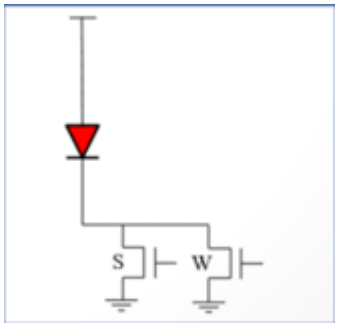


Figure 5.8: Simplified version of the NSLEDS pixel design

The pixel design used for the NSLEDS RIIC has been tested and proven to work reliably. For this reason, we chose this same design for the HDILED RIIC. Both of these RIICs have a pixel pitch of 24 μm, have been hybridized to SLED wafers, and have been integrated into operational IRSPs at lab facilities at the University of Delaware and the Eglin AFB in Florida. As a result, we chose to base the design of the ART-IDEA 12 μm pitch RIIC pixel on the NSLEDS pixel[40]. To better understand how the NSLEDS pixel works, let's start with a high-level perspective and then consider the details. The concept is very simple; at the high level, a pixel on a hybrid consists

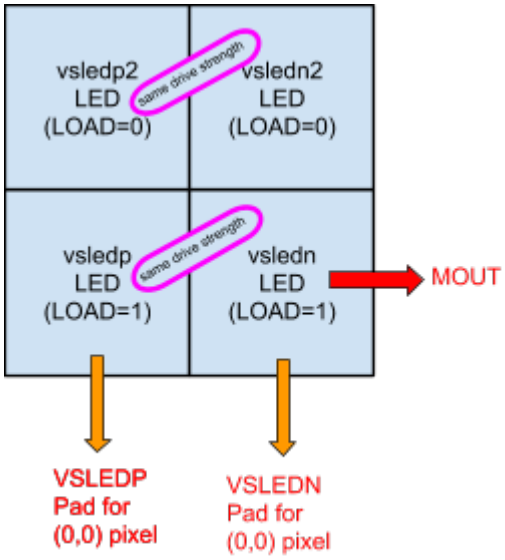


Figure 5.9: NSLEDS super-pixel top level design diagram

of an emitter, in this case an IR LED, and a pair of transistors that provide a way to control the current flowing through the LED. As mentioned before, we refer to these transistors as gears, because one transistor is much bigger than the other. As a result, the amount of current varies significantly as the smaller gear (smaller drive transistor) can only provide currents in the micro-amp range, whereas the larger gear (larger drive transistor) can provide currents in the milli-amp range[38, 44, 40, 6]. Figure 5.8 shows the simplest way to think about a single pixel in any of our current generation IRSPs. Starting with TCSA, all the IRSPs we have designed have this dual gear to provide more dynamic range to imagery being displayed on the array. The small gear is utilized to draw atmosphere imagery, whereas the strong gear is used to draw objects that appear really hot to the sensor, such as a fire or explosion.

NSLEDS and HDILED RIICs use a 2x2 super-pixel architecture that can be better understood by examining the diagram shown in figure 5.9. A 2x2 super-pixel works in a time-multiplexing manner; within the super-pixel there are two pairs of pixels, the first pair is activated when the *LOAD* signal is asserted HIGH. This first pixel pair is comprised of *vsledp* and *vsledn*. The second pair of pixels, *vsledp2* and

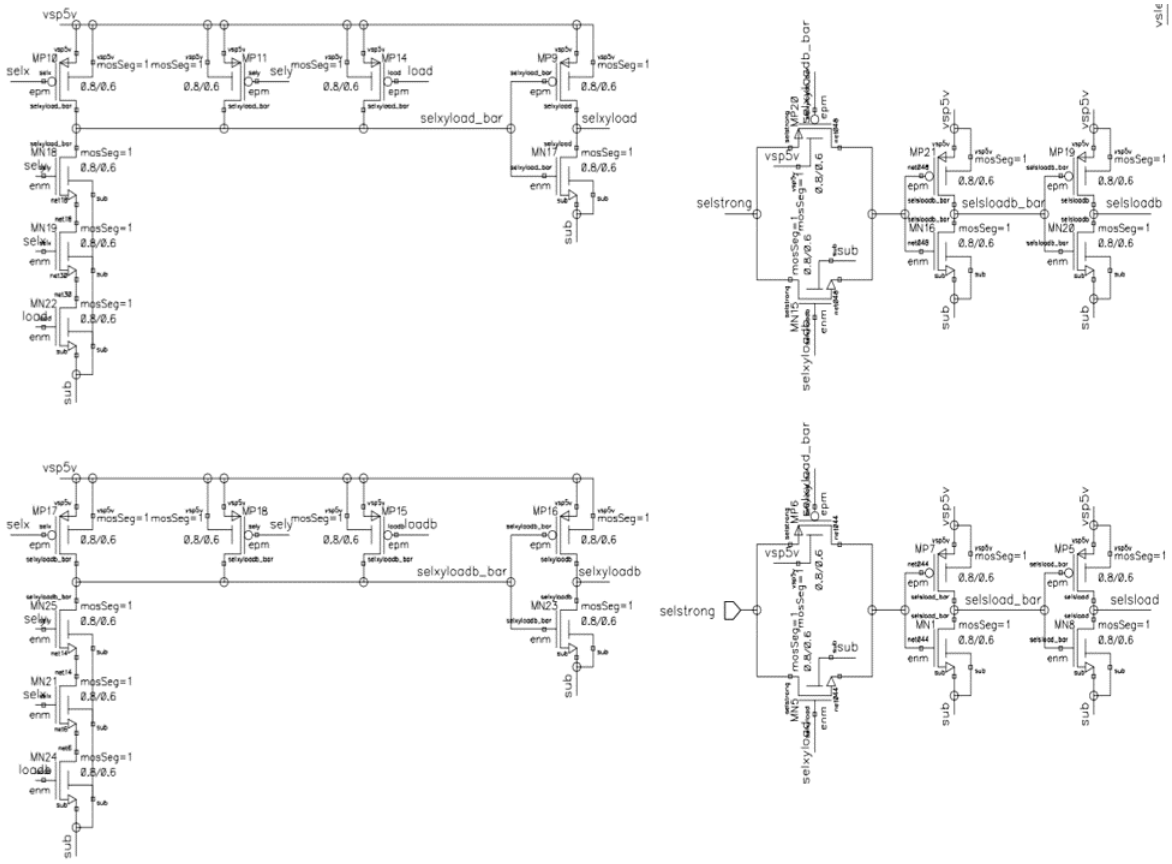


Figure 5.10: Address decoder (left) and gear selector (right) circuits for the NSLEDS super-pixel design

vsledn2, are active when the *LOAD* signal is LOW. All of these pixels are identical and can reach the same drive strength if desired. Inside the super-pixel, there is a small circuit that allows us to collect telemetry data. This is the monitor-out (*MOUT*) line that is used during wafer testing to check if the super-pixel is functional. However, due to spacing constraints within the super-pixel, only *vsledp* and *vsledn* can be monitored during wafer testing. If either of the LOAD pairs is active, two analog signals p and n charge the corresponding pixel to the value necessary to drive the LED. In this case, p and n are not to be confused with positive or negative, they are simply labels given to those input analog signals, hence *vsledp* and *vsledn*.

In the more detailed actual schematic of the NSLEDS super-pixel, there are a

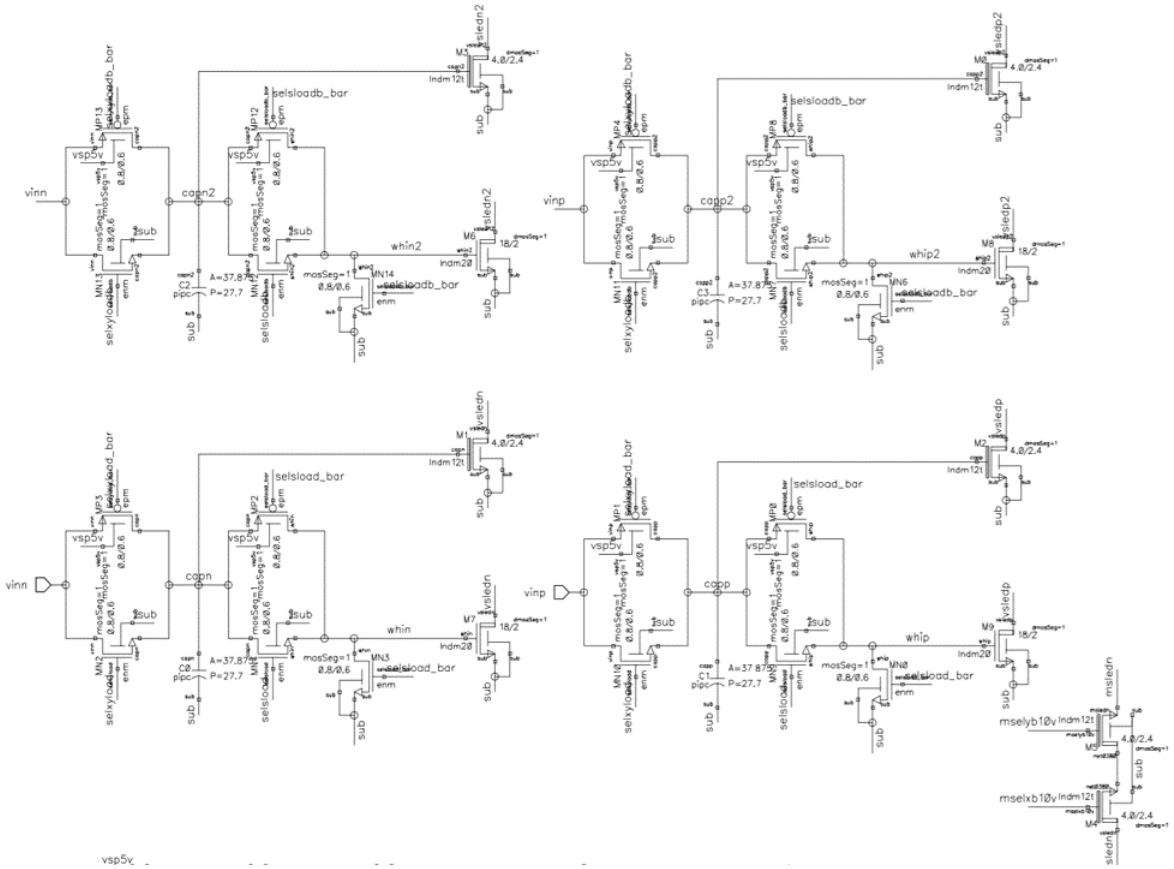


Figure 5.11: Drive circuits for all 4 pixels within a NSLEDS super-pixel and MOUT circuit (bottom right)

few circuits that comprise the logic that controls the gears. The first set of circuits is shown in figure 5.10. There are two different circuits and two copies of each. The address decoders are the left circuits shown, these take three inputs, *selx* and *sely* are the x and y addressing lines for the pixel, whereas the *load* inputs for these circuits are complements and derive from the same external signal. This way, only one of the pairs is active at a time, dependent on whether *load* is HIGH or LOW. The last stage of the circuit is an inverter, thus making the logic a NAND/AND gate with a pair of complementary outputs. The output signal after the inverter stage, *selxyload*, follows the AND logic, signifying that all three conditions are met. The output signal before the inverter stage, *selxyload_bar*, follows the NAND logic, always being a complement

of *selxyload*. With this naming convention, a '_bar' at the end of signal name indicates it is a complementary signal of the named signal. To the right of the address decoder circuit is the next link in the chain, the gear selector circuit. This circuit takes as input a digital signal, *selstrong*, which when asserted HIGH, tells the strong gear to activate in later stages; otherwise the weak gear is selected. The *selstrong* signal passes through a transmission gate that is controlled by the outputs of the address decoder. When the transmission gate is open and the *sels* signal passes through, it passes through two inverters in series. It may appear the inverters are redundant, but they serve two very important functions. First, since the *selstrong* signal is passing through a transmission gate, there is no filtration of the signal, which means that if the voltage level of the input signal is not adequate or if there is noise on the line, subsequent logic signals will be affected. By putting the signal through both inverters, the noise cancels out and the voltage levels are always either HIGH or LOW, never in-between. The second function of the two inverters is to provide the next stage of the pipeline with a pair of complementary signals, *selsload* and *selsload_bar*.

The last stage of the super-pixel schematic corresponds to the drive circuits and (MOUT) circuit, as shown in figure 5.11. Each of the drive circuits receives an analog signal, *vinn* or *vinp*, that controls the drive transistor gate. There are two transmission gates that control the behavior of this circuit. The left-most transmission gate only opens when the address decoder sets *selxyload* HIGH and *selxyload_bar* LOW. The second transmission gate only opens when the gear selector circuit asserts the pixel is to be driven using the strong gear. By default, the weak gear is always selected for drawing every time the pixel is addressed. In addition, between the two transmission gates, there is a small memory capacitor that stores the value of the drive strength even after the first transmission gate closes. Both the weak and strong gear transistors are very large in comparison to all other components of the pixel circuit. It is therefore necessary to have a way to reset the charge trapped in the strong gear's gate capacitor once there is no longer a need to draw very hot objects. There is a small NMOS transistor connected to the gate of the strong gear, this transistor acts as a switch to

ground that opens when the gear selector circuit disables the second transmission gate. Last but not least, the *MOUT* circuit consists of a pair of NMOS transistors that is connected to a single pixel drive circuit and allows the user to probe the drive circuit's output current.

5.3 First RIIC super-pixel iteration using the ONC18 3.3 V process

Because this represents the first time that a new technology library has been used to create a RIIC pixel, the first iteration has been done without modifying the standard components. Everything uses the automatically generated parts with default sizes. Obviously, if devices of the default size are used, the layout will not be compacted or use space efficiently. As a result, the initial 2x2 super-pixel layout has been designed without taking into consideration any space restraints in an area of 48 μm x 48 μm. Figure 5.12 shows the first completed layout of a 2x2 RIIC super-pixel. This first design using 3.3 V transistors has been realized using a total of four metal layers. Layers one through three are used to connect all the components. The thicker layer four is reserved for the metal contacts to be used in the hybridization process. The layout is based entirely on the schematics shown on in figures 5.10 and 5.11. The breakdown of the layout is a follows: All of the digital circuitry is located at the top of the layout, including the transmission gates of the four drive circuits. The bigger components, the memory capacitor and the NLDMOS transistors, are scattered below the digital circuitry. The metal-insulator-metal top capacitors (CMIM), represented by the blue squares, can't be smaller than 2.2 μm x 2.2 μm, which becomes a problem for a pixel whose size restrain is 12 μm^2. In addition, CMIMs reduce the area of the top metal layer, in this case metal four, which could result in shorts during hybridization and insufficient space for contacts. This reveals the need for a different method of adding capacitance to the circuit.

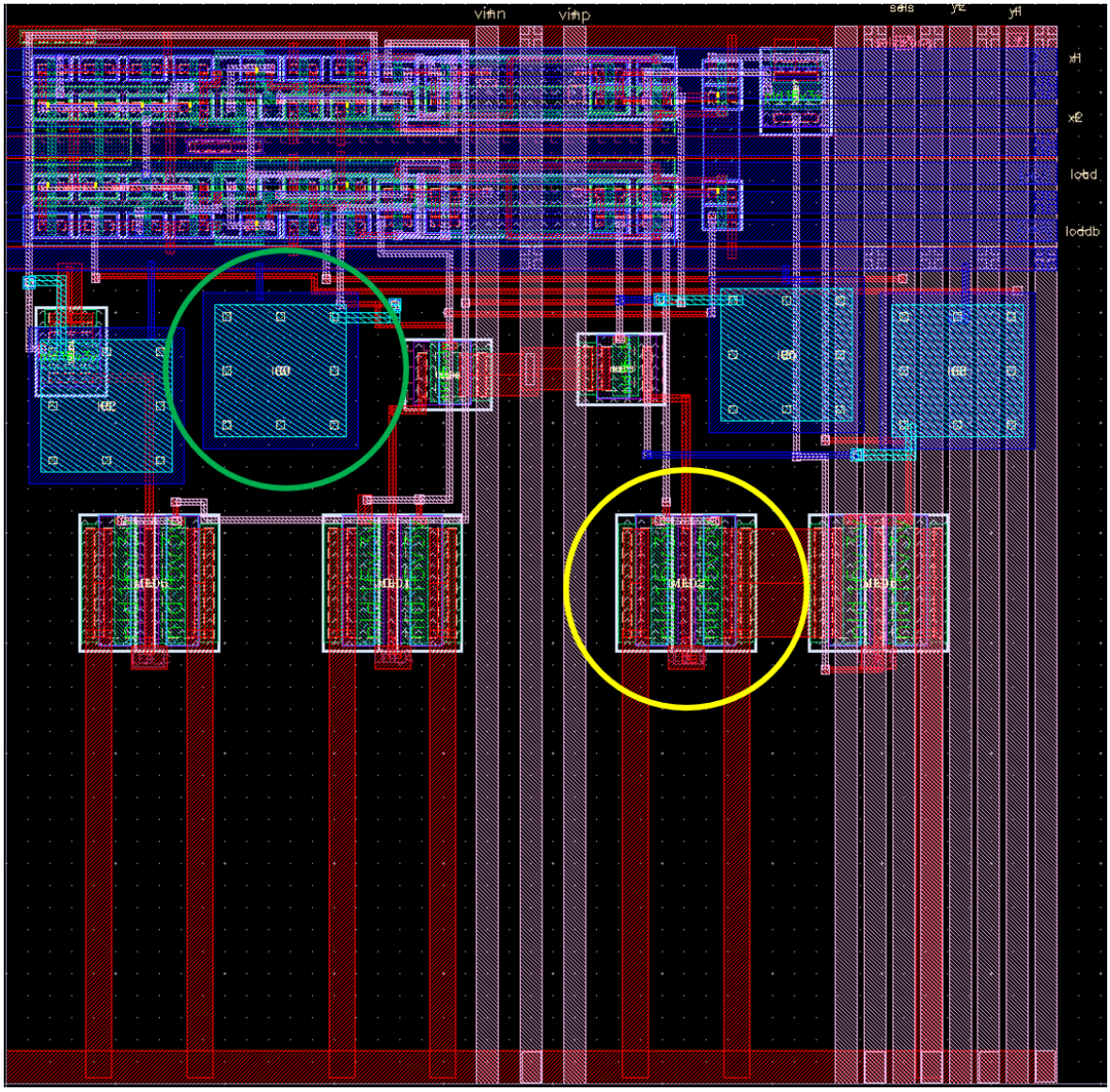


Figure 5.12: Final layout of a 2x2 super-pixel using the 3.3V technology library in an area of 48 μm x 48μm. The memory capacitor (green circle) and the NLDMOS (yellow circle) are the largest components in the layout.

5.4 Methods for design verification

After completion, the layout must be checked for correctness. Cadence Virtuoso software offers three essential tools to perform this examination. The first tool is the design rule check (DRC). There are thousands of rules that a VLSI designer must follow, all dependent on the process being used for the layout. DRC checks that all of

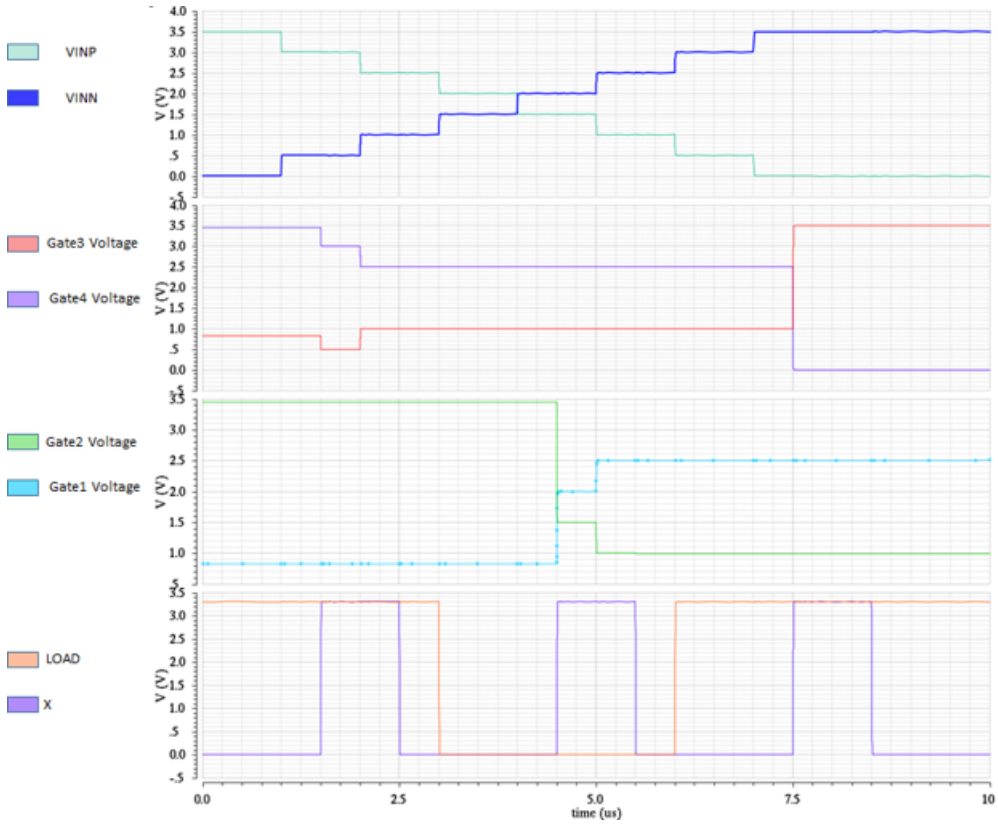


Figure 5.13: Post-PEX simulation of inputs and gate states for a 2x2 super-pixel using the ONC18 3.3 V flow process. Signals *vinp* and *vinp* dictate the behavior of the outputs when the pixels are active. The y address signal is set to HIGH for the entire simulation, thus not shown. If the x and *load* input signals are HIGH, pixel drivers 3 and 4 are active. If the x signal is HIGH and the *load* signal is LOW, pixel drivers 1 and 2 are active. When a pixel driver is active, the voltage at the gate of the drive transistor will be either *vinn* or *vinp*. Figures 5.14 and 5.15 use the input patters shown in this figure.

the rules that apply to the flow process are being used, for example, minimum distance between metal layers, floating gates, missing well diodes, un-doped polysilicon traces, etc. The next tool is the layout versus schematic (LVS) check. This tool compares all the instances in the schematic(s), such as transistors or capacitors, as well as nets, the metal or poly traces that connect components, and verifies that they exist and are connected correctly on the layout of the schematic(s). The third tool is the parasitic extraction (PEX) check. This tool is very powerful, as it lets the user analyze in detail

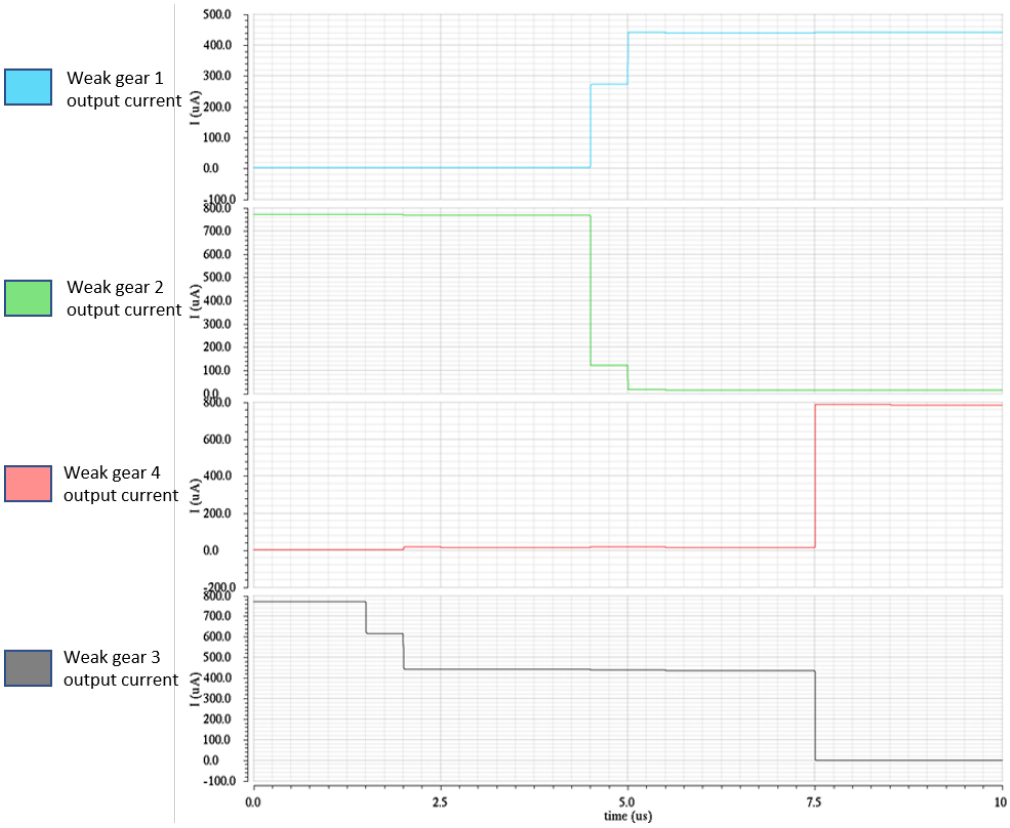


Figure 5.14: Post-PEX simulation of the weak gears, based on the inputs provided in fig 5.13 for a 2x2 super-pixel. When the appropriate driver is activated, its weak gear transistor outputs a current that follows its provided input. Weak gears 1 and 4 follow *vinn*, the other two weak gear transistors follow *vinp*.

all the undesired parasitic resistances, inductances and capacitances that become part of the circuit due to the placement and routing of the layout. Every single metal path on the layout has some resistance that changes based on the length and width of the metal trace. The same is true for capacitance, which can be found almost everywhere, from two metal traces running next to each other to capacitance formed in the substrate of the semiconductors. PEX generates a new schematic that contains the ideal components and all the parasitic components identified. The output schematic can then be simulated to ensure the parasitic components do not affect the integrity of the design.

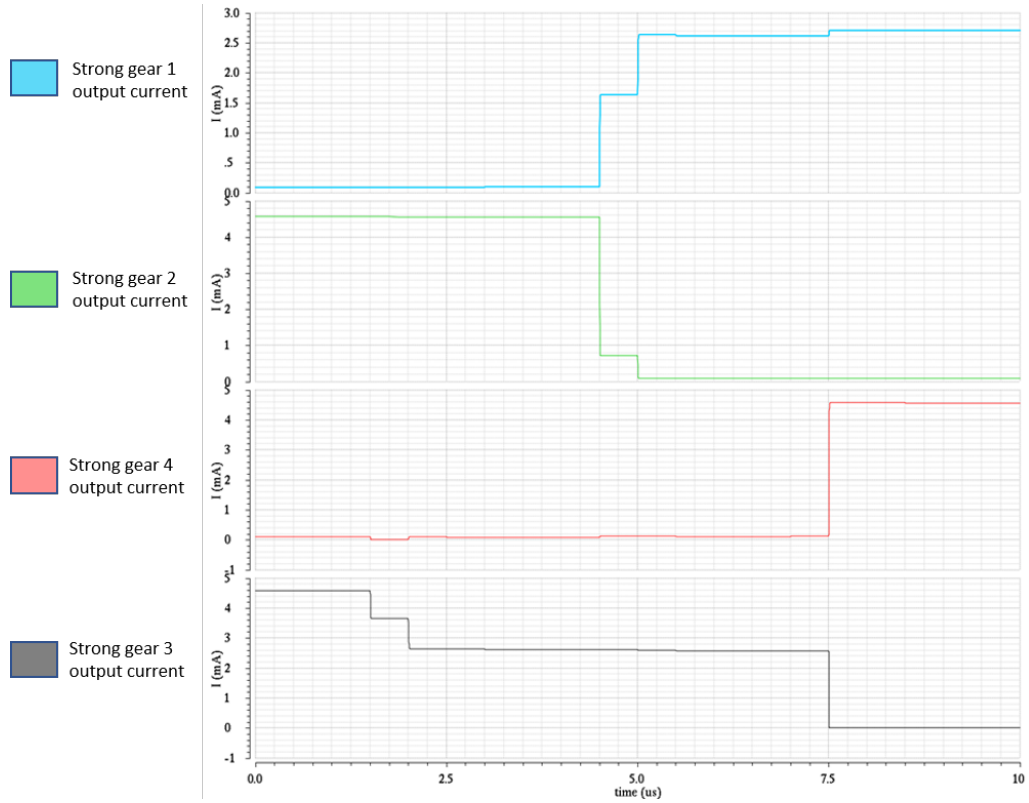


Figure 5.15: Post-PEX simulation of the strong gears, based on the inputs provided in fig 5.13 for a 2x2 super-pixel. When the appropriate driver is activated, its strong gear transistor outputs a current that follows its input provided. Weak gears 1 and 4 follow *vinn*, the other two strong gear transistors follow *vinp*.

The simulation results of the post-PEX extraction are shown in figures 5.13, 5.14 and 5.15. These simulations focus on showing the functionality of the design, as it is important to verify correct behavior post-PEX. Figure 5.13 shows how the input signals *vinn* and *vinp* have been set to rise and fall, respectively, over the same step intervals in a 10 μs period. If the pixel is active, these input signals control the gear gates directly, with *vinn* routed to pixels one and four and *vinp* to pixels two and three. For the simulation, the y address signal is always held HIGH, thus it is not shown on the figures. The *sels* signal, which selects the gear to use, has been set LOW to obtain the results shown in figure 5.14, and HIGH to obtain the results in figure 5.15; it is also not shown on the simulations. To isolate the times at which the pixel pairs are active,

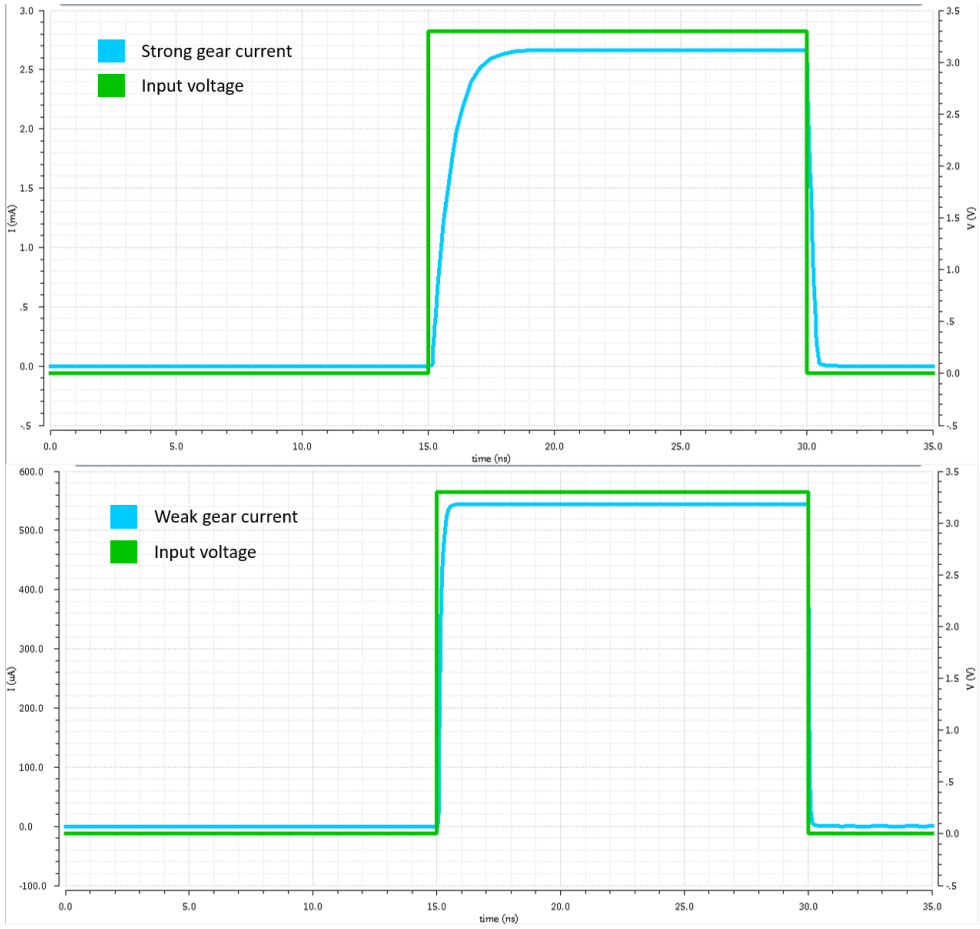


Figure 5.16: Pre-PEX simulation that shows the rise time of the strong (top) and weak (bottom) gears. This is an ideal circuit where only the characteristic of the components affect the behavior of the circuit.

x and *load* have been toggled at different rates. When x and *load* are HIGH, a pair of pixels is active, and when x is HIGH and *load* is LOW, the other pair is active. At any other time, the gates of the drive transistors hold the value stored in the circuit's memory capacitor. The simulations shown in figures 5.14 and 5.15 confirm that the post-PEX circuit works as expected.

A set of simulations shown in figures 5.16 and 5.17 provide a closer look at the effects of the parasitics. For this scenario, the same post-PEX circuit extracted from the layout in figure 5.12 has been used. However, this scenario focuses on showing the outputs of both gears for a single pixel over 35 ns. Moreover, the same input voltage

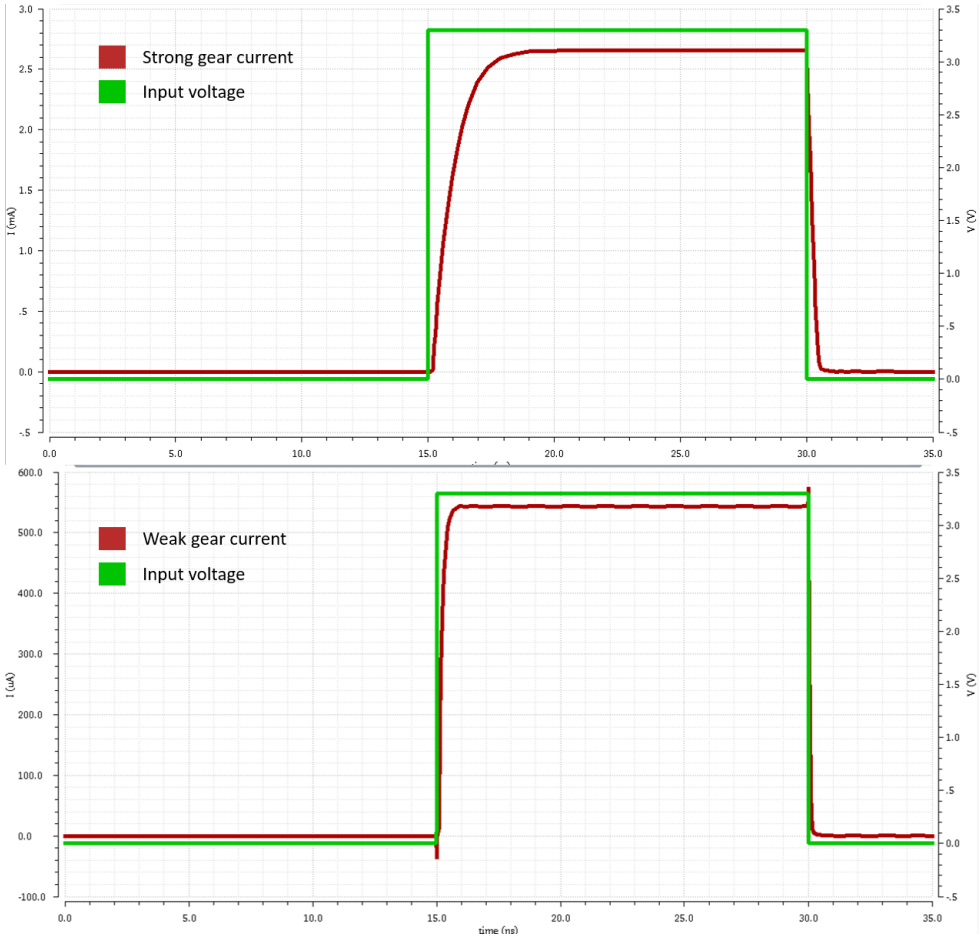


Figure 5.17: Post-PEX simulation that shows the rise time of the strong (top) and weak (bottom) gears. The output reflects the effect that parasitic components have on the ideal circuit. The parasitic components depend on the layout of the circuit. For this design, the parasitic components have no effect on the strong gear's output. The weak gear's output was affected slightly, as there is a bit of undershoot and overshoot on the edges. However, this is not significant enough to cause problems.

is used for the pre- and post-PEX simulations. The characteristics of the ideal circuit are shown in figure 5.16. Note that the ideal circuit only considers the characteristics of the ideal components to simulate the results. The simulated effects the parasitics have on the circuit are studied in figure 5.17. The parasitics show no effect on the performance of the strong gear, and very little effect on the performance of the weak gear.

5.5 Adaptations to the design of the ART-IDEA super-pixel

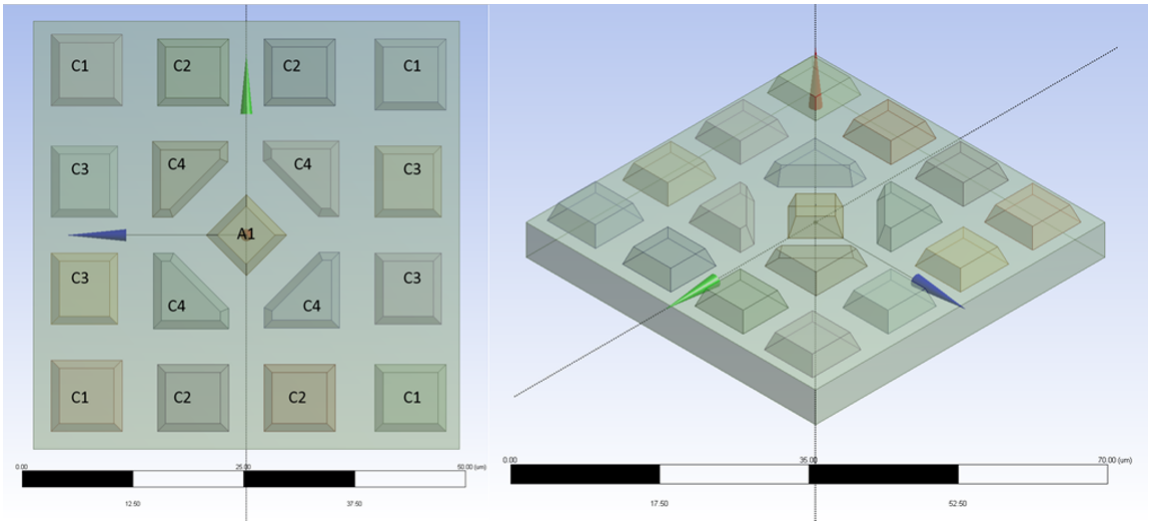


Figure 5.18: 4x4 super-pixel concept for the RIIC and SLED designs of ART-IDEA.

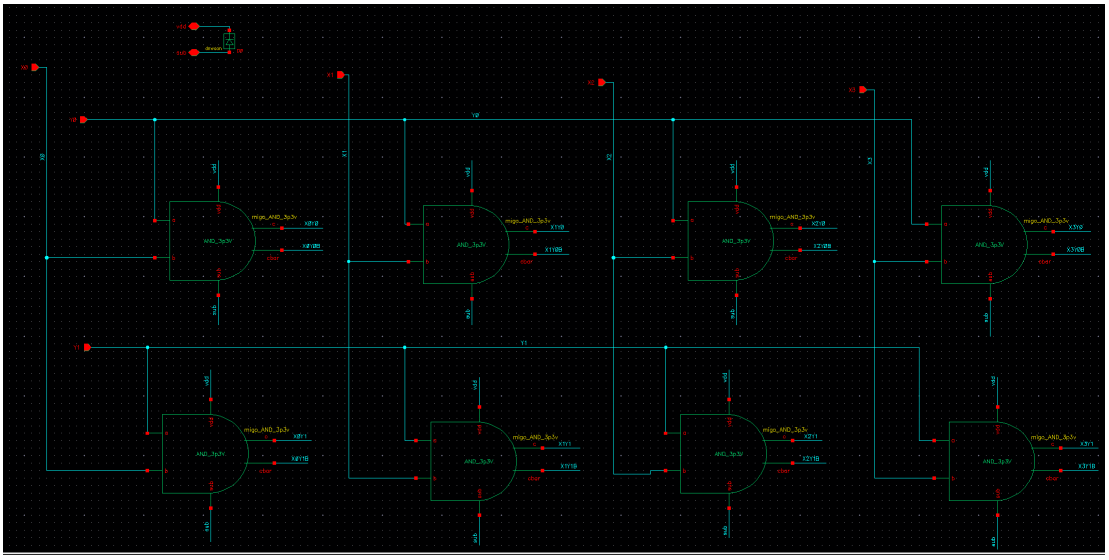


Figure 5.19: Address decoder for a 4x4 super-pixel.

The ART-IDEA project uses the concept of a super-pixel, but it is a modification of the super-pixel of NSLEDS and HDILED. As mentioned in earlier sections, a

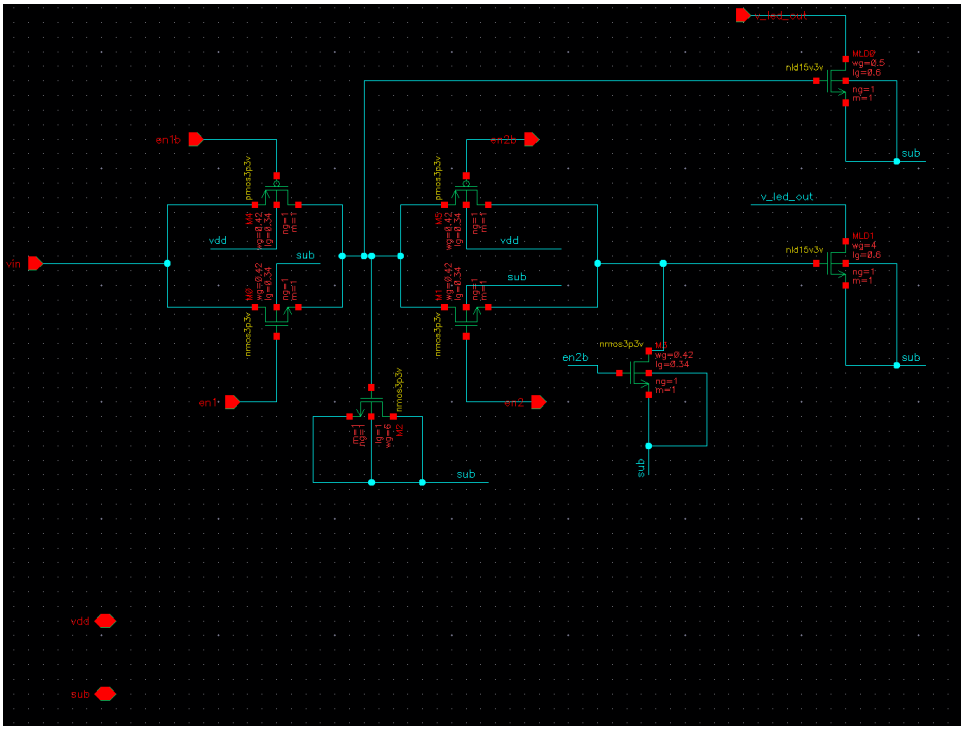


Figure 5.20: Address decoder for a 4x4 super-pixel.

super-pixel design refers to a group of individually addressable pixels that share common pixel-level circuitry on the RIIC and common contacts on the SLED super-pixel. This is a useful technique for maximizing utilization of the available space on both components of the hybrid array. For instance, every LED requires an anode and a cathode connection for proper operation. In the NSLEDS and HDILED designs, the SLED super-pixel groups together four LEDs to share a common anode contact. For the ART-IDEA super-pixel, the LEDs are grouped in a small 4x4 grid sharing a single common anode in an area of 48 μm^2. The principal reason for deciding that a 2x2 super-pixel would not suffice for a 12 μm pitch pixel design is insufficient space to lay out all the components. This became very apparent in the initial iteration of the layout of the 2x2 RIIC super-pixel. To fit everything in the RIIC, more of the logic can be combined if more pixels are grouped together within a common area. Our goal is to design a prototype where the circuitry for sixteen pixels can share a 48 μm x

48 μm tile. The concept also applies to the SLEDS, as shown in figure 5.18, where all the contacts denoted with 'C' are the cathode contacts for each of the individual pixels, and the center contact denoted, by 'A', is the common anode shared by all 16 pixels[38].

Other changes have been made to the RIIC architecture schematic. One is the complete elimination of the *load* signal from the design, and instead another address line has been added. In the ART-IDEA super-pixel, each individual pixel is addressed directly without the need for time multiplexing between pairs. The new design for the address decoders is much more straightforward, as shown in figure 5.19. The design consists of an array of AND gates with a complementary outputs, where the vertical nets constitute the address bits for the X direction and the horizontal nets, the Y direction. Because there are still two analog inputs, *vinn* and *vinp*, each AND gate enables a pair of pixels. Another change to the schematic has been made to the drive circuits for all sixteen pixels. The memory capacitor has been replaced by an NMOS device with its source, drain and bulk shorted to ground and the gate connected between the two transmission gates, as shown in figure 5.20. This modification is possible because of the property of CMOS devices that the gate forms a capacitor with the substrate. Additionally, the transistor is much smaller than the CMIMs and the top metal is not used, making it ideal for the pixel circuits.

5.6 Final 4x4 ART-IDEA super-pixel layout

The final design for the ART-IDEA RIIC pixel is based on the 4x4 super-pixel discussed in section 5.5. The top cell for the design is as shown in figure 5.21; there are a total of eleven inputs and seventeen outputs on the super-pixel. The inputs are as follows

- ***sels:*** a signal that selects the drive gear for all sixteen pixels,
- ***vinn, vinp:*** analog inputs that control the gates of the drive transistors. Each super-pixel writes two pixels at a time, thus the need for two analog inputs,
- ***x0,x1,x2,x3:*** digital input signals for addressing the pixel along the x-axis from left to right,

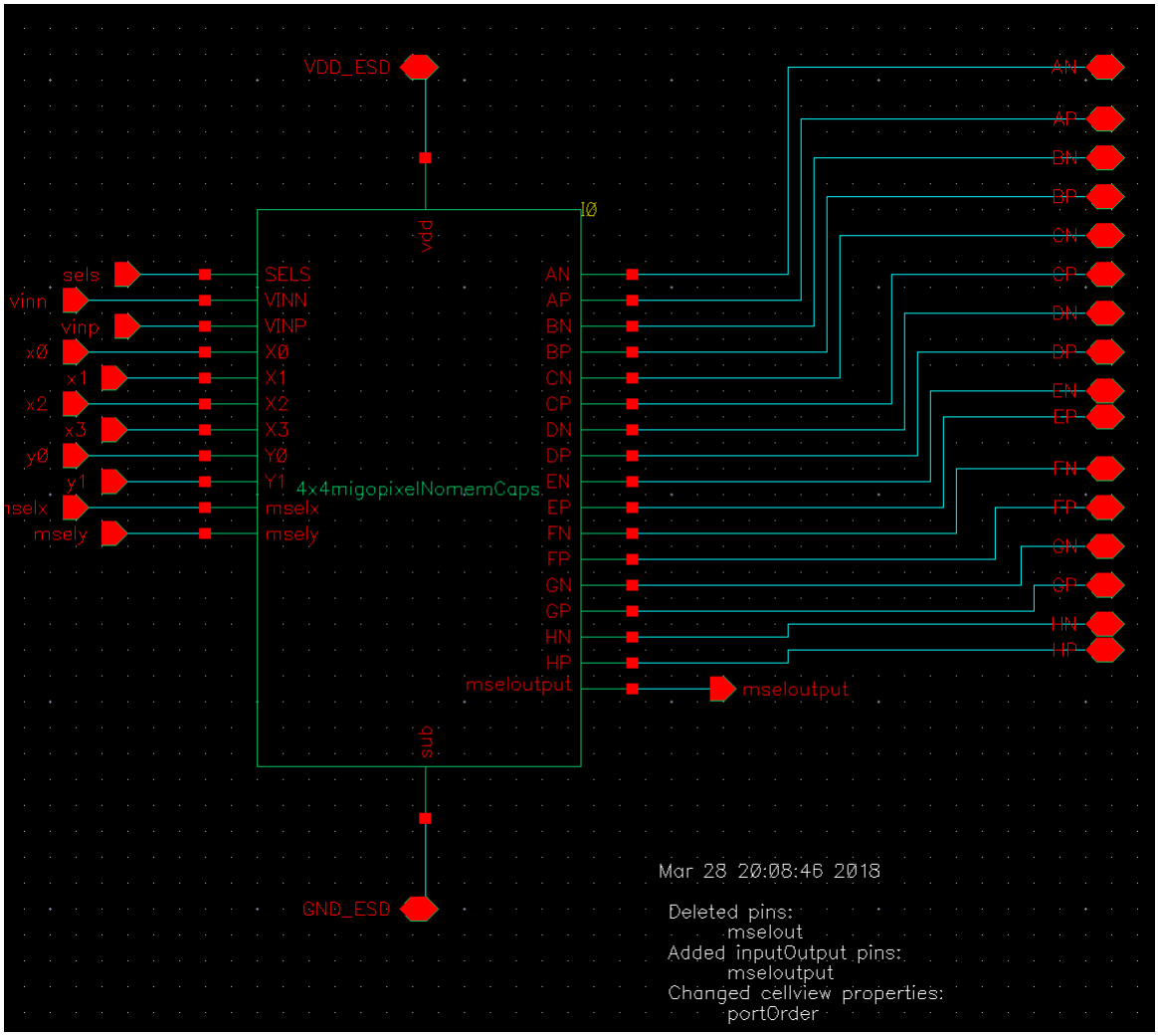


Figure 5.21: Top level cell for the 4x4 super-pixel of ART-IDEA.

- ***y0, y1:*** digital input signals for addressing the pixel along the y-axis from top to bottom,
- ***mselx, msely:*** control signals allowing access to telemetry in the pixel. In this version of the super-pixel, only one of the sixteen pixels can be monitored. This is intended for use during wafer testing in future tiled designs.

Sixteen of the outputs shown in figure 5.21 are LED current drivers. They are denoted with two letters, the first is the pair letter and position within the layout, the second identifies whether it is controlled by *vinn* (if second letter is *N*) or *vinp* (if

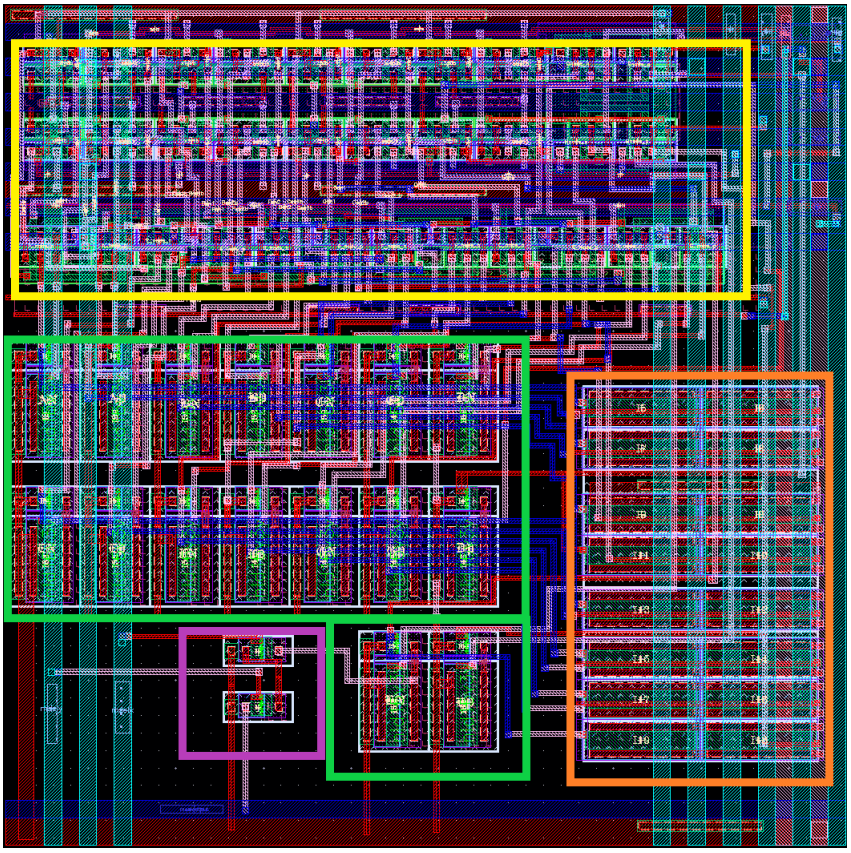


Figure 5.22: Final layout for the ART-IDEA 4x4 super-pixel design. Yellow: all circuitry, except big components, orange: memory capacitors, green: drive transistors, pink: MOUT circuit.

second letter is P). A and B are the first row, C and D the second row, E and F the third, and G and H the last row. The last output is the telemetry[3] output for pixel HN that can be used for ensuring proper functionality during wafer testing[45, 39, 44]. Only one pixel receives a telemetry circuit, if more pixels have a telemetry circuit, the number of metal traces needed would increase significantly, overwhelming the allotted space.

[3] The telemetry used in this design consists of two NMOS devices in series that connect the current driver of a pixel to a bus. The NMOS transistors open when the *mselx* and *msely* signals are HIGH. On a full-scale device, all the pixels that have the telemetry circuit are connected to the same bus. The bus is routed to a pad that is used during the wafer testing phase.

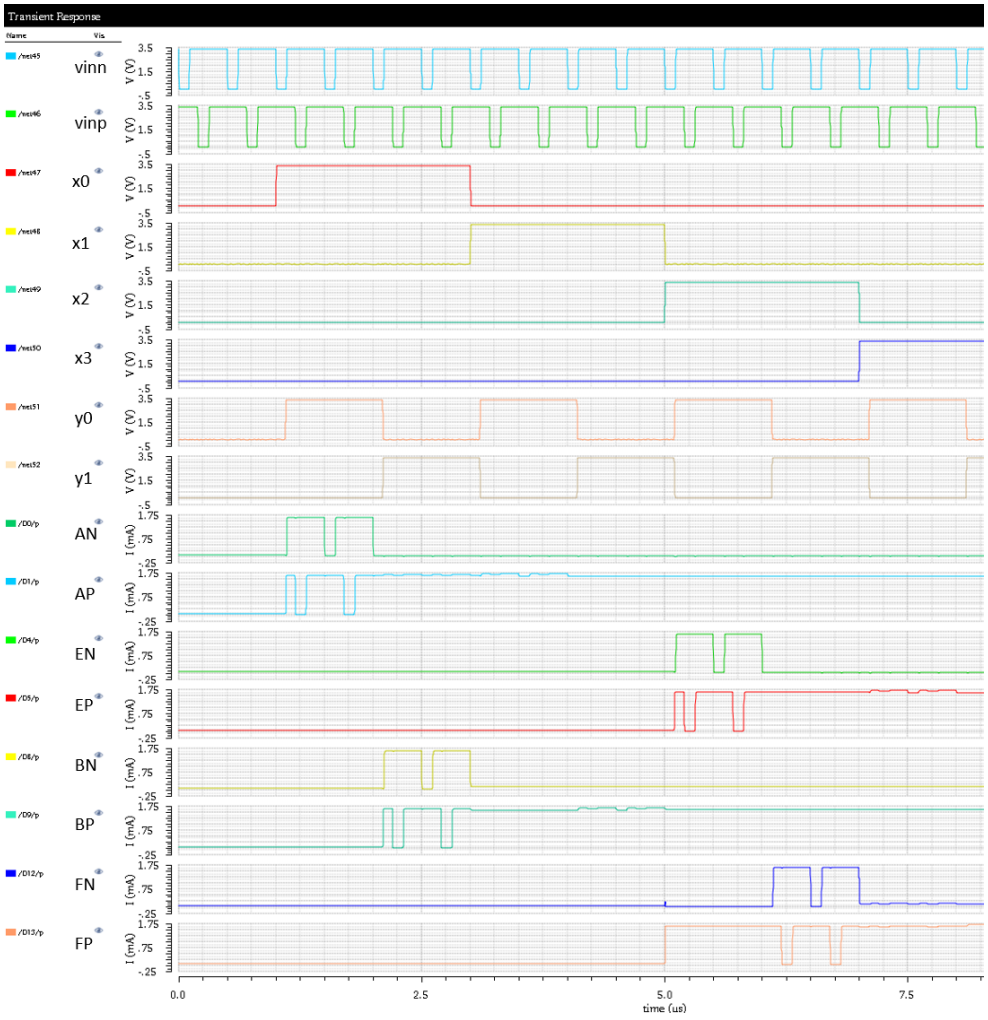


Figure 5.23: Post-PEX simulation for the 4x4 ART-IDEA super-pixel.

The final layout for the ART-IDEA 4x4 super-pixel is effected in a total area of 48 μm x 48 μm using a total of five metal layers, as shown in figure 5.22. In the layout, the top area in the yellow square is where most of the circuits lie, as it contains all logic CMOS circuits with all VLSI space-saving techniques applied. On the bottom portion, surrounded by the orange square, the memory capacitors are connected, and as mentioned before, these are NMOS devices configured as capacitors. The drive capacitors are grouped towards the middle and bottom, identified by the green squares. Finally, the pink square surrounds the MOUT telemetry for pixel HN.

The routing for internal connections has been done using mainly metal layers 1 through 3, additionally, signal buses that allow the super-pixel to be tiled in any direction have been inplemented. These buses run horizontally using metal layers 1 and 3 and vertically using layers 2 and 4. Some of these signal buses are visible in figure 5.22, especially those that use metal layer 4.

Once the final layout for the ART-IDEA super-pixel has passed the DRC and LVS checks and the PEX performed, the non-ideal schematic is generated with all the parasitic components. The newly created schematic has been simulated by introducing a series of input combinations that test that all possible states of the pixel logic work as designed. Simulation has been done for every possible RIIC scenario. An example of the simulation data can be observed in figure 5.23. Starting from the top are the two analog signals that control the pixel strength, *vinn* in cyan and *vinp* in green. For these signals, the input values are identical but shifted slightly so that the rising and falling edges differ from one another, and both swing from 0 V to 3.3 V. The next group of signals shows addresing lines, *x0* in red, *x1* in yellow, *x2* in cyan, *x3* in dark blue, *y0* in orange and *y1* in tan. From the addressing lines, we can see which pixel pair should be active among the 16 available pixels. The current output of the strong gear transistors compromises all other curves. These outputs mimic the analog inputs whenever they are activated by the address lines. The first pair represents the LED pair AN and AP in the green and blue colors, respectively. When *y0* and *x0* are both HIGH, AN and AP are active and follow the corresponding input pattern. When *y0* goes LOW, around 2.1 μs, the value last seen on the pixel gets stored in the memory capacitor. The next pair to be activated is BN and BP, in yellow and cyan, respectively, around the 2.1 μs mark. Pair EN and EP is activated around the 5.1 μs mark, and FN and FP activate when *x2* and *y1* are HIGH.

5.6.1 Experimental circuits

When designing the ART-IDEA pixel, we have also had the opportunity to experiment with small changes to improve or solve issues observed with the NSLEDS

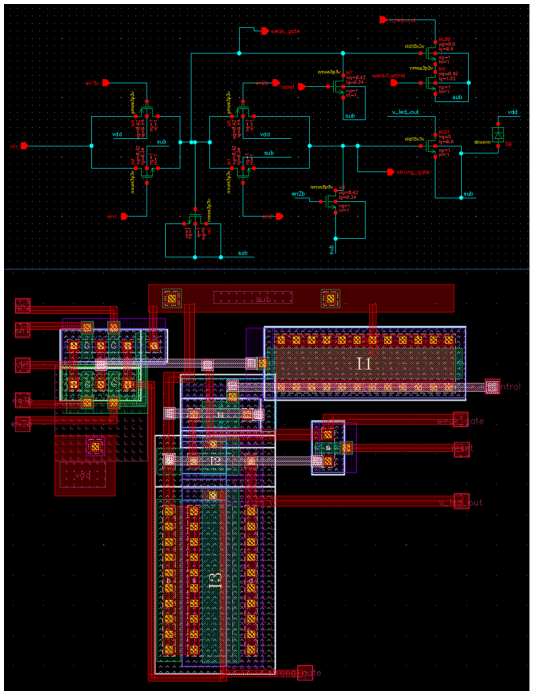


Figure 5.24: Final schematic and layout for the improved drive circuit. This design was based on the simulations performed in Appendix B

pixel. One such experimental circuit lowers the maximum current output of the weak gear to increase the bit accuracy of background objects. The minimum allowed size for the NLDMOS used as the weak gear on the ART-IDEA pixel has a turn-on voltage of around 800 mV, and the maximum current output is 240 μA when the drain is at 15 V and the source grounded, as shown in figure B.2. One option for decreasing the maximum current output of the weak gear is to use a resistor to limit current flow. This results in a finer control over the lower end of output currents for the weak gear. The problem is that resistors are relatively large, with fixed resistance; however, an NMOS transistor can be used as a current-limiting resistor by simply cascoding it to the weak gear. The circuit schematic shown in figure B.1 has been used to simulate the effects of using an NMOS or PMOS transistor as a resistor. The width and length of the NMOS and PMOS transistors, along with the gate voltage, have been simulated to observe their effects on the weak gear NLDMOS. For the PMOS transistor, the results are not

very good, as the turn-on voltage of the path increases, decreasing the available voltage range. In contrast, the path with the series NMOS works as expected, providing very interesting simulation results. All of the simulation results can be found in Appendix B.

Another minor change to improve the overall functionality of the pixel circuit is to add the ability to reset each pixel individually. The current generation of RIICs reset the array by applying a global reset. The global reset induces a reset period that turns all pixels OFF after every write frame. However, there are many scenarios drawn on the array in which parts of the image change at different rates. In many cases, the background remains static for a considerable time while a single dynamic object moves around. If we only reset those parts of the array that need to be updated, the entire system can display at much higher framerates[55, 56, 57]. This idea is being implemented at a software level, but adding a reset at the pixel level adds this feature at the hardware level. Another advantage of a pixel-level reset line is to keep leaky transistors in check. Transistors are not perfect, and there is always a small leakage current associated with each device. Most of the time, it is so small that pixel behavior is unaffected. However, instances have been observed where these leaks are sufficient to cause individual pixels to bloom, or emit light, when the array is in an idle state. The reset line on the memory capacitor solves this issue, as shown in the B.7 simulation. The improved circuit schematic and layout are shown in figure 5.24. It contains the reset line and the weak gear with an NMOS is series appropriately sized to a width of .42 μm and a length of 1.22 μm, based on the best values observed during the simulations.

5.7 Contact pads and ESD protection

Electrostatic discharge (ESD) is a natural phenomenon that can occur whenever friction is applied between two different bodies and static electric charges build up on their surfaces. As integrated circuits become smaller, they become more susceptible to the permanent damage from an ESD event. For instance, high-current ESD events

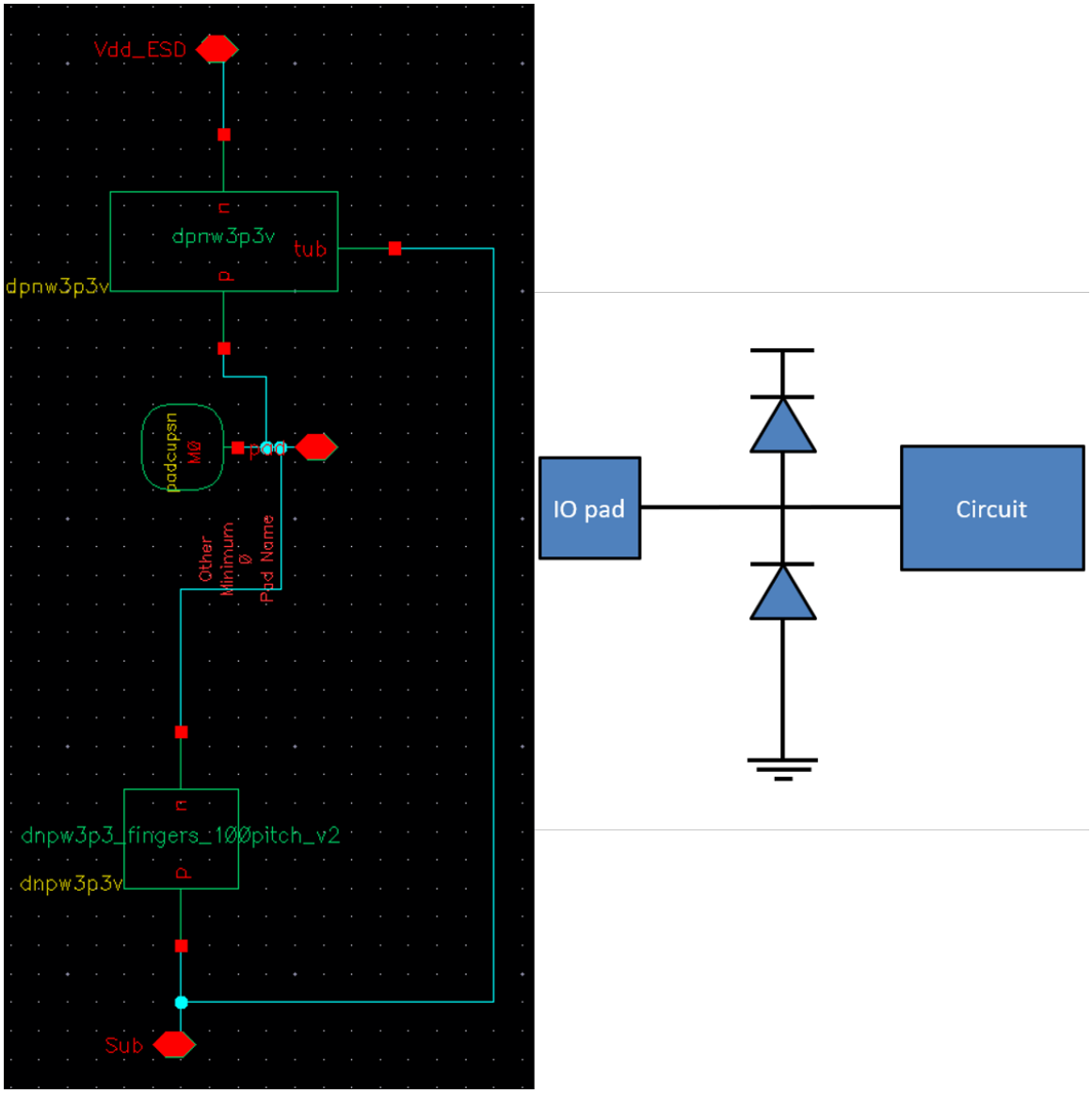


Figure 5.25: ESD protection diagram, (left) Cadence schematic for an input/output (IO) pad with ESD diodes, (right) top-level schematic of the design.

create voltages based on the impedance of the material they are flowing through, creating electric fields and damaging thin films on the IC. Material such as polysilicon can become less resistive during an ESD event, causing more current and voltage to pass through, creating failure. On bipolar transistors, the emitter-base junction may become leaky or shorted after an ESD event. On MOSFET transistors, the gate plate

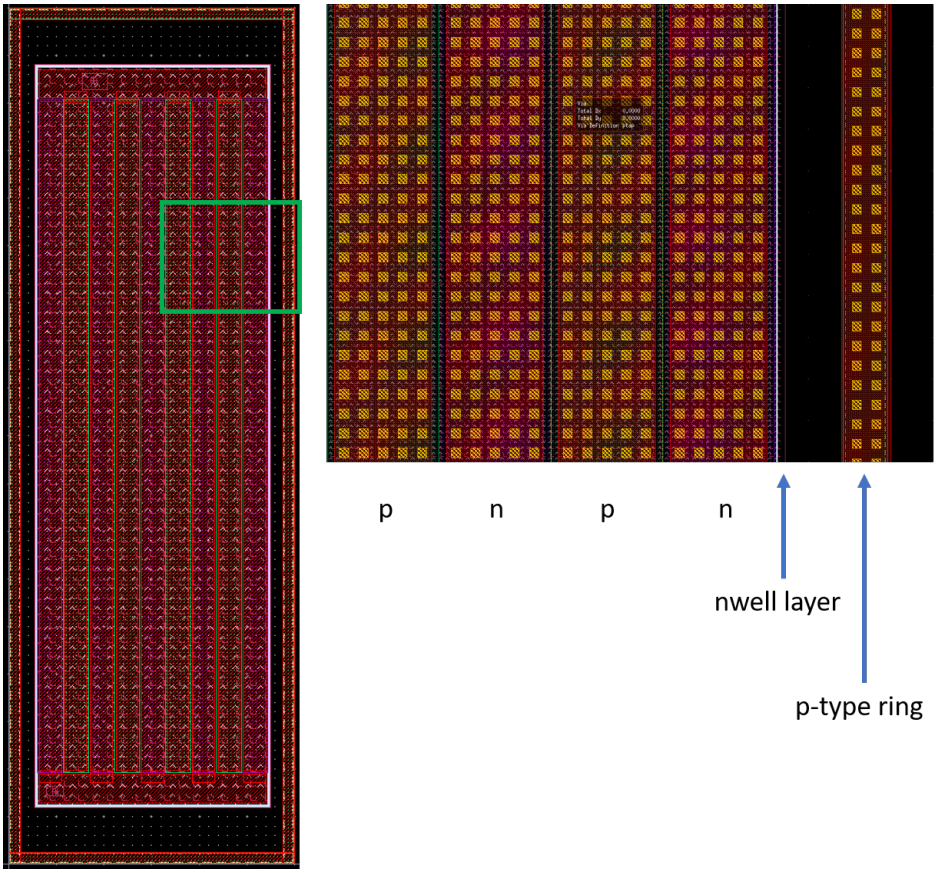


Figure 5.26: ESD diode to be connected to VDD_ESD, the diode is interlaced with p and n-type fingers and grown on an nwell. The entire diode is also surrounded by a p+ substrate wall.

can melt due to the thermal energy produced. Additionally, the diode junctions on the drain can also be damaged [58].

For this reason, all IC devices must have some sort of ESD protection to reduce the associated risk of destruction. A common ESD protection solution is to add two reverse-bias diodes at the input and/or output pins as shown in figure 5.25. During normal operating conditions, the diodes are off and there is no current flow across them. However, if the voltage at the pin exceeds its rated breakdown voltage, the diode effectively acts as a wire that shorts the path to a ground plane or a power plane, thus removing the stress from the internal circuitry.

The actual layout for the diodes shown in figure 5.25 has been custom made to

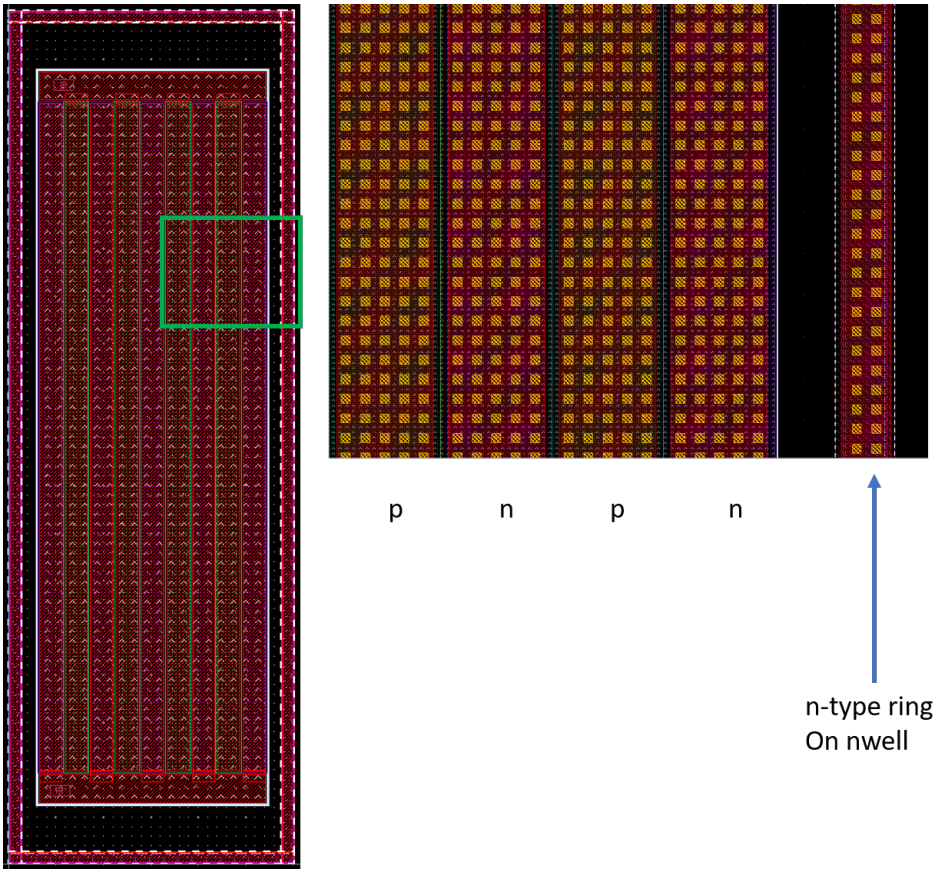


Figure 5.27: ESD diode to be connected to GND_ESD, the diode is interlace with p and n-type fingers and grown directly on a pwell. The entire diode is also surrounded by an n+ nwell wall.

meet the ESD guidelines recomended for an IC. The custom diodes are made using the MOS Sou/D junctions of the OnSemi 3.3 V technology library. These junctions effectively comprise a diode with a breakdown voltage between 8 to 10 volts. Additionally, two types of diodes are used, the first is an nwell diode with a p+ wall around the entire diode area. The second diode is a p-sub diode with n+ guard wall grown on an nwell. Furthermore, an ESD diode must have very low capacitance and low series resistance to minimize the impedance. For this reason, the ESD diodes have deliberately been made large, with a fingered pattern. The finger pattern helps in keeping the perimeter very large and thus the capacitance low.

5.8 Final Test Chip Layout to be Fabricated

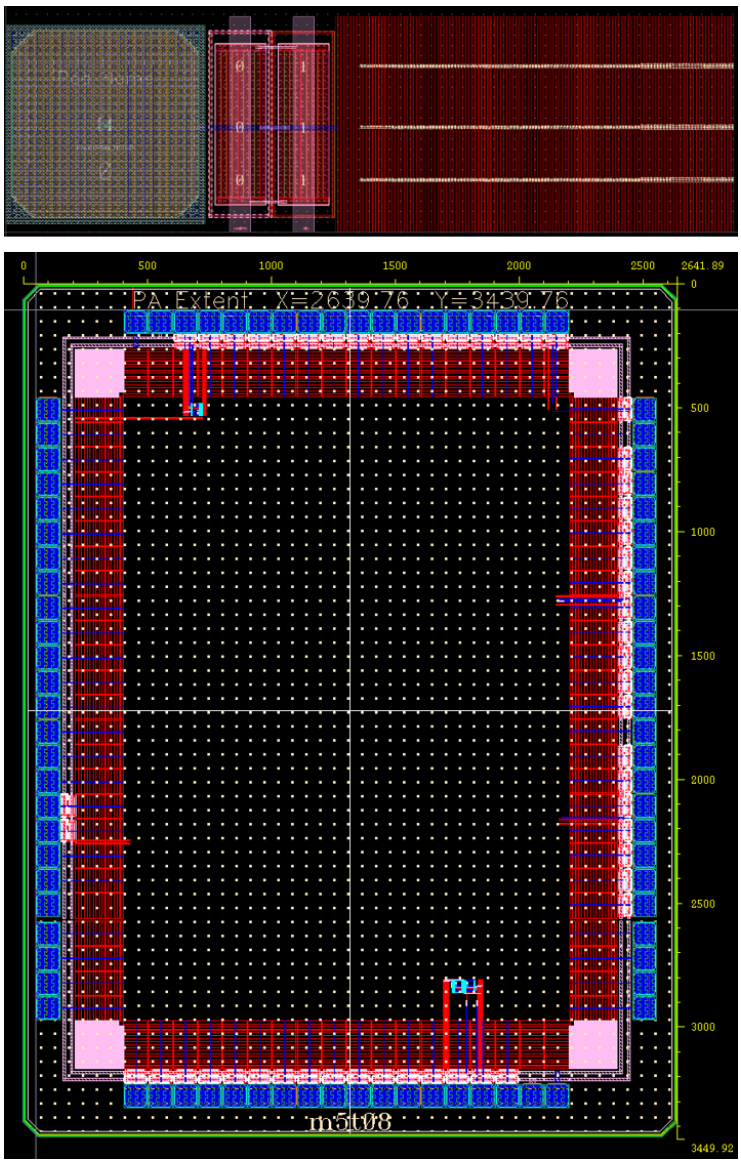


Figure 5.28: Top: zoomed-in layout of a single IO pad with ESD diodes and signal paths. Bottom: Final chip layout, a total of six circuits have been made available for wire bonding.

Using the ONC18 3.3 V process, various test circuits have been created to test every component of the 4x4 RIIC super-pixel. Every circuit in the final design has been simulated post-PEX to verify proper theoretical function before fabrication. The following circuits comprise part of the final test chip layout. The schematics and layouts

for these circuits can be found in Appendix C, and the final, top-level layout is shown in figure 5.29.

- **Stand alone gears:** Different-size NDL transistors are brought out to pins on the test chip. This allows characterization of the devices and their ability to drive LEDs.
- **Single pixel drive circuit:** The pixel drive circuit used in NSLEDS and HDILED RIICs has been reduced in size via the 0.18 CMOS process to operate smaller pixels. The stand-alone circuit serves as a test unit to verify functionality and as the control unit for comparison with the enhanced drive circuits.
- **Single pixel driver with reset line and limited weak gear:** In previous hybrids, we have observed that random pixels may emit light when the IRSP is in an idle state. We attribute this behavior to leaky gates in the digital logic. The proposed reset mechanism is directly embedded on the drive circuitry. Therefore, we can reset the array even before it is programmed. Furthermore, resetting will be fully firmware-controllable, meaning that we can choose whether to reset after a scene is drawn. This choice depends on the tests being done and/or the detector specifications. The minimum NLD transistor size is 0.5 μm, and it can output currents of up to 200 μA. However, this current may need to be reduced, depending on the brightness of the final fabricated LEDs. We have added a series transistor to the weak gear to act as a resistor. The idea is to operate the added transistor in the linear region to appear to the weak gear as resistance, thus effecting the desired current reduction.
- **Address decoder and gear selector:** A stand-alone version of the address decoder for the RIIC super-pixel is added to the test chip for verification of proper functionality. A stand-alone gear selection circuit is also added to the test chip for verification of functionality. This circuit dictates which gear to activate to drive the LED based on external control signals.
- **ART-IDEA super-pixel:** The 4x4 RIIC super-pixel on a 48 μm^2 area is the main focus of the test chip. This design features 16 sets of SLED pixel drivers, an address decoding circuit, and gear selection circuits for all drivers. All 16 sub-pixels in the super-pixel are independently addressable.
- **Tiled ART-IDEA super-pixel:** This circuit layout tests the ability of the RIIC super-pixel to be tiled to form a bigger RIIC. The cell has been designed to be tileable in any direction.

5.9 Packaging of the test chip

The final chip layout shown in figure 5.29 has been submitted to OnSemi foundaries for fabrication. The area purchased for fabrication of the ART-IDEA RIIC

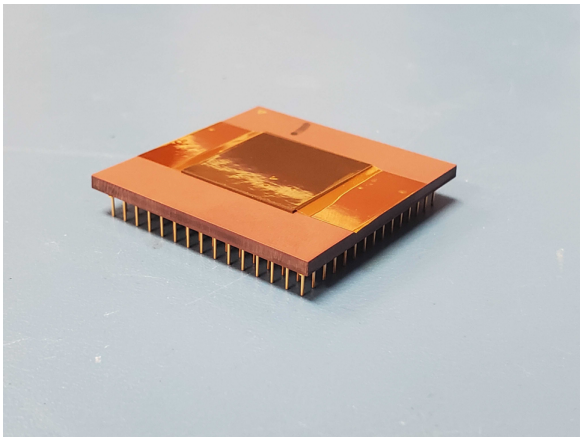


Figure 5.29: RIIC chip prototype packaged in a 144 PGA package

part has a total area of 5mm x 5mm on a shared wafer run. A total of 20 die have been fabricated within this area. After dicing, five of the chips have been sent to Majelac Technologies LLC to be wire bonded to a 144-pin grid array (PGA) package. The wire bonding layout used, along with the final pinout of the devices, is found in Appendix D.

Chapter 6

DESIGN OF THE LED DEVICES FOR ART-IDEA

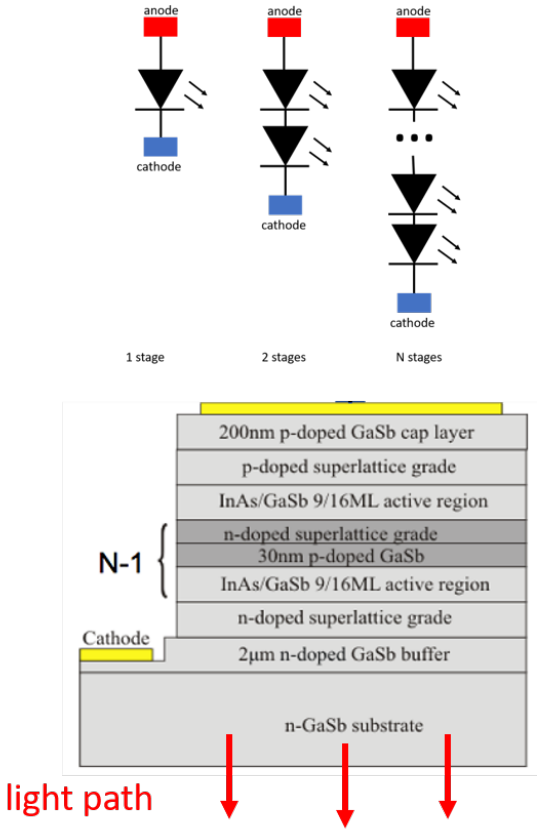


Figure 6.1: Architecture overview of SLED devices. A SLED may have one or more stages, a stage can be thought of as a single LED. More stages stack more LEDs in series. A SLED stage is composed of an active region and a tunnel junction. These may be repeated N times to make an N stage device. On a SLED device the light emits through the back of the device.

This chapter presents the methodologies that have been implemented during the design and fabrication of the first batch of SLEDs pixels for the ART-IDEA project.

Given the ground-breaking nature of this process, we have learned many valuable lessons from this first iteration. For the work to be discussed in this section I was involved from a high level, meaning I coordinated and led the decision making for the design of the SLEDs. However, the growing and characterization have been done by Firefly Photonics, our partner in this effort.

The SLED devices used for making our projectors emit in the MWIR region, between 3 μm to 5 μm. The exact wavelength may vary slightly depending on the generation of projector or goals of the programs funding the projects. The SLED devices are grown on GaSb using molecular beam epitaxy (MBE), and the super-lattice (SL) active regions are InAs/GaSb layers. The stack composition for the SLED devices is shown in figure 6.1. A SLED device by default has at least one active SL region that emits light; we call this a stage[59, 60]. More stages can be sandwiched in the middle of the stack, each separated by a tunnel junction of types n- and p-doped GaSb. If a SLED device is referred to as having N stages, N-1 stages have been added in the middle of the sandwich[3, 61, 62, 59]. Figure 6.1 illustrates using LEDs to represent a stage; since each active InAs/GaSb SL region emits light under the proper bias conditions, each stage can be represented as an LED on a series chain of N LEDs. The purpose of stacking LEDs in this manner is to increase the total light output of a SLED device[61, 3, 8, 63, 64].

6.1 Motivation for decreasing the LED size

The state of the art SLED technology being used in our IRSP systems has a light extraction efficiency of about 1%[3, 63]. The low-efficiency number of LEDs has been the main motivating factor in our quest to reduce the SLED pixel size. We have observed in previous SLEDs that light extraction became more efficient with smaller LED pixel size. Denis Norton, a former PhD student at the University of Iowa, has described these observations in his dissertation[3]. In figure 6.2, the data collected shows that, as the area of the SLED device decreases, the radiance increases. The cause is believed to be that the angle of the sidewall becomes more efficient as the

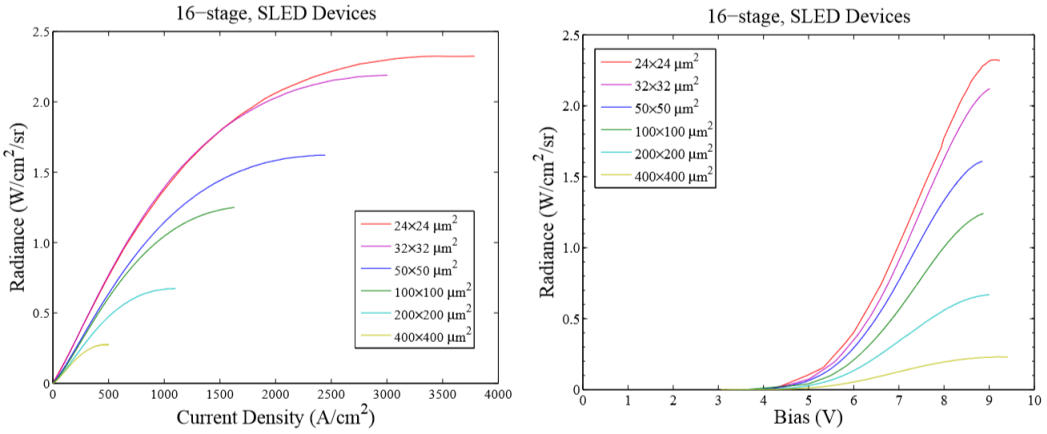


Figure 6.2: Current density (left) and bias voltage versus radiance for variously sized 16-stage SLED devices[3].

ratio of mesa height to SLED width increases [3, 38, 61]. This theory is supported by the simulation data in figure 6.3, where a SLED device without sidewall is compared to a SLED device with a 45° sidewall. The ray-tracing simulations predict an increase in light extraction from the device with angled walls[8, 3, 38].

6.2 Fabrication of the SLED devices

During the very early design phase for the SLED devices to be used in conjunction with the ART-IDEA RIIC, we have had to determine their design specifications. Most other projectors' SLED arrays use a 16-stage stack. However, as the number of stages increases, the turn-on voltage of the SLED arrays increases by a similar factor ($\sim$ 300 mV per stage)[3, 8, 62, 4]. Figure 6.4 presents an example showing how the number of stages affects the properties of the SLED device. In this case, four devices with the same area of 120 μm x 120 μm, but with different numbers of stages, are compared. The SLED with 16 stages outputs the most light, but also had the highest turn-on voltage, around 5 V. For this project, we wanted to develop a SLED that can be operated at a lower voltage, consequently decreasing the total power consumption of the system. At the same time, we desired a pixel with a pitch less than 24 μm for future IRSP development. Looking at this from a different perspective, a device

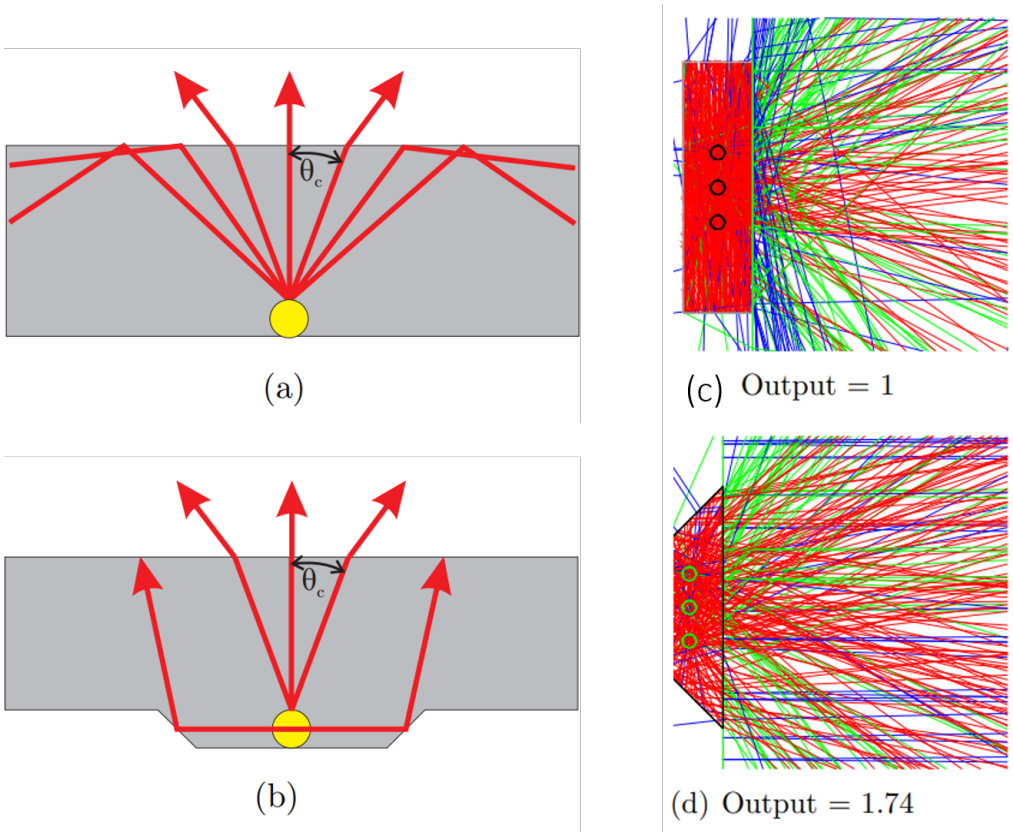


Figure 6.3: Diagrams and ray-tracing simulations that show the advantages of angled sidewalls for light extraction. θ_c is the maximum angle at which light can escape the back of the substrate. (a) Shows a device without sidewalls, a ray-tracing simulation is shown in (c) where the total output is normalized. The geometry in (b) has sidewalls with an angle of 45°, photons hitting the sidewalls may bounce off at an angle that allows them to leave the substrate. A ray-tracing simulation that uses the geometry of (b) is shown in (d). The theoretical output increases by .74 of the normalized value of (b)[8].

with a higher number of stages also becomes taller[4]; a taller device with a small area translates to smaller mesas and less space for the metal contacts, as the sidewalls have an angle. For these reasons, we have chosen to use 8-stage devices for the first prototype, as they are a good compromise between the light output we want to achieve, reasonable turn-on voltage and device height.

Two types of 8-stage devices have been grown on 3" wafers, differing mainly

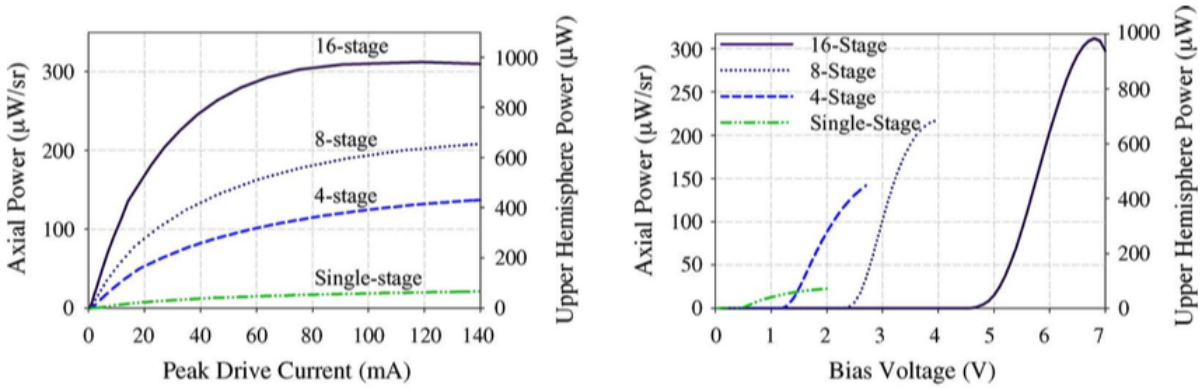


Figure 6.4: Two plots that show the effect of having different number of stages on SLED devices. With a higher numbers of stages, the maximum light output from a SLED increases, however, this increases the turn-on voltage of the SLED device

in stage thickness and, by secondary effect, etch depth. The first wafer is IAG739, which has a stage thickness of 133 nm and an etch depth of 2 μm; the second wafer, IAG740, has a stage thickness of 266 nm and an etch depth of 3 μm. As a reference, the usual 16-stage device has a stage thickness of 133 nm and an etch depth of 4 μm. The photolithography mask designed for dividing the SLED devices is shown in figure 6.5. The mask has been designed to grow small-format pixels of various sizes. There are four quadrants that are symmetrically identical, but partitioned/subdivided differently. The first quadrant features LEDs with pixel pitches from 24 μm through 406 μm without any partitions. The second is also divided into areas of the same dimensions as quadrant 1, however, the areas have been further partitioned to create 12 μm pitch pixels. A 24 μm x 24 μm area on quadrant 2 is further partitioned to create a mini-array of four 12 μm pitch pixels with a lane width of 3 μm and effective pixel mesa width of 7 μm^2. The third and fourth quadrants are similar to quadrant 1 with the exception that the partitions have 18 μm pitch and 24 μm pitch pixels, respectively. The finalized list of SLED pixels fabricated during this work is detailed in Appendix E. Having mini-arrays as well as single pixels allows us to compare the light extraction of different mini arrays and full-size pixels, verifying whether wall

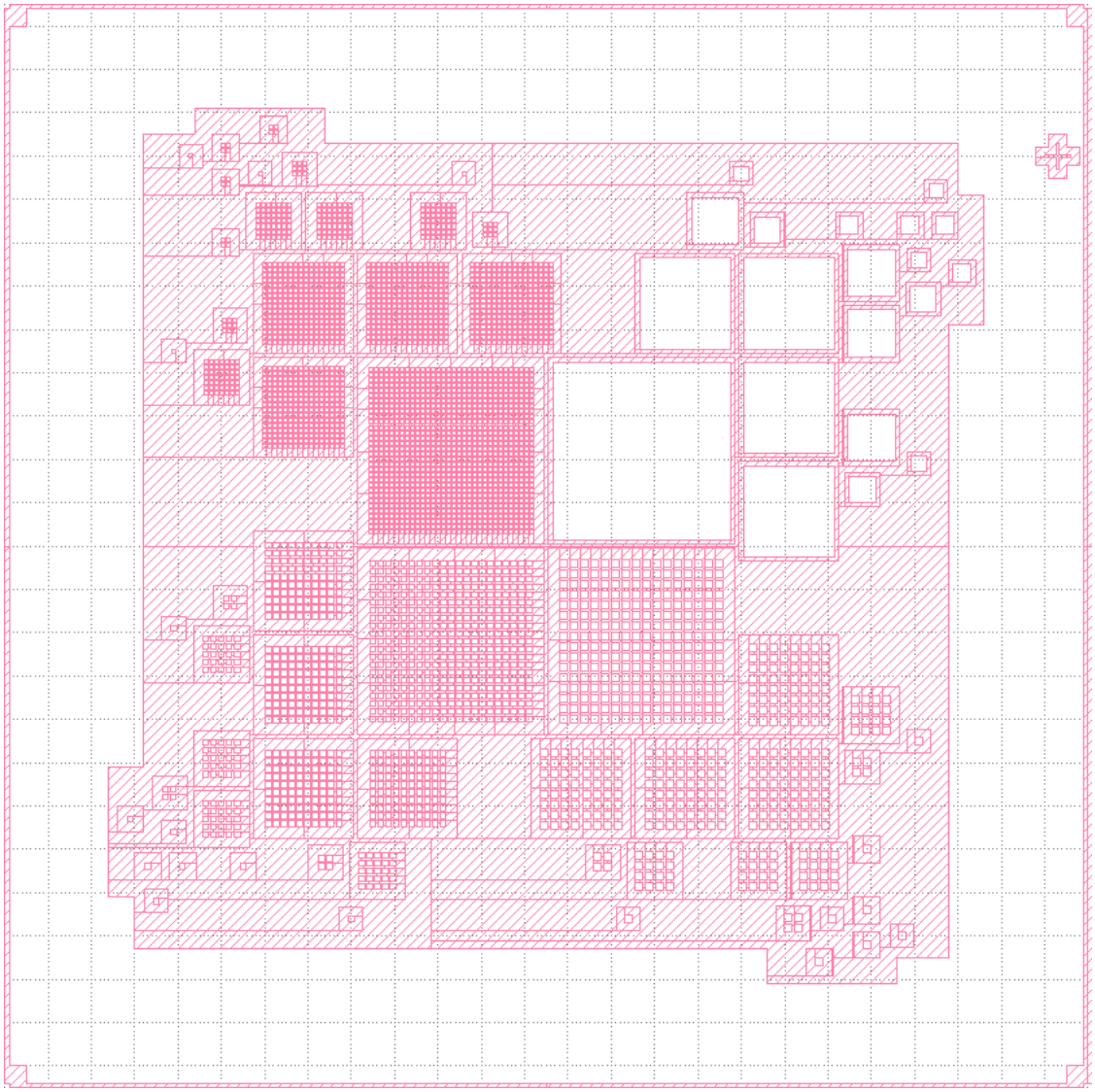


Figure 6.5: Variable size mesa (VSM) mask used for fabricating the SLED devices. The mask is geometrically symmetrical between the four quadrants; each contains mesas of different sizes partitioned mesas that help us compare the differences between them.

angles affect extraction.

6.2.1 Challenges Encountered During SLED Fabrication

Creating an IR SLED pixel smaller than a 24 μm pitch has never previously been attempted; hence we have encountered a few challenges during the fabrication

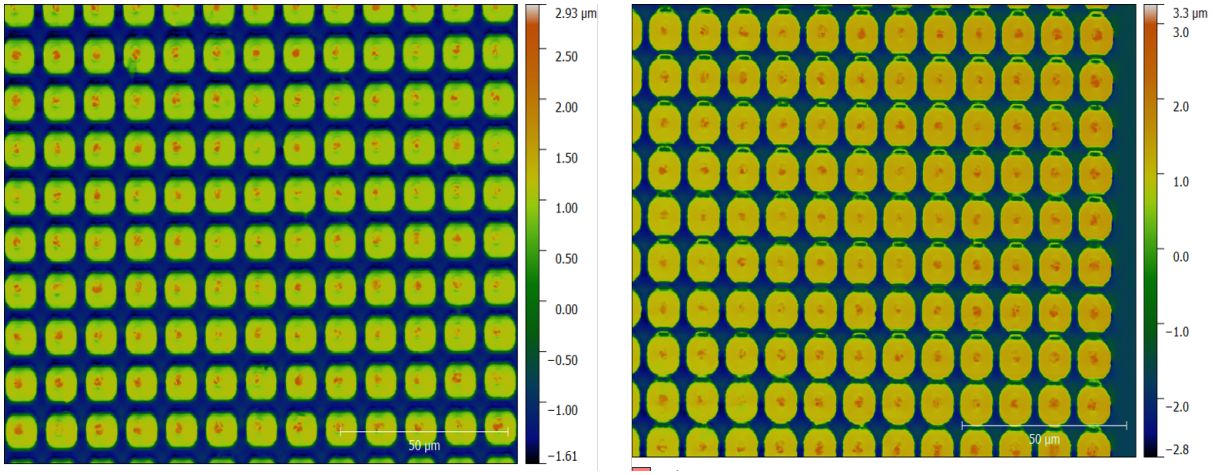


Figure 6.6: 12 μm mini-arrays for IAG739 (left) and IAG740(right). Using atomic force microscopy (AFM) to observe the height profile of the two samples reveals shorts in the trenches of the IAG740 part.

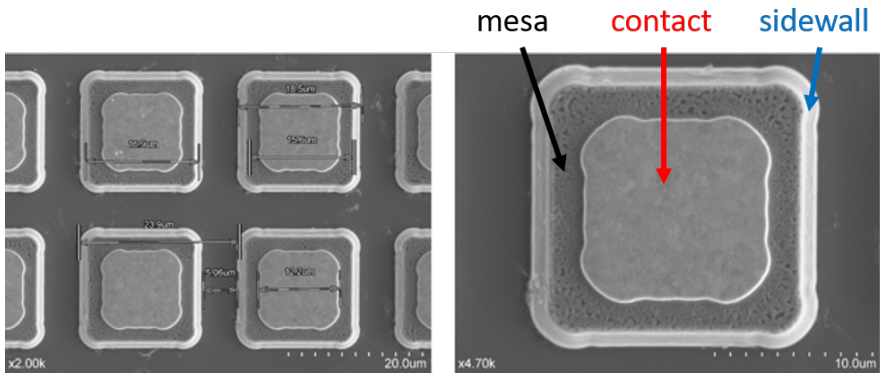


Figure 6.7: SEM for a 24 μm pitch SLED device

process. One problem can be observed in figure 6.6. The figure shows an image of two sets of 12 μm pitch mini-arrays, the one on the left corresponds to a IAG739 device with a thickness per stage of 133 nm, and the image on the right is a IAG740 device with stage thickness of 266 nm. We have observed some bridging between the 12 μm pitch devices on the thicker 740 wafer. This is likely due to poor clearance of etched material between these small devices, as the 18 μm and 24 μm pitch features on the same wafer do not exhibit this effect. Additionally, the masks used to make the

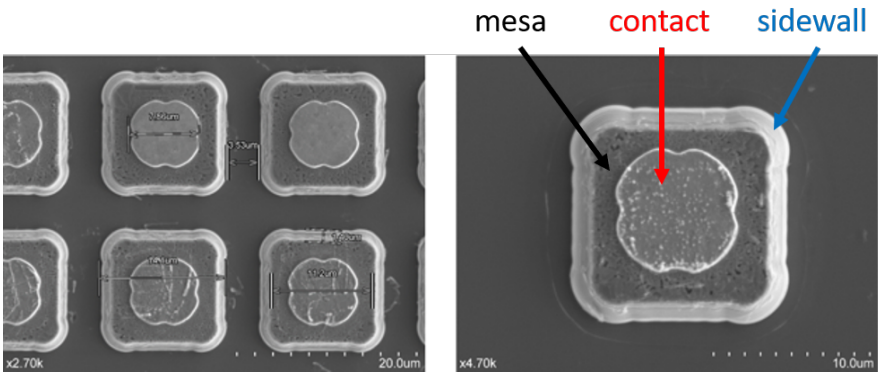


Figure 6.8: SEM for a 18 μm pitch SLED device

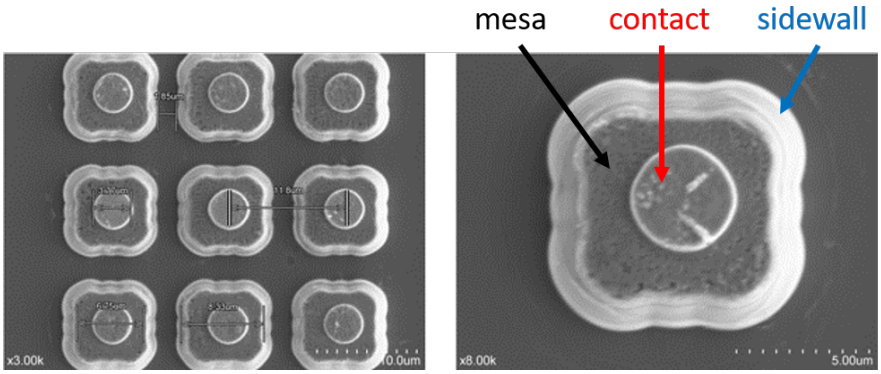


Figure 6.9: SEM for a 12 μm pitch SLED device

SLED devices have optical proximity correction (OPC) issues; the pixels and contacts are designed to be square, but as the features are made smaller, the contacts become more rounded. Scanning electron microscopy (SEM) images have been taken for small format pixels, and figures 6.7, 6.8, and 6.9 show the resulting devices created for the project. The circular contacts are more prominent on the 18 μm and 12 μm pitch SLED pixels. A new mask with better OPC will be used in the future to prevent such issues from recurring.

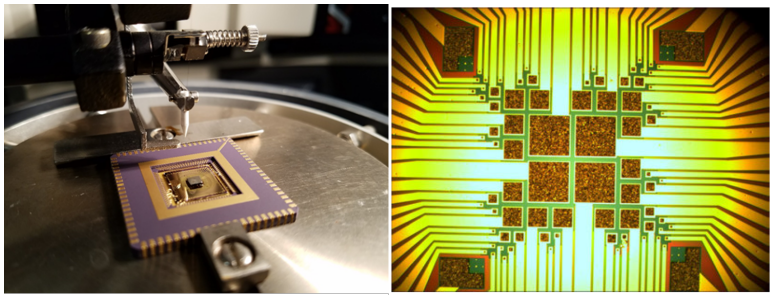


Figure 6.10: The SLED chip is first flip-chip bonded to a silicon fan-out header (right) using indium bumps[3]. After, the part is wire bonded to an 84-pin LCC package. Both of these operations are done at UIowa facilities.

6.3 Packaging of the SLED chips

The packaging of the SLED devices has been completed by Firefly Photonics using the facilities at the University of Iowa (UIowa). The devices have been flip-chip bonded to fan-out headers and then wire bonded to an 84-pin LLC package, as shown in figure 6.10. Wire bonding has proven very difficult on the smaller 18 μm and 12 μm pitch devices, resulting in a poor working pixel yield for these devices for both the single and the grouped mesas. However, it is important to note that by default the yield of the SLED devices using variable size mesa (VSM) methods is inherently low for pixels smaller than 100 μm^2[3, 64]. For more details on the packaging, refer to Appendix E.

Chapter 7

RESULTS OF TESTING THE RIIC AND SLED PIXELS

To direct future research on IRSPs based on LED technology, both hybrid components need to be restructured and the methods of hybrid construction to date must be reconsidered. This section presents the test results on the physical RIIC and SLED pixels. It is important to emphasize that no hybridization combining the two parts has been attempted; however, proof of concept testing has been completed on using the RIIC to drive the fabricated SLED pixels. Those results are also discussed in this section.

7.1 RIIC pixels test results

The RIIC circuits are packaged on a 144 PGA ceramic package, thus to test it, a PCB with a PGA socket has been designed to access all chip signals. Figure 7.1 shows how the chip mounts in the center of the PCB and all 144 pins are brought out to numbered female jumper connectors. There are also three power rails, VAA, VBB and VCC, that the user can utilize as power buses. Power and ground are supplied via a Tektronix PS2521G programmable power supply using mini-banana connectors. The primary test measurement is effected by a Keithley 24XX meter/supply. The final piece of test setup is a Digilent Electronics Explorer board used to supply the digital signals for the chip. All of these components are controlled from a control PC throughout testing. Figure 7.2 displays the described setup. The data collection is effected by the control PC and stored as a .json file; both the Tektronix and the Keithley are controlled via General Purpose Interface Bus (GPIB), and serial Recomended Standard-232 (RS-232), respectively. For a typical test, the Digilent board provided digital patterns configured with the Waves software, then, using a Python interface, the voltage and

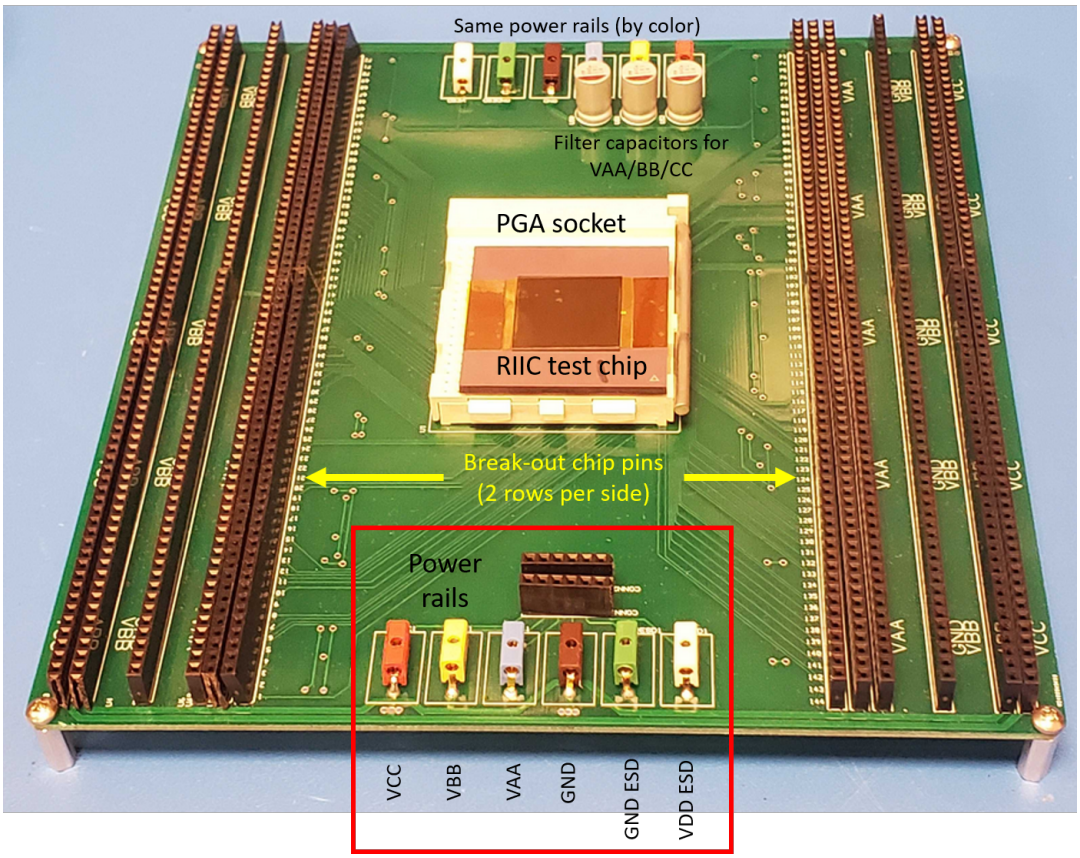


Figure 7.1: PCB used for housing the 144 PGA chips. It brings out all 144 pins to two rows of female jumper connectors. Power is brought in via mini-banana connectors, the names of the power rails are abstract (i.e. VCC does not mean voltage collector collector). Additionally, the power rails are directly connected to rows of female jumper connectors labeled on each side. Moreover, ESD diodes can be installed on the underside of the PCB if the user desires. To get a perspective for size, the packaged RIIC test chip is 1.5" x 1.5".

current levels of the power supply are set, and current measurements collected by the Keithley meter.

7.1.1 First test on the 4x4 super-pixel

The most important circuit layout to be tested is the ART-IDEA RIIC super-pixel design, as it is the basis for any future 12 μm pitch design. As mentioned in section 5.6, the circuit has 16 LED driver outputs, two analog inputs, six address lines

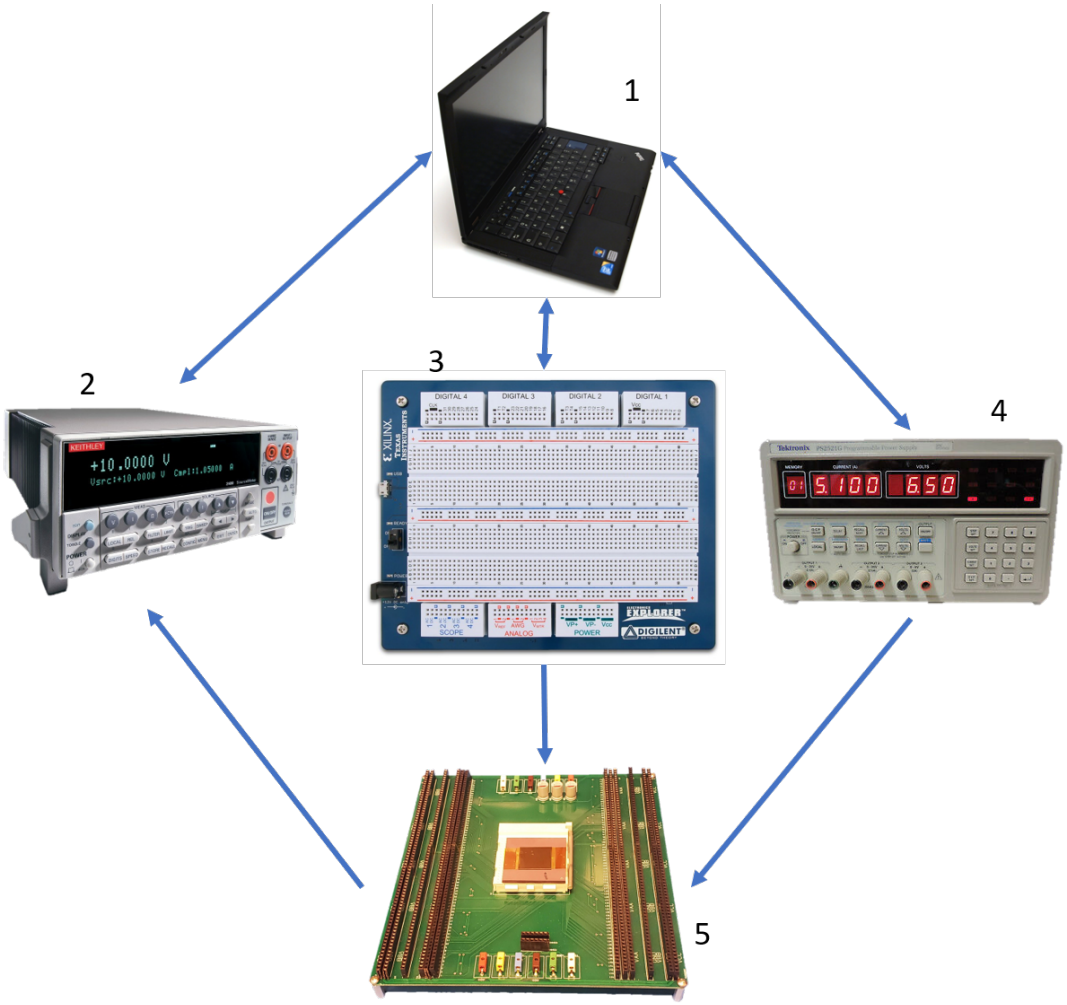


Figure 7.2: Set up used to test the RIIC chip. (1) control PC, (2) Keithley meter, (3) Digilent Explorer board, (4) Tektronix power supply, (5) RIIC chip mounted on break-out pcb

and three telemetry signals. The very first test done on this circuit is a proof of life test with the following settings:

- ***sels:*** logic LOW at 0 V using digital pin on Explorer board.
- ***x0,x1,x2,x3:*** HIGH,LOW,LOW,LOW where HIGH = 3.3 V, these use digital pins on the Digilent Explorer board.
- ***y0,y1:*** HIGH,LOW, also using the Explorer board.
- ***mselx,msely:*** tied to ground.

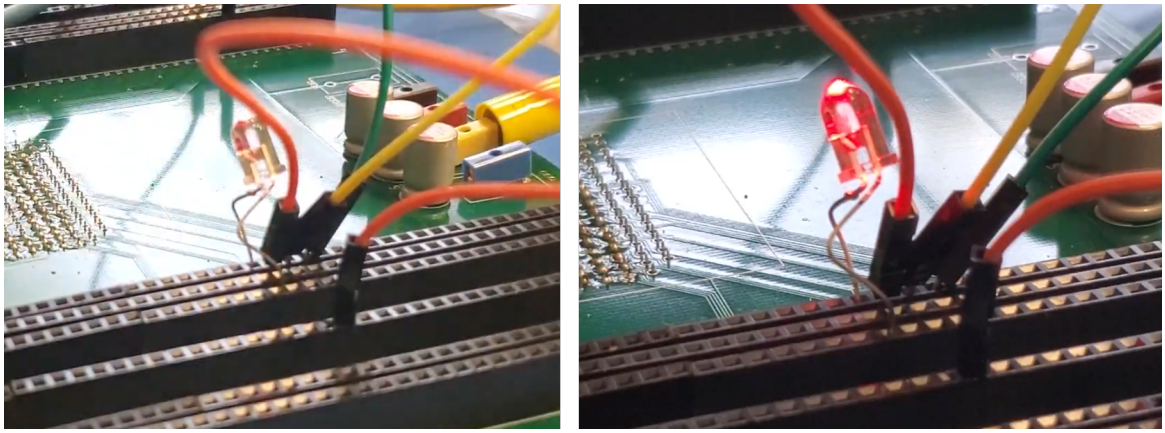


Figure 7.3: Lighting up an LED using a single RIIC pixel is the first test run on the 4x4 super-pixel. Left - the weak gear is driving the pixel. Right - the strong gear is driving the pixel

- ***vinn:*** channel 2 on Tektronix supply, set to 0 V.
- ***vinp:*** channel 3 on Tektronix supply, set to 0 V.
- ***VDD:*** channel 1 on Tektronix supply, set to 3.3 V.
- **LED line *AN*:** macro LED tied to 5 V on Keithley meter. The macro LED chosen for the first test is a standard prototyping red LED.
- **All other outputs:** tied to ground.

With the settings above, pixels AN and AP are activated for writing, however, since AP is tied to ground there will be no current flow on it, even if the analog signal *vinp* goes above the threshold voltage needed to turn on the drive transistor. Additionally, the LED power voltage on line AN has been intentionally held at 5 V just as a safety measure for the first test. For the test, all the values have been held to the settings above with the exception of the analog input *vinn*. This value is manually raised slowly to 3.3 V, as that is the maximum allowed value for this input. After successfully demonstrating light on the LED, the test has been repeated with the same settings and procedures with the exception that the *sels* signal is set to HIGH, as can be seen in figure 7.3.

7.1.2 Characterization of the RIIC pixels

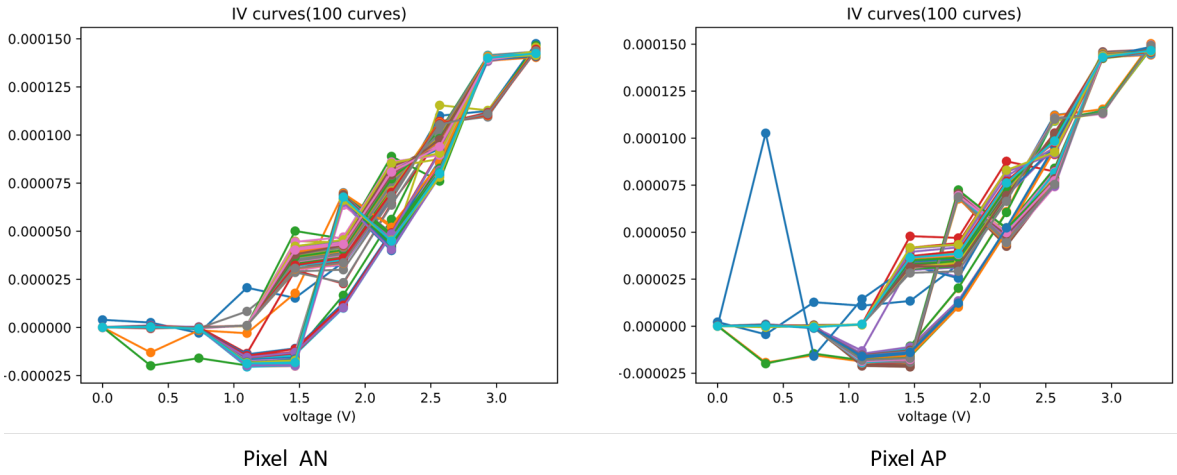


Figure 7.4: 100 sweeps of pixel AN and AP using *vinn* and *vinp* analog input signals, respectively; the weak gear has proven noisier than expected

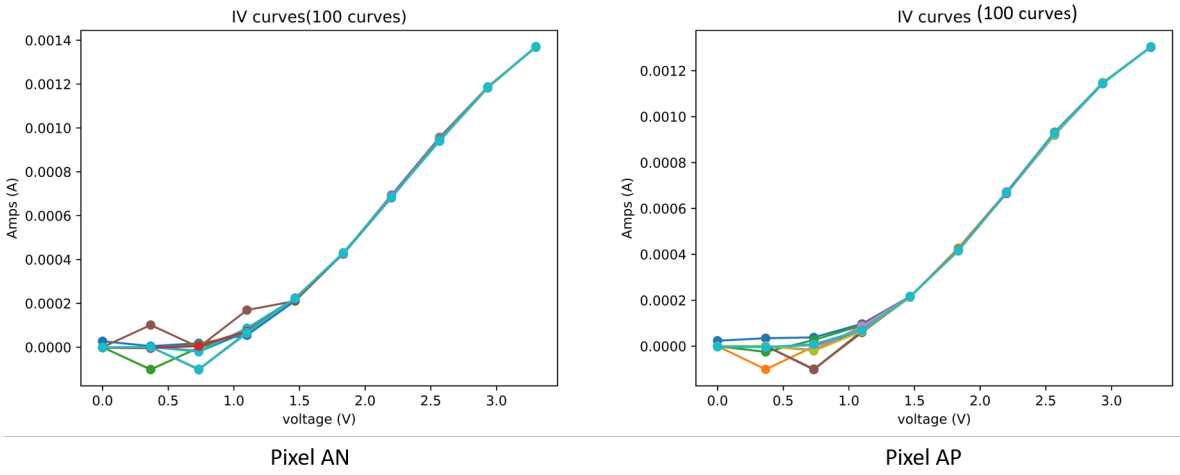


Figure 7.5: 100 sweeps of pixel AN and AP using *vinn* and *vinp* analog input signals, respectively. The strong gear worked as expected and matched simulation results

The subsequent tests collect IV data of the drive circuitry under different scenarios. The first of these series of tests has been run on pixel AN using the weak gear,

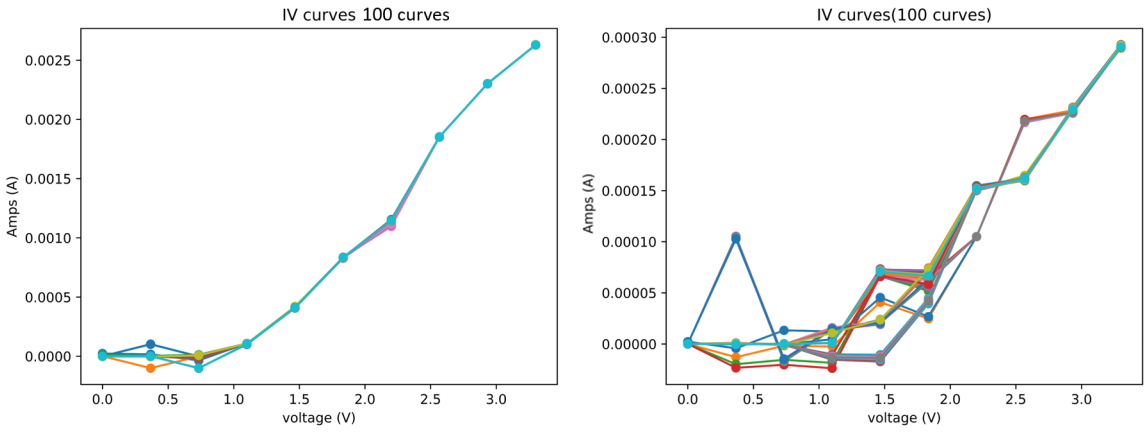


Figure 7.6: 100 simultaneous sweeps of pixel *AN* and *AP*. Since both *vinn* and *vinp* are run simultaneously the current doubles as expected

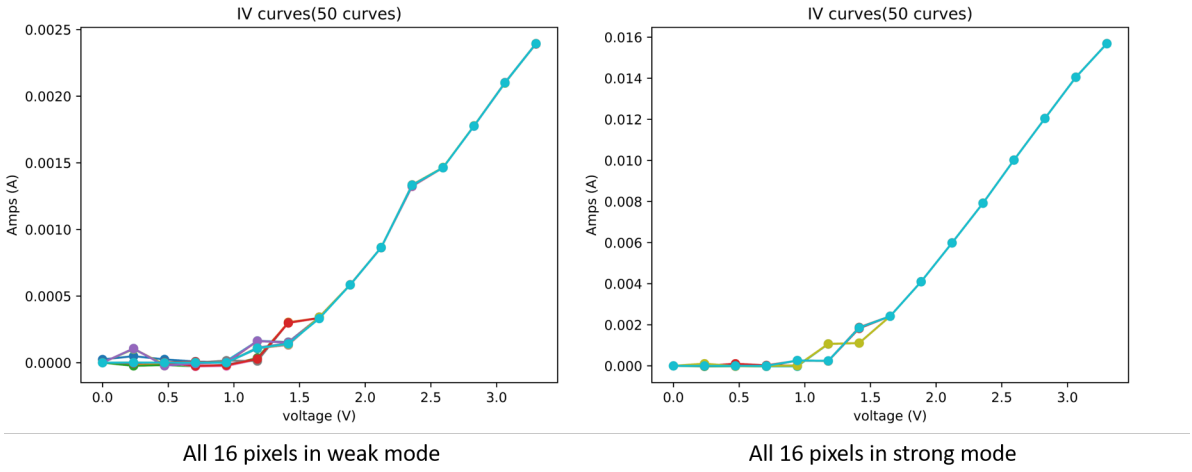


Figure 7.7: 50 simultaneous sweeps of all 16 pixels. The total current output for both gears increases accordingly.

sweeping the analog *vinn* signal from 0 V to 3.3 V with a total of 10 steps in between. The test is repeated 100 times on the same pixel using a macro LED as the load. The LED power is supplied by the Keithley and kept constant at 5 V during the duration of the sweep. Since there are two analog inputs per pixel pair, *AP* was tested with the same methods, but with *vinn* held at 0 V while *vinp* was swept from 0 V to 3.3 V.

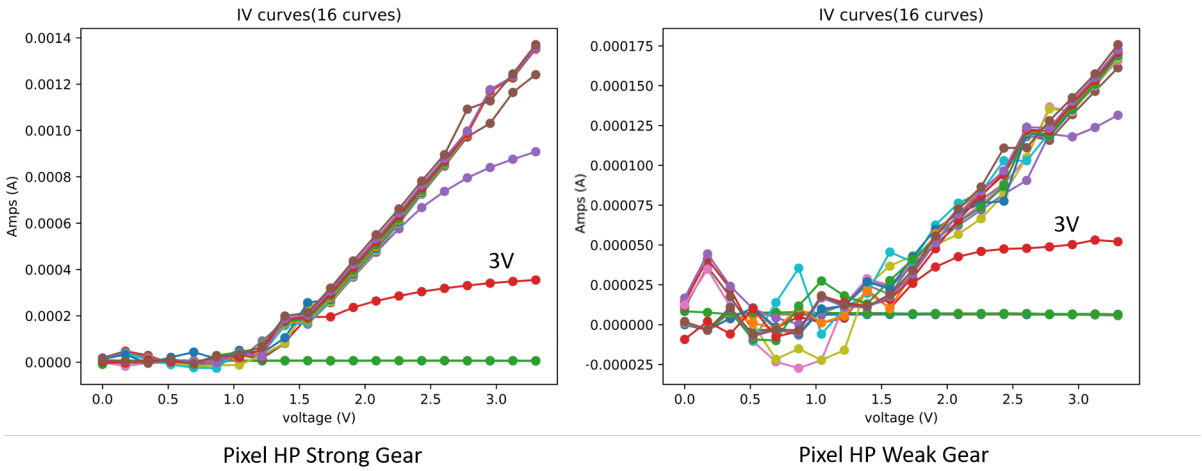


Figure 7.8: Parametric sweep displaying the behavior of both gears with a varying voltage on the LED supply from 0 V to 15 V, with increments of 1 V. For every step, *vinp* is swept from 0 V to 3.3 V.

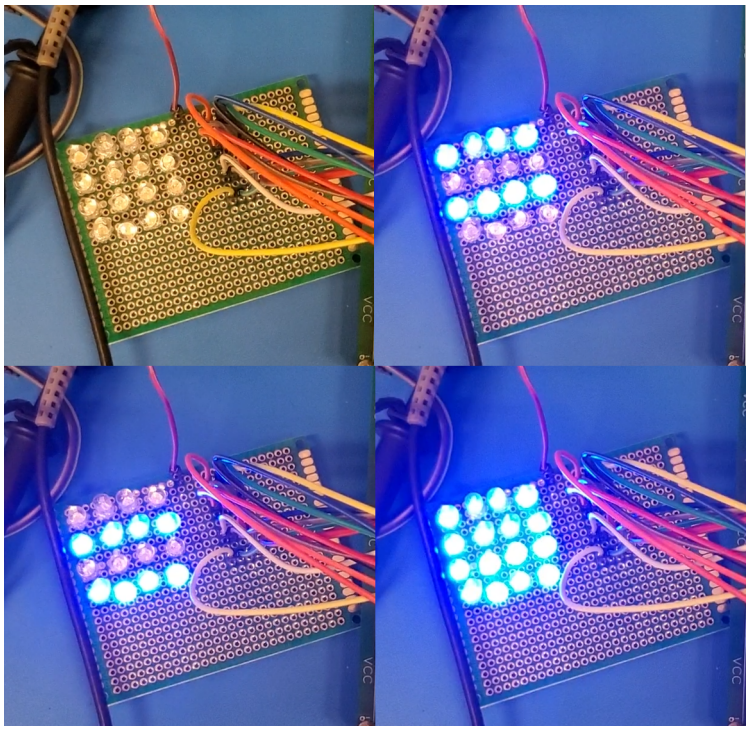


Figure 7.9: A 4x4 mini-grid of macro LEDs being driven by the 4x4 RIIC super-pixel

The resulting IV curves for the weak gears of pixel AN and AP are shown in figure 7.4. The following plots in figure 7.5 display the results of sweeping the strong gear for the same pixel pair, maintaining the settings as the weak gear test, but with the *sels* bit set HIGH. This is also repeated 100 times for each pixel to obtain a better idea of consistency and repeatability of the pixels. For currents of $\sim$200 μA, the RIIC demonstrates adverse noise effects; this is very noticeable on the weak gear. This is likely due to the improvisational nature of the test setup as jumper wires are used to make the connections necessary for the test. Nonetheless, for a future iteration of the test chip, it is worthwhile to investigate ways to make the weak gear less prone to noise.

The next set of tests run on the RIIC super-pixel aim to verify that multiple pixels can operate at the same time and to determine the effect that it has on current draw. For these tests, multiple address lines within the pixel are selected. In the first example shown in figure 7.6, only address lines *x0*, *y0* have been enabled to activate pixels AN and AP. For the example shown in figure 7.7, all of the address lines have been enabled, thus putting all the pixels in write mode. The current consumption increased more or less linearly with the number of pixels turned on. Interestingly, the noise observed on the weak gear for single pixel sweeps is not observed when all pixels are enabled, as the total current output exceeds $\sim$200 μA.

During the design stage, simulations of the NLDMOS have demonstrated that the gears can be operated at voltages up to 15 V with a very stable current output, as explained in section 5.1.1. Figure 7.8 shows the IV curves for a parametric sweep where *vinp* varies from 0 V to 3.3 V and the LED power line increases by 1 V after every sweep, up to the maximum allowable voltage of 15 V. For this test, the first voltage point able to turn ON the LED is 3 V. After setting the LED power line to 5 V and higher, there is very little change in the current output of the gears. As expected with this design, we have the ability to adjust the LED voltage supply depending on the types of IR LEDs used and their turn-on voltages.

The remaining tests run on the RIIC address the proofs of concept of other aspects of the design, for instance, creating input patterns that activate certain pixels,

sweeping every pixel individually to ensure their functionality, or testing the other circuits, such as the tiled super-pixel or the improved drive circuit. An example of such a test is depicted in figure 7.9. In this example, all of the pixels have been activated via their respective address lines, strong gear is enabled on all pixels, and the *vinn* and *vinp* values change via a 2-bit counter once per second. When *vinn* is HIGH, the top and third rows light up, and when *vinp* is HIGH, the second and bottom rows light up.

7.2 SLED pixels test results

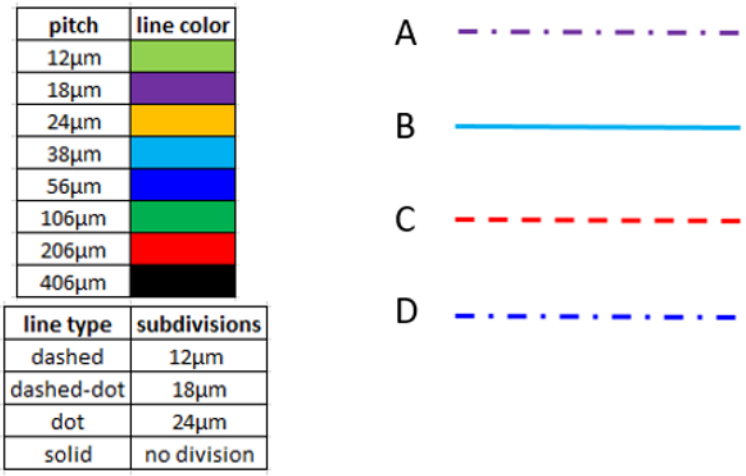


Figure 7.10: Legend for reading SLED plots. Solid lines = single mesas. Broken/dotted lines: Dashed = 12 μm pitch subdivisions, Dash-Dot = 18 μm pitch subdivisions, Dot = 24 μm pitch subdivisions. Knowing this legend is key to understanding the LV curves in this section. Examples: Sample A is purple, denoting an 18 μm x 18 μm mesa, and the Dash-Dot line means it has been subdivided to make a 18 μm pitch SLED device. In this particular case, only one device fits in that area. Sample B is a very straightforward 38μm x 38μm mesa from quadrant 1 with no subdivisions. Sample line C is a 206 μm x 206 μm mesa subdivided into 12 μm pitch pixels. Finally, D is a 58 μm x 58 μm mesa with 18 μm pitch subdivisions.

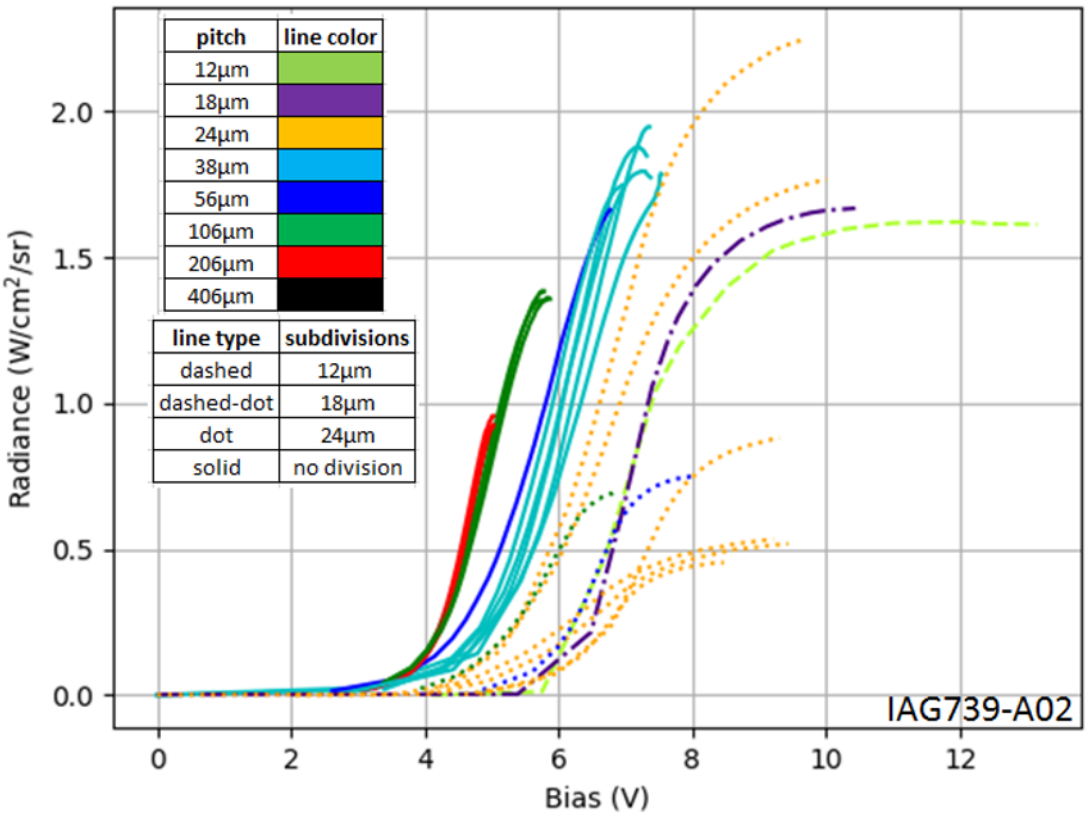


Figure 7.11: SLED test chip IAG739-A02 radiance vs. voltage

The SLED testing has been performed at UIowa facilities by the team that grew the LEDs for the project. The testing has been done in a JK Henriksen CTS-1360 Dewar at 77 K. As devices under test emit in the MWIR spectrum, an indium-antimonide (InSb) detector has been used for all data collection. It is worth mentioning that the test chips display a very low yield for 24 μm, 18 μm and 12 μm pixels. Much of the yield issues arise from the flip-chip bonding of the SLEDs chip to a Si fan-out header and the wire bonding process, not the smaller mesas. The following plots in this section show the radiance of several test chips tested. The radiance for mesas larger than those found on the 24 μm pitch devices behaved and emitted light as expected

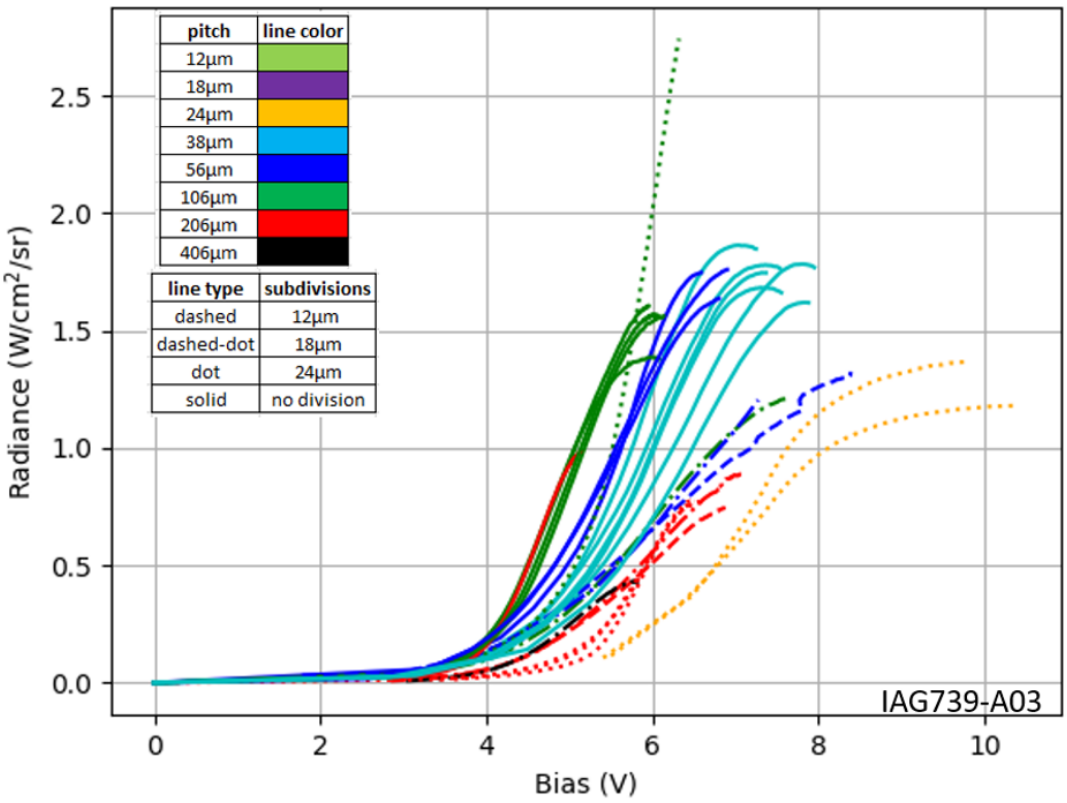


Figure 7.12: SLED test chip IAG739-A04 radiance vs. voltage

for a device with eight stages. However, the small-format pixels display very scattered, low radiance results across the data collected.

In section 6.2, it has been discussed how the SLED devices come in different sizes, and for some of the quadrants on the wafer, these areas have been subdivided to create mini-arrays of small format pixels. Figure 7.10 provides the legend for reading the plots in this section. Before analyzing the data collected, it is important to understand how to read the plots. The radiance-versus-voltage plots in figures 7.11, 7.12 and 7.13 correspond to three different SLED test chips. The 8-stage devices have been chosen to reduce the turn-on voltage of the pixels, however, according to the data collected, the turn-on voltage is higher than desired, ranging from 4 volts for large mesa devices to 6 volts for small mesa devices. The trend of increasing light extraction

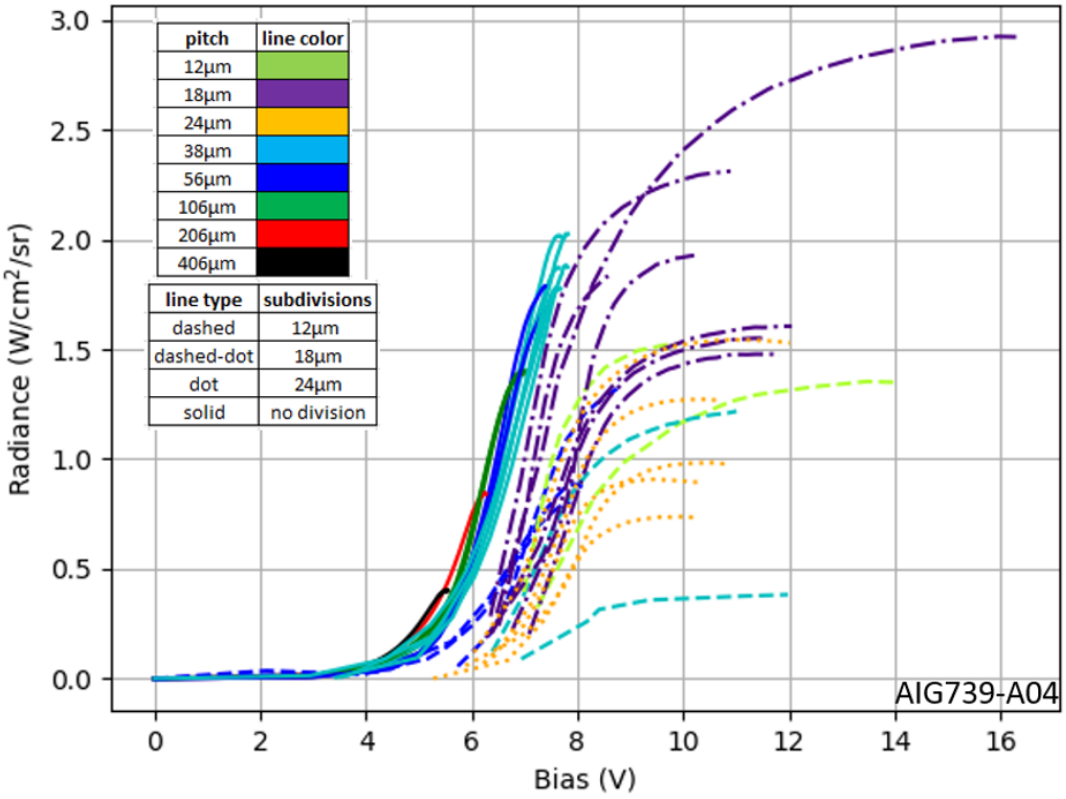


Figure 7.13: SLED test chip IAG739-A04 radiance vs. voltage

can be observed on all of the test chips for larger pixels. However, the small-format devices, pixels with a pitch of 24 μm or less, had very scattered results. For instance, on chip IAG739-A02, the pixel with the highest radiance had a pixel pitch of 24 μm; however, on that same test chip other 24 μm pitch devices performed very poorly. The 12- and 18- micron pitch devices on IAG739-A02 did not perform better than their larger counterparts, and both had similar radiance.

Test chip IAG739-A03, figure 7.12, reveals some interesting results. A mesa of 106 μm^2 subdivided into a mini-grid of 24 μm pitch pixels radiates more light than the devices of the same area and no partitioning. Another interesting result can be observed by studying the red plots of test chip IAG739-A03. The solid red line is a non-divided mesa with an area of 206 μm^2, other red lines with either a dashed or a

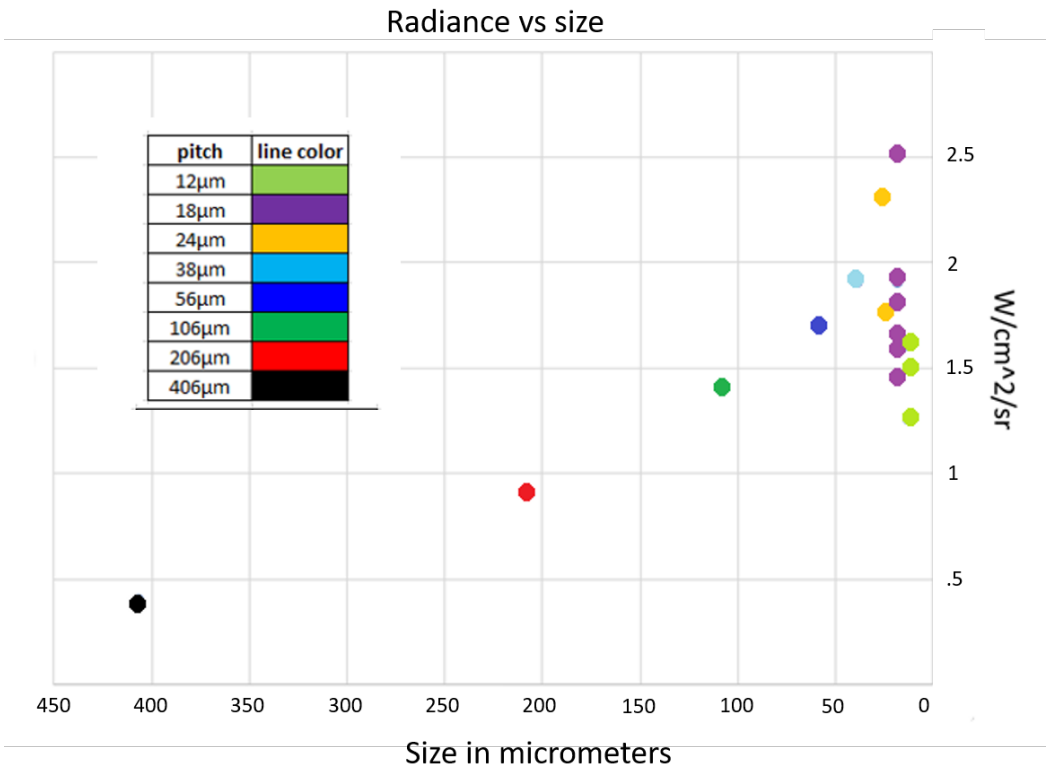


Figure 7.14: Comprehensive view of SLED devices tested. Each dot represents a single device with the highest radiance observed for devices of that size (see color legend). Small-format pixels have conflicting results, thus multiple are plotted. Data plotted is an aggregation of result from IAG739 chips.

dotted pattern represent mini-grids of 12 μm pitch and 24 μm pitch, respectively, in an area of 206 μm^2. All of these devices show similar light output; however, the expected outcome is an improvement in light extraction from the small-format mini-grids. Test chip IAG739-A04 in figure 7.13, displays the device with highest radiance, an 18 μm. However, this device appears to be an outlier, as others of the same pitch exhibit lower radiance. A comprehensive graph that summarizes the results across tests can be studied in figure 7.14. The plot compares the maximum light output observed for pixels of different sizes. The large-format pixel had very similar results across testing, thus only one dot is plotted to represent them. The small-format pixels, on the other

hand, had significant variance, thus more than one dot is used to show the mixed results. More data collected for each of the test chips can be found in Appendix E.

Overall the small-format pixels performed very poorly, with a large discrepancy among results on all test chips. During the growth process, the MBE chamber had contamination and the mask had optical proximity issues for small-format pixels. Additionally, flip-chip bonding and wire bonding proved to be difficult using the available equipment at UIowa. All of these are possible causes for the low yield exhibited by the SLED test chips. To obtain better results, a second growth is necessary; the second run needs to include a better set of masks with OPC, and the flip-chip bonding and wire bonding with better equipment. There is also a limit at which shrinking the pixel will no longer improve light extraction. Knowing where that limit lies is another good incentive for a second run for these experiments. On the bright side, MWIR light has been demonstrated from a 12 μm pitch pixel for the first time using IR technology. Although more research is necessary, a working 12μm pitch pixel makes it feasible to obtain a 4Kx4K array.

7.3 Combined test results

The final goal for any mature IRSP system based on LED technology is to create a working hybrid of the RIIC and SLED parts. This process is very expensive and usually exclusive to mature parts, not experimental devices. Nonetheless, it is worthwhile to combine the RIIC and LEDs created for this project to determine how well they work together. The test setup for these experiments is nearly identical to that presented in section 7.1 and figure 7.2, but with the addition of a PLCC84 socket to hold the SLED test chips and a FLIR SC6800 camera, as shown in figure 7.15. One of the most important tests is to demonstrate the ability of the RIIC to light and control the brightest of the LEDs. For this test, the LED power supply has been held to 15 V using the Keithley meter then the RIIC configured to step through the full analog input range of 0 V to 3.3 V. A working LED on the SLED test chip is tied to pixel AN on the RIIC using jumper wires. Images from the successful test of the light captured

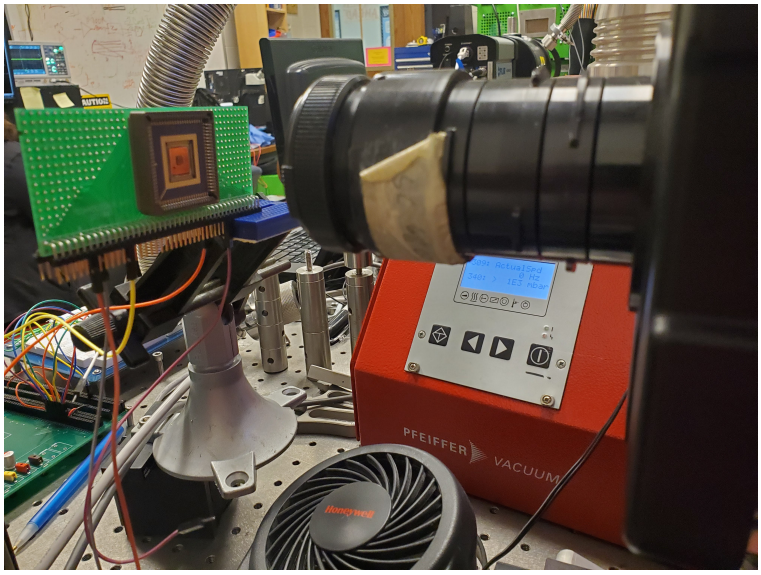


Figure 7.15: To test the SLED test chips in conjunction with the RIIC test chip, a PLCC86 socket has been added to the test set up to hold the SLED test chips, and a FLIR SC6800 camera to capture the light.

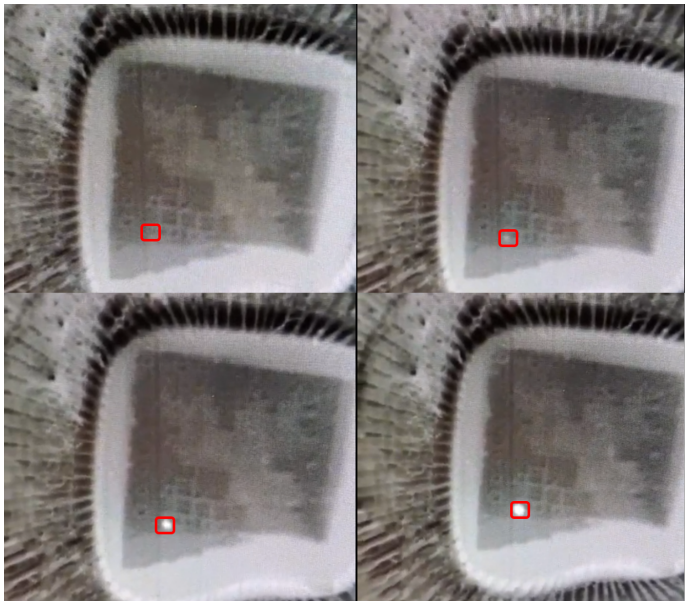


Figure 7.16: Using the RIIC pixel to drive a SLED pixel at different light intensities. Light, current and voltage (LIV) data that correspond to this image are in figure7.18.

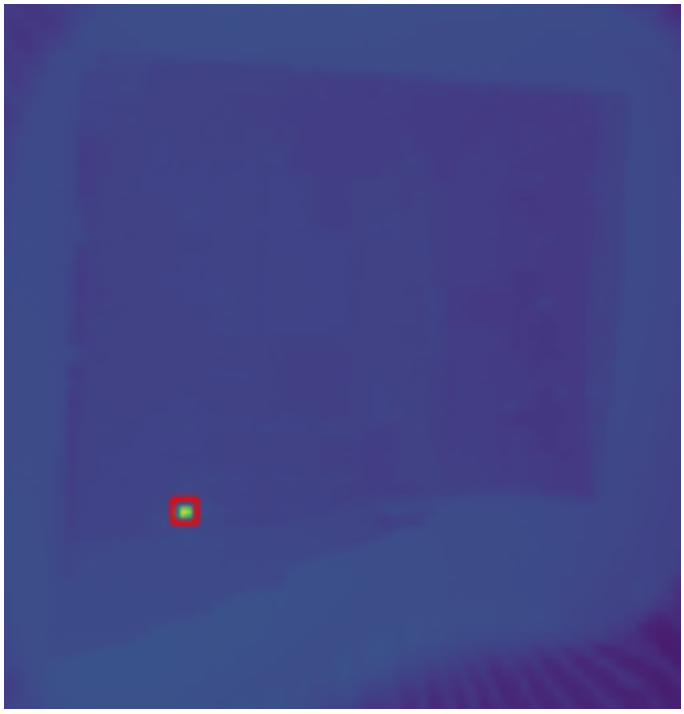


Figure 7.17: Post-processed camera image captured for a 38 μm^2 mesa SLED device on test chip IAG739-A02 line 2 using strong gear.

by the camera are shown in figure 7.16. From left to right and top to bottom, the image captures different stages of light emission as the control analog signal ramps up.

Three SLED test chips have undergone testing at UDel's facilities, each with a slight process variations. Plots for SLED chip IAG739-A02 are discussed in this section, as it has 8-stage devices with 133 nm per stage thickness. The other two test chips are more experimental, and their results can be found in Appendix F. The following plots in this section demonstrate the correlation between the light captured by the IR camera in units of camera-counts and the current consumption of the pixel. The data is collected by stepping the drive gear from minimum to maximum value using the *vinn* analog control signal and keeping the LED power at 15 V. Additionally, all the SLED pixels have been driven by pixel AN of the RIIC. A total of twenty steps are taken between 0 V and 3.3 V, and for each of these voltage steps, ten camera frames are captured. The camera is set to process frames at 100 Hz with an integration time

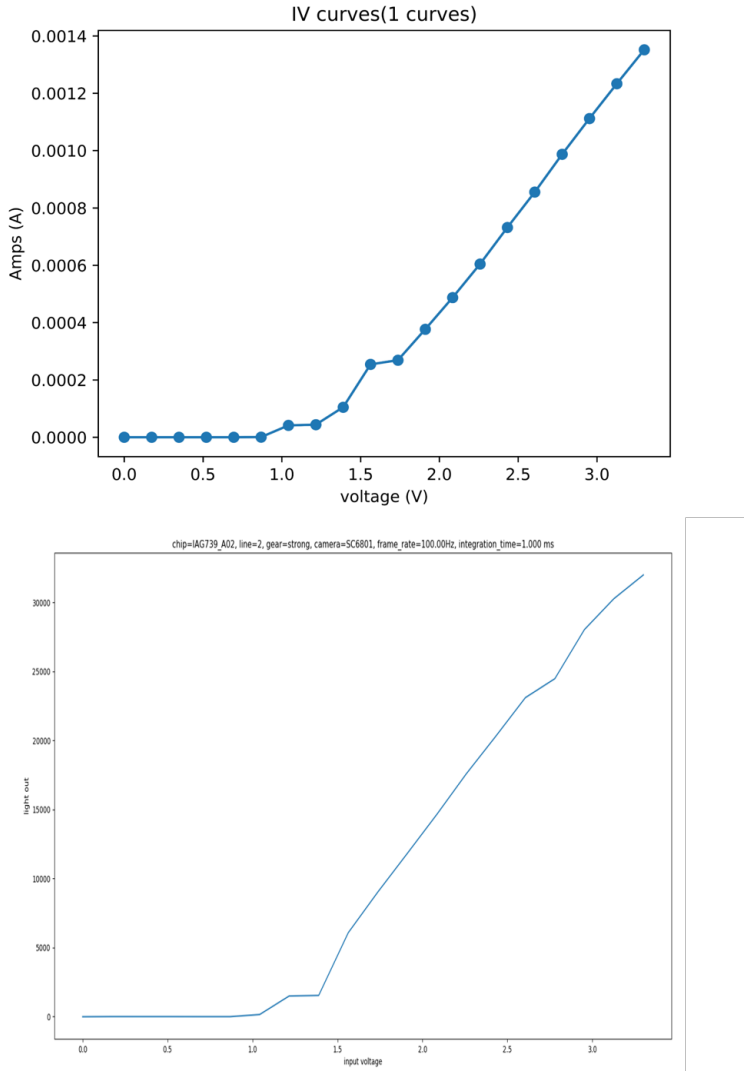


Figure 7.18: Top - LED current as a function of RIIC pixel voltage. Bottom - Light captured in camera-counts as a function of RIIC pixel voltage. LED tested - 38 μm^2 mesa SLED device on test chip IAG739-A02 line 18 using strong gear.

of 1 ms. Frames captured by the camera are processed via background subtraction, where the background frames are collected before any light is emitted from the pixel. Ideally, the resulting difference should be enough to determine the total light captured by the camera; however, due to ambient noise, a region of interest is required around the pixel of interest to eliminate the noise[65]. All of the testing done on the chips is

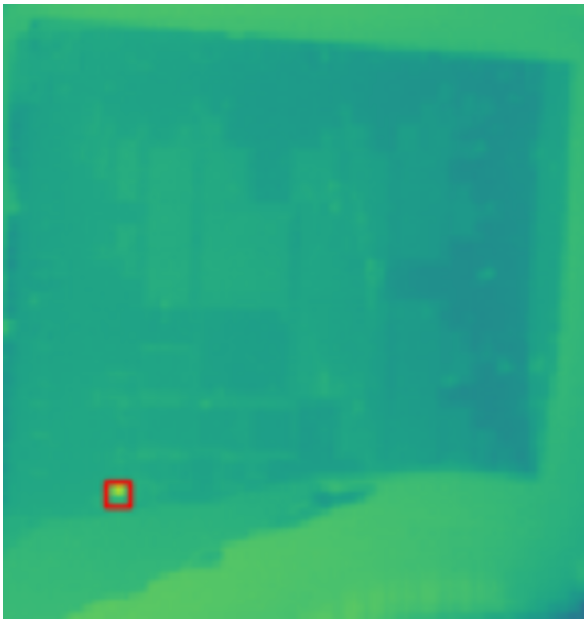


Figure 7.19: Post-processed camera image captured for a 38 μm^2 mesa SLED device on test chip IAG739-A02 line 2 using weak gear.

performed at ambient temperature, about 300 K. Figures 7.17 through 7.20 show the results for a 38 μm^2 mesa for both the weak and strong gears. Figures 7.21 and 7.22 present the test results for a 12 μm pitch SLED device.

As discussed in section 5.1.1, the gears on the RIIC super-pixel are compatible with LEDs of various turn-on voltages, as the NLDMOS current stays relatively constant from 4 V onward. The current measure on the 38 μm^2 SLED device is identical to the current measured on the macro LED for both the weak and the strong gear. It is important to note that the turn-on voltage for a macro LED is usually less than a volt, whereas the turn-on voltage for the particular SLED device shown in the figures is 6 volts. This gives a turn-on voltage of 750 mV per stage for these chips. The pixel data collected shown in figure 7.22 is slightly different from the data collected on the same test chip for other SLED devices, as a saturation point was reached on the device. This is believed to be a device-specific behavior likely due to the low yield of the chips and the temperature not being at 77 K during testing.

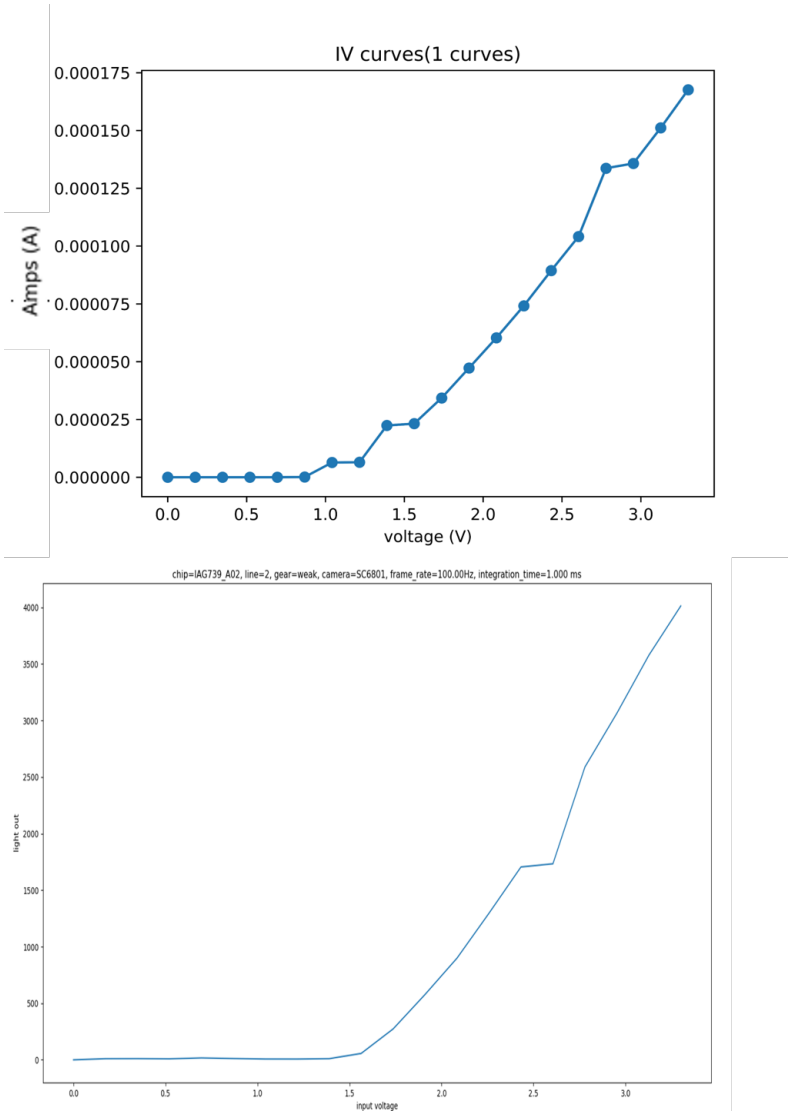


Figure 7.20: Top - LED current as a function of RIIC pixel voltage. Bottom - Light captured in camera-counts as a function of RIIC pixel voltage. LED tested - 38 μm^2 mesa SLED device on test chip IAG739-A02 line 18 using weak gear.

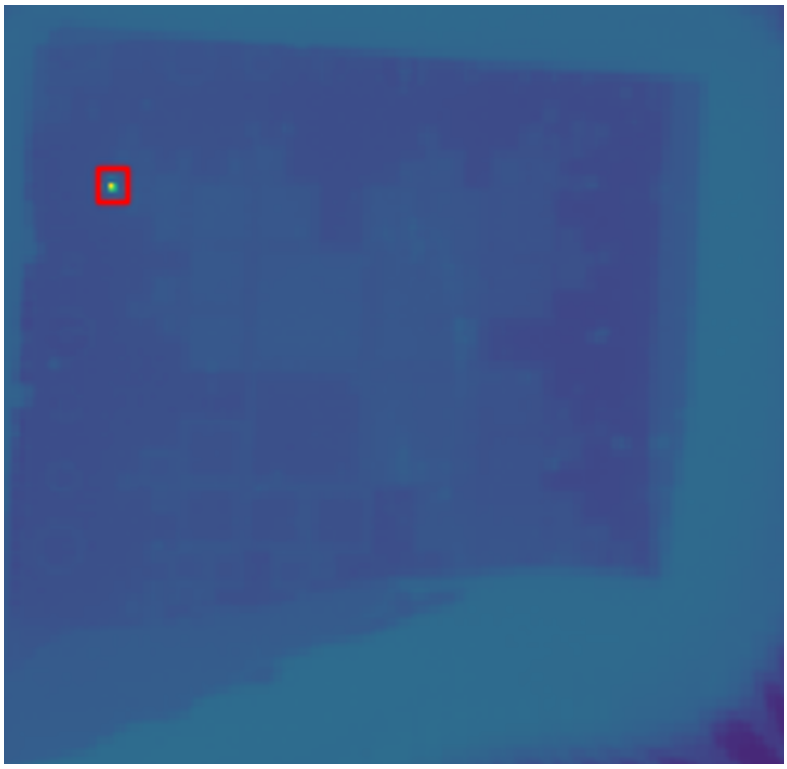


Figure 7.21: Post-processed camera image captured for a 12 μm pitch SLED device on test chip IAG739-A02 line 2 using strong gear.

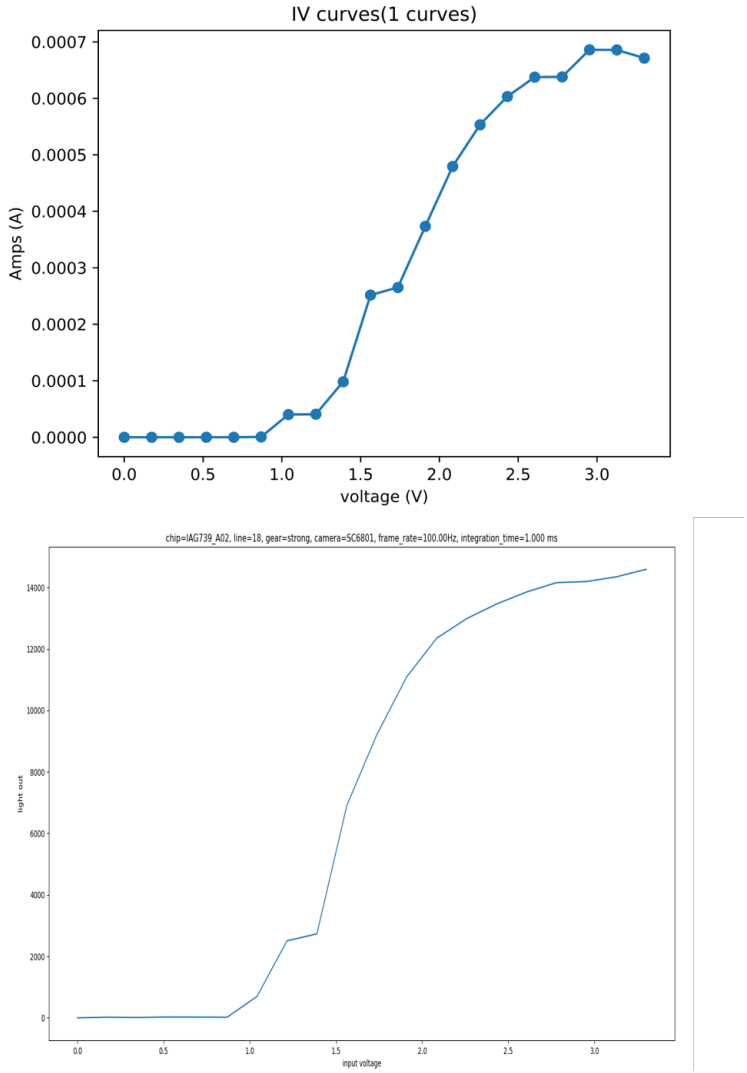


Figure 7.22: Top - LED current as a function of RIIC pixel voltage. Bottom - Light captured in camera-counts as a function of RIIC pixel voltage. LED tested - 12 μm pitch SLED device on test chip IAG739-A02 line 18 using strong gear.

CONCLUSION

Infrared scene projectors are valuable tools used in hardware in the loop test scenarios. Over the years, the sensor technology has advanced substantially and reached very high resolutions. MWIR cameras and sensors are no exception to this advancement in technology. Demands for brighter, faster and higher resolution IRSPs are at an all-time high, as they provide a cost-effective solution to field testing. In 2008, CVORG, a research group led by Dr. Fouad Kiamilev at the University of Delaware, became involved in the study of creating better IRSPs using LED technology. The emitter array since developed consists of two main components, the RIIC and the SLEDs, which are bonded together via flip-chip bonding using indium bumps.

The very first successful LED-based IRSP was produced in 2014 with a resolution of 512 x 512 pixels. Although it had some limitations in its dynamic range, it proved the technology was viable and opened the path for further research. In the following years, a variety of IRSPs have been developed, including TCSA, a two-color system with a resolution of 512 x 512, NSLEDS, a single color 1024 x 1024 pixel resolution system, and HDILED, a high definition 2048 x 2048 pixel resolution system. The most successful systems developed to date have been the NSLEDS projectors, and much of their success is due to the higher yields per wafer. However, a 1024 x 1024 projector does not have the resolution desired for system testing. HDILED, on the other hand, has the resolution desired, but due to its 24 micrometer pixel pitch (the same as NSLEDS), its physical size has a huge impact on yield and makes production very expensive.

The work described in this dissertation explores a new approach to increasing the density and resolution of pixels for future IRSPs. This is the very first time we have changed the fabrication process of the RIIC, as we have moved away from the

AMIS500 process to the ONC18 process. Additionally, the architecture of the RIIC super-pixel has been modified for better optimization of available space. The results of the new RIIC architecture are very favorable, as the 4x4 super-pixel design works reliably. The use of NLDMOS as drive gears makes the new RIIC very adaptable to various types of LEDs with different turn-on voltages or numbers of stages.

On the SLED side, the LED pixels have been created using VSM techniques, including the very first instances of LEDs with a pitch of 18 μm and 12 μm in MWIR. The results for the SLED devices have been successful in demonstrating light emission from the 18 μm and 12 μm pitch pixels. However, results are inconclusive as to whether decreasing the size of the pixel past 24 μm pitch helps with light extraction. During fabrication, proximity issues have been experienced with the lithography of small-format pixels, and an MBE contamination problem occurred that may have skewed the characteristics of the SLED devices.

Since the completion of this project, more collaborations between UDel, CDS, Firefly and UIowa have started with the goal of exploring improvements to the SLED technology. Current efforts could improve the efficiency of SLED pixels up to 7X. It is certain that higher resolution arrays will remain a priority until resolutions of 4096 x 4096 or higher are reached. The RIIC super-pixel designed and proven to work by this project will be a major contribution in the progression to such resolutions.

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Appendix A

GLOSSARY OF TERMS

Table A.1: List of terms 1

AFB	Air Force Base
AFM	Atomic force microscopy
AIREA	Advanced infrared emitter array
ART-IDEA	Advanced RIIC technologies for increasing density of emitter arrays
C	Capacitance
CDS	Chip design systems
CMIM	metal-insulator-metal capacitor
CMOS	Complementary metal oxide semiconductor
CNT	Carbon nanotube
COTS	Commercial off-the-shelf
CSE	Close support electronics
DRC	Design rule check
ESD	Electrostatic discharge
FLIR	Forward-looking-infrared
FPA	Focal plane array
GaSb	Gallium antimonide
GND	Ground
GPIB	General purpose interface bus
GUI	Graphical user interface
GWEF	Guided weapons evaluation facility
HDILED	High definition infrared light emitting diode
HWIL	Hardware in the loop
IC	Integrated circuit
InSb	Indium antimonide
IR	Infrared
IRSP	Infrared scene projector
LCD	Liquid crystal display
LCoS	Liquid crystal on silicon
LED	Light emitting diode
LLC	Low liability company
LVS	Layout versus schematic
MBE	Molecular beam epitaxy
MCW	Multi-contact wedge
MEM	Microelectromechanical
MOUT	Monitor-out
MWIR	Mid-wave infrared
NLDMOS	N-type laterally diffused metal oxide semiconductor
NMOS	N-type metal oxide semiconductor
NSLEDS	Night-glow super-lattice light emitting diode system
OnSemi	OnSemiconductor

Table A.2: List of terms 2

OPC	Optical proximity correction
PCB	Printed circuit board
PEX	Parasitic extraction
PGA	Pin grid array
PMOS	P-type metal oxide semiconductor
R	Resistance
R&D	Research and development
RF	Radio frequency
RIIC	Read-in integrated circuit
RS-232	Recommended standard 232
SBIR^{g}ov	Small business innovation research
SBIR	Santa Barbara infrared
SEM	Scanning eletron microscopy
SL	Super-lattice
SLED	Super-lattice light emitting diode
SLEDS	Super-lattice light emitting diode system
SPI	Serial peripheral interface
T&E	Test and evaluation
Udel	University of Delaware
UIowa	University of Iowa
UUT	Unit under test
VDD	Voltage drain drain
VLSI	Very large scale integration
VSM	Variable size mesa

Appendix B

EXPERIMENTAL CIRCUIT SIMULATIONS AND FIGURES

This is supporting material for section 5.6.1. It contains the results of the simulations performed and the circuits used to simulate them. The results have been used to determine the correct components to be used to improve the drive circuit of the ART-IDEA pixel. The final drive circuit resulting from these experiments has been laid out in Cadence and incorporated in the final chip layout to be fabricated by OnSemi. The new prototype drive circuit has a reset line added to the node at the memory capacitor to fully discharge it and a properly sized series NMOS transistor to the weak gear to allow for finer control of the lower end of light emission.

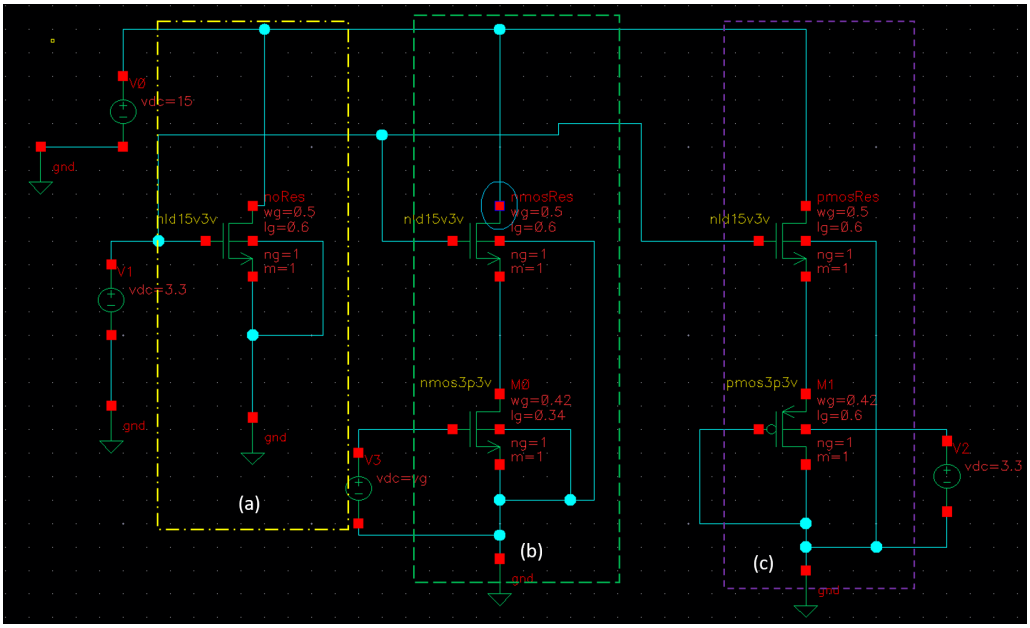


Figure B.1: Cascoding transistors simulation schematic. The three paths are, (a) stand-alone NLDMOS, (b)NLDMOS with a series NMOS, (c) NLDMOS with a series PMOS.

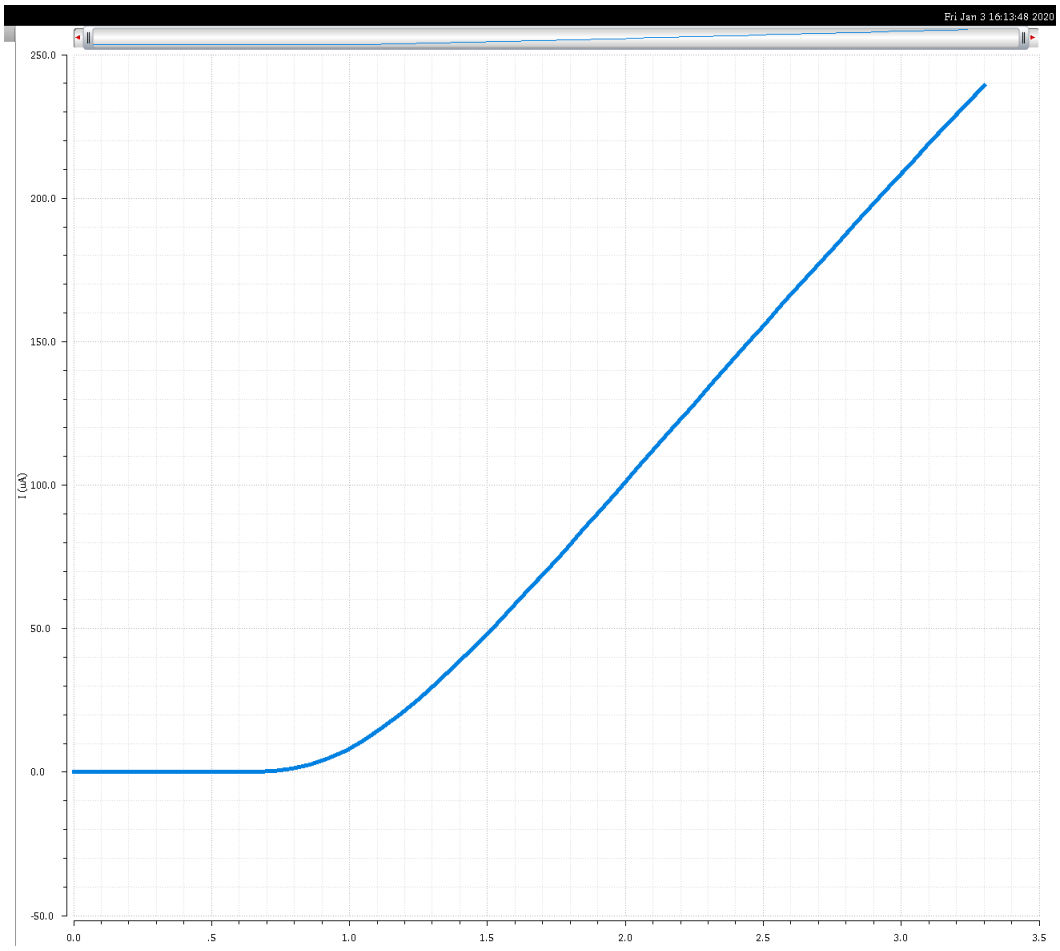


Figure B.2: For reference, this is the current vs. voltage curve for the weak gear NLDMOS of the ART-IDEA pixel.

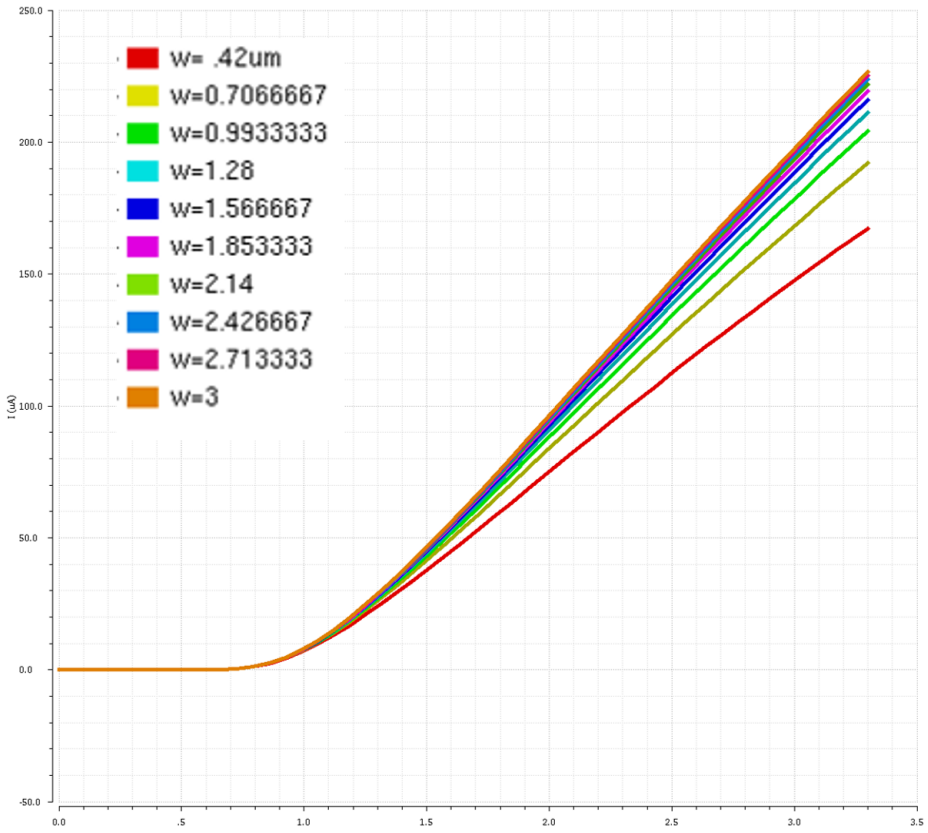


Figure B.3: Varying the width of the series NMOS transistor does not have as large an effect as expected. This is because the larger the width of the device, the wider the channel. In other words, there is a bigger highway for electrons to flow.

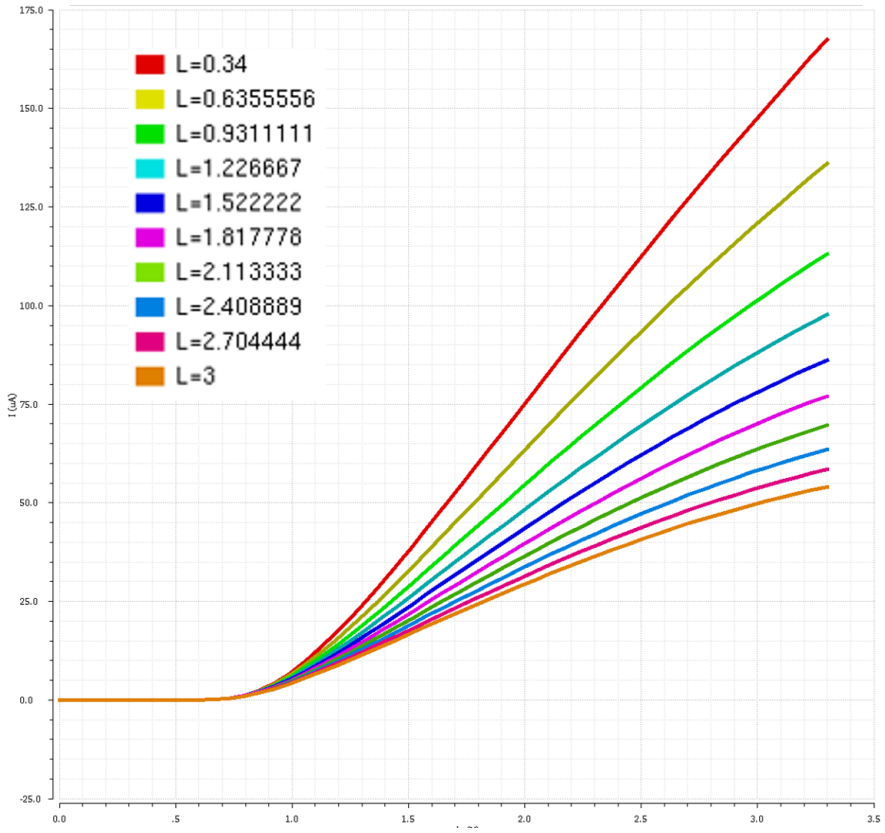


Figure B.4: Varying the length of the transistor creates a longer channel on the transistors. As a result, the electrons have to travel a longer distance to reach the other side. This increases the impedance of the device, decreasing the amount of current that can flow.

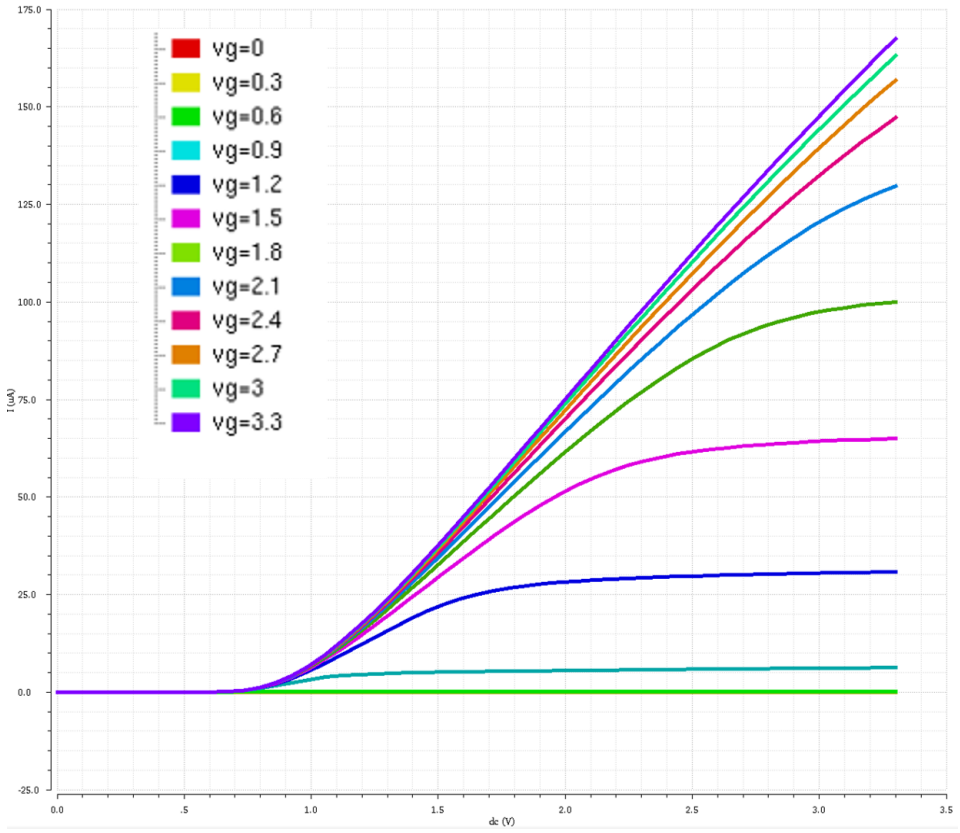


Figure B.5: Varying the voltage at the gate (V_g) of the MOS transistor puts it in different modes of operation. In the linear region, the MOS acts as a resistor and the value of equivalent resistance changes depending on the value of V_g

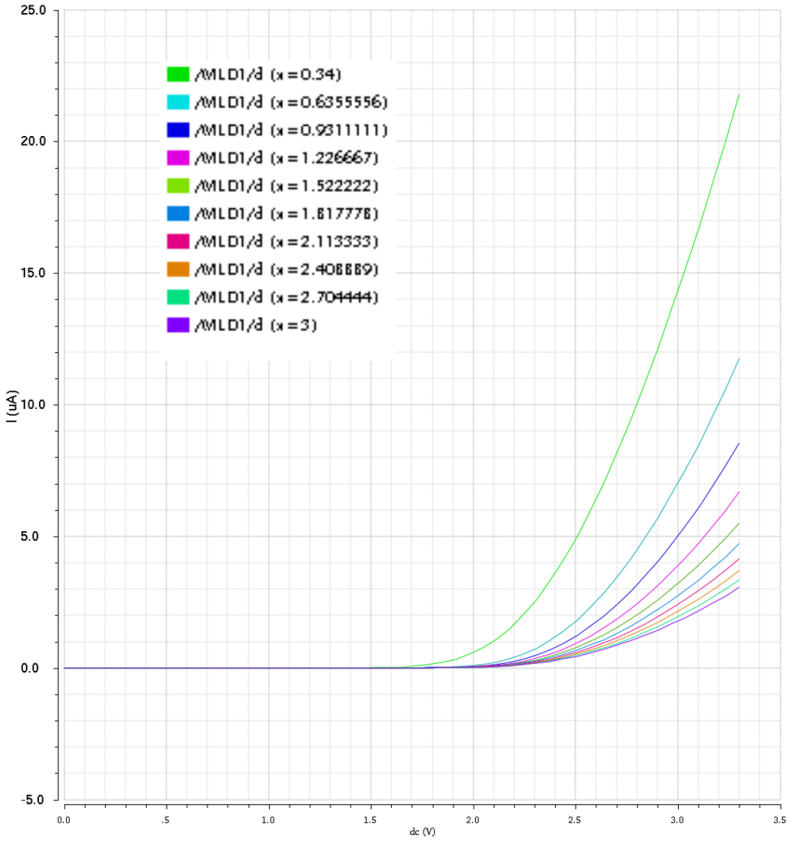


Figure B.6: Varying the length of the PMOS transistor yields very high apparent resistance, but the threshold voltage for the path increases significantly. For this reason, further investigations into using a PMOS device as a resistor have been dropped.

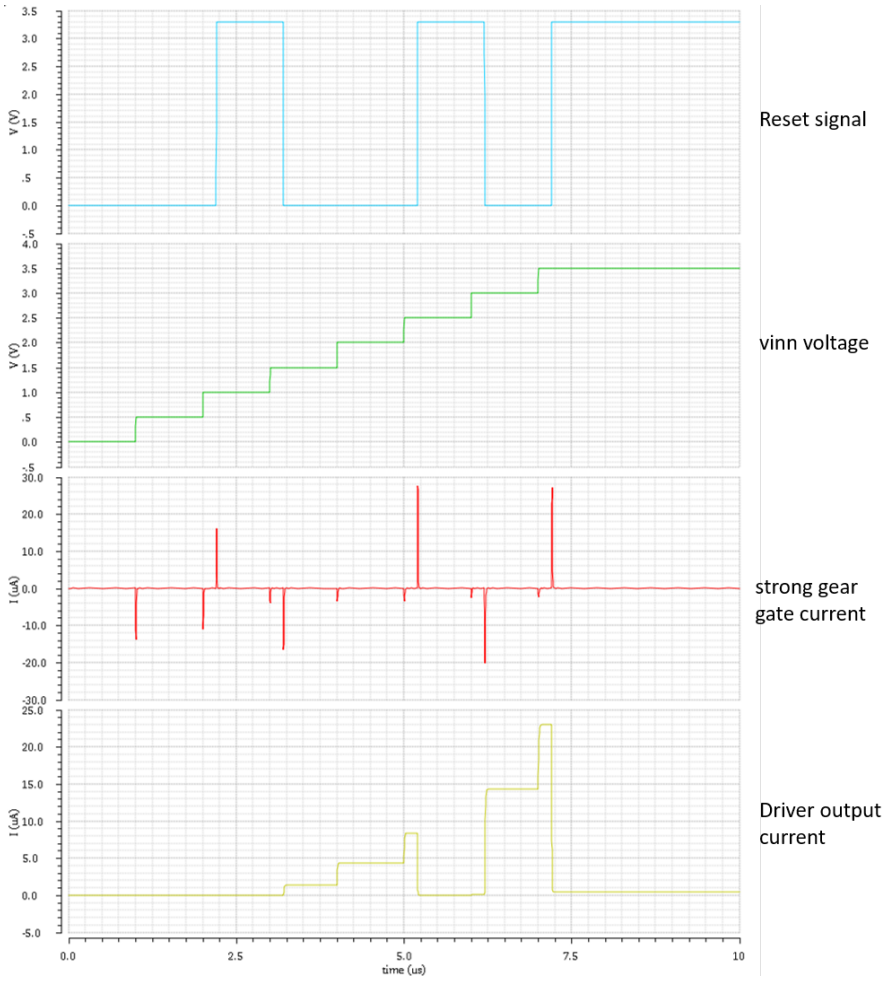


Figure B.7: Simulation that shows the effect of the reset line on the drive circuit.

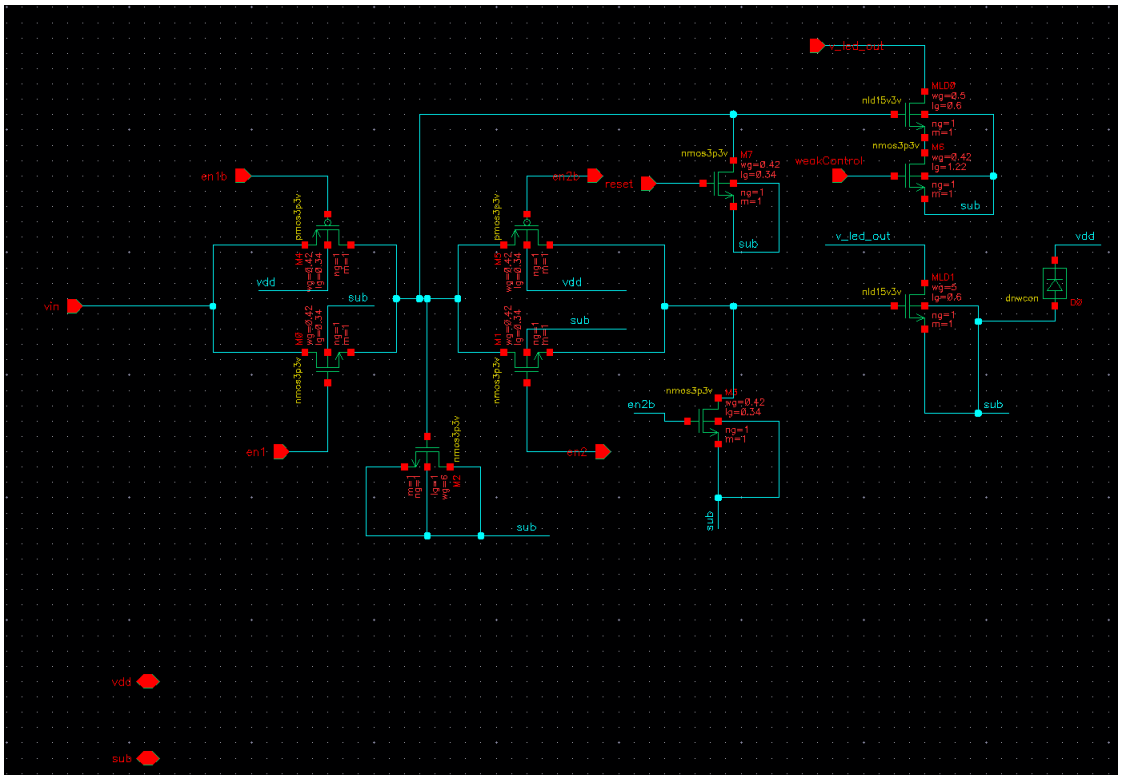


Figure B.8: Improved drive circuit with a reset line and a weak gear with a series NMOS connected.

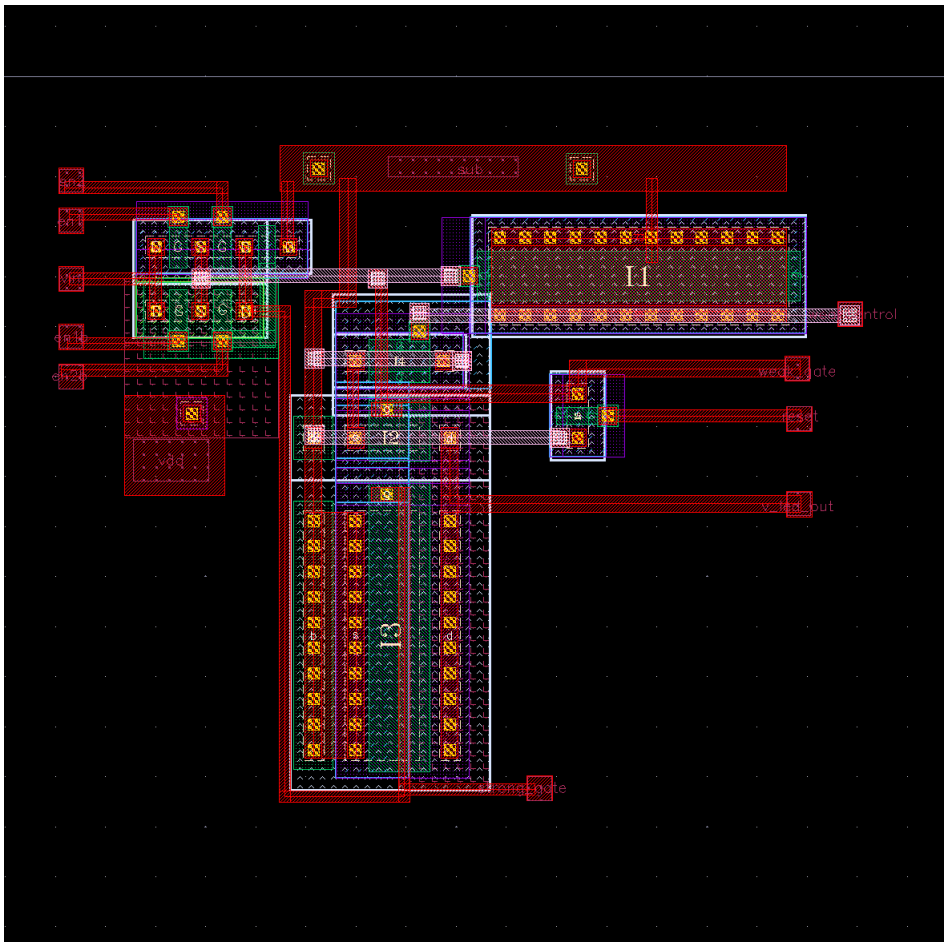


Figure B.9: Improved drive circuit layout for the ART-IDEA pixel.

Appendix C

FINAL TEST CHIP CIRCUIT LAYOUTS

The information here is supporting material for section 5.8. All of the circuits fabricated on the first ART-IDEA prototype chip are presented.

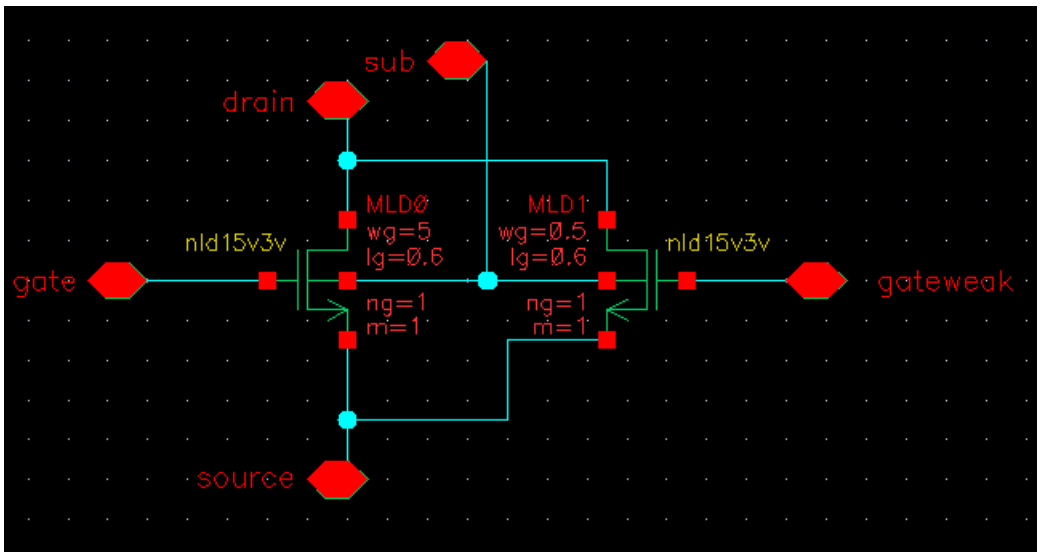


Figure C.1: NLDMOS drive transistors, left: large transistor, right: small transistor.

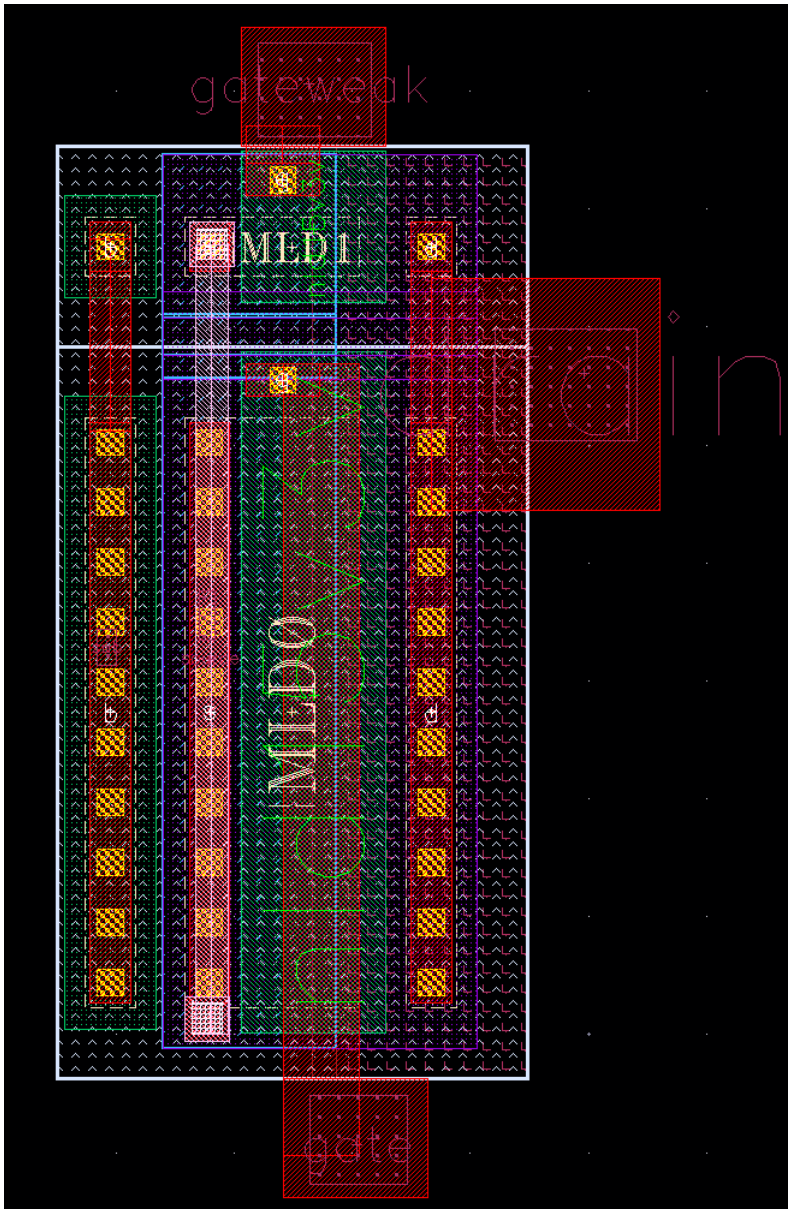


Figure C.2: NLDMOS drive transistor layout. Top portion is the weak gear and bottom portion is the strong gear.

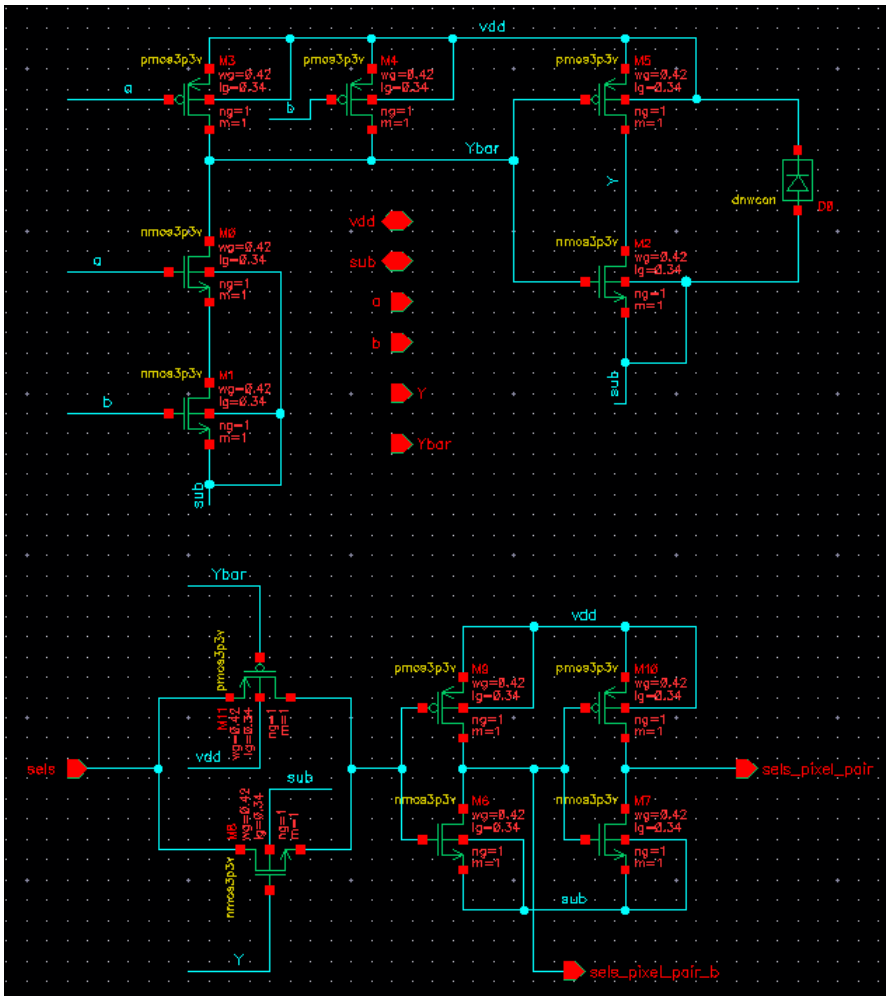


Figure C.3: Address decoder circuit and gear selector combined into one block on the test chip.

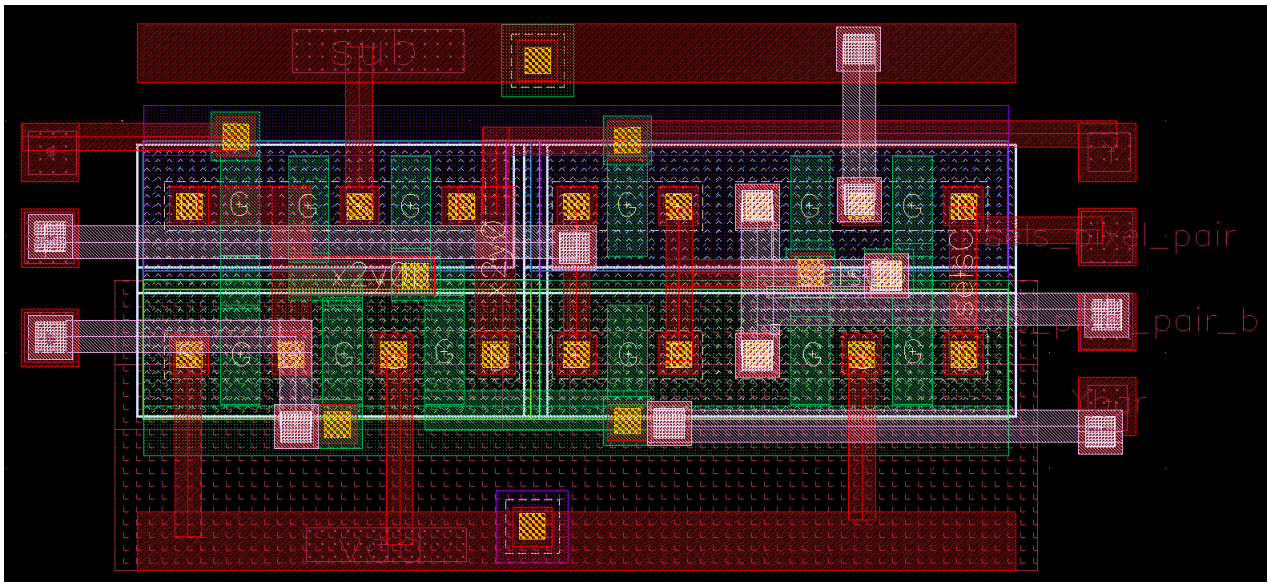


Figure C.4: Layout block for the address decoder and gear selector circuit.

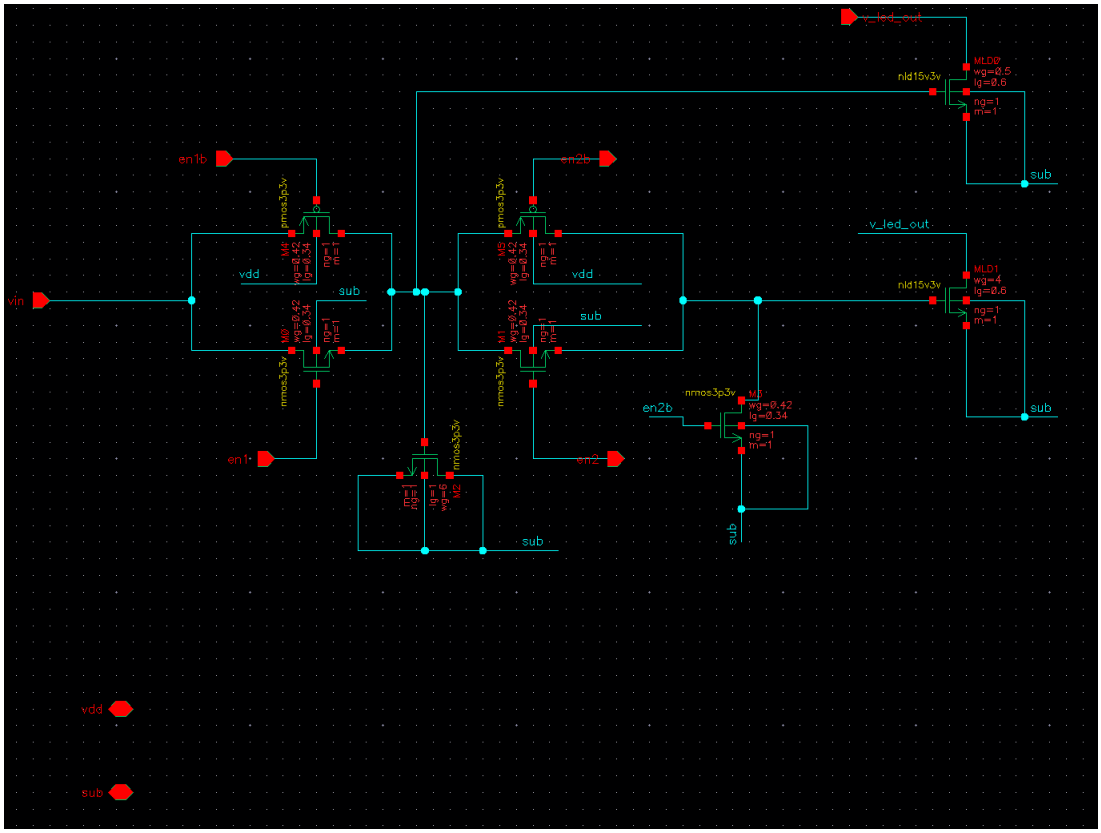


Figure C.5: Circuit schematic for the LED driver. This version has been used on previous RIICs.

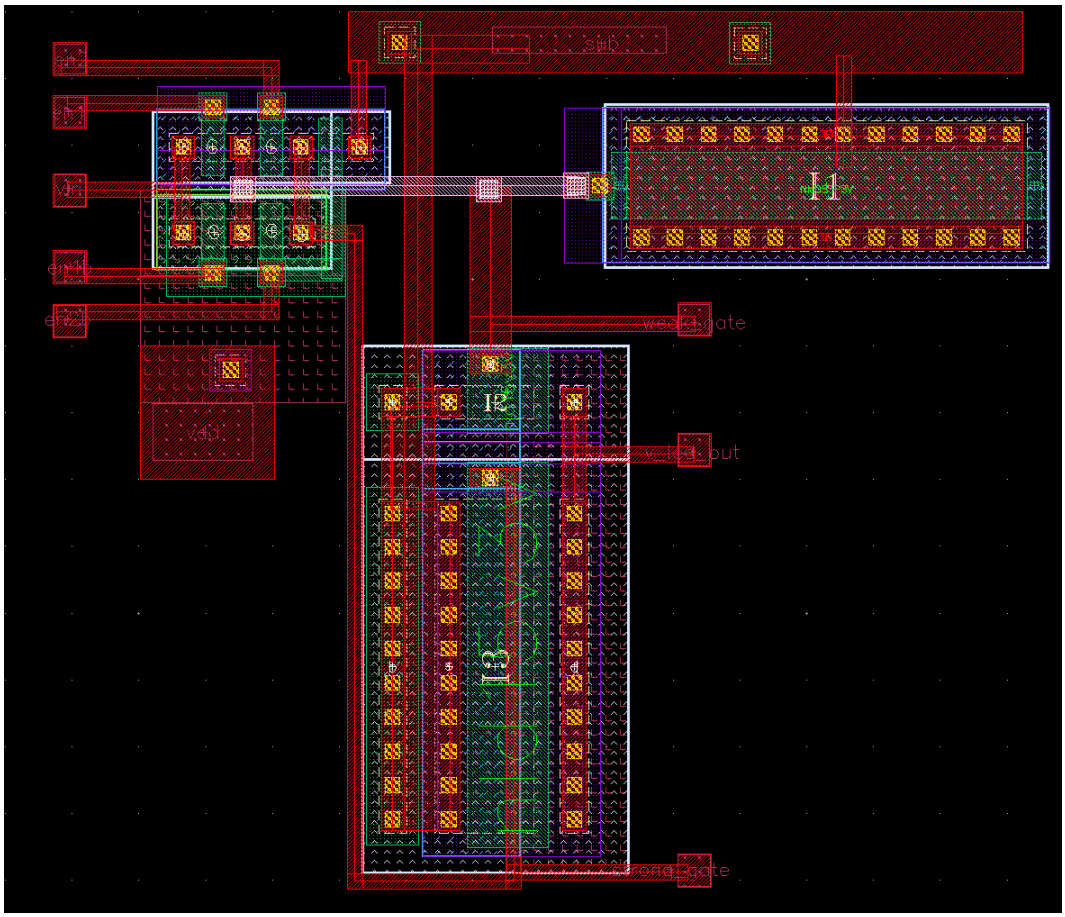


Figure C.6: Layout for the drive circuit shown in figure C.5

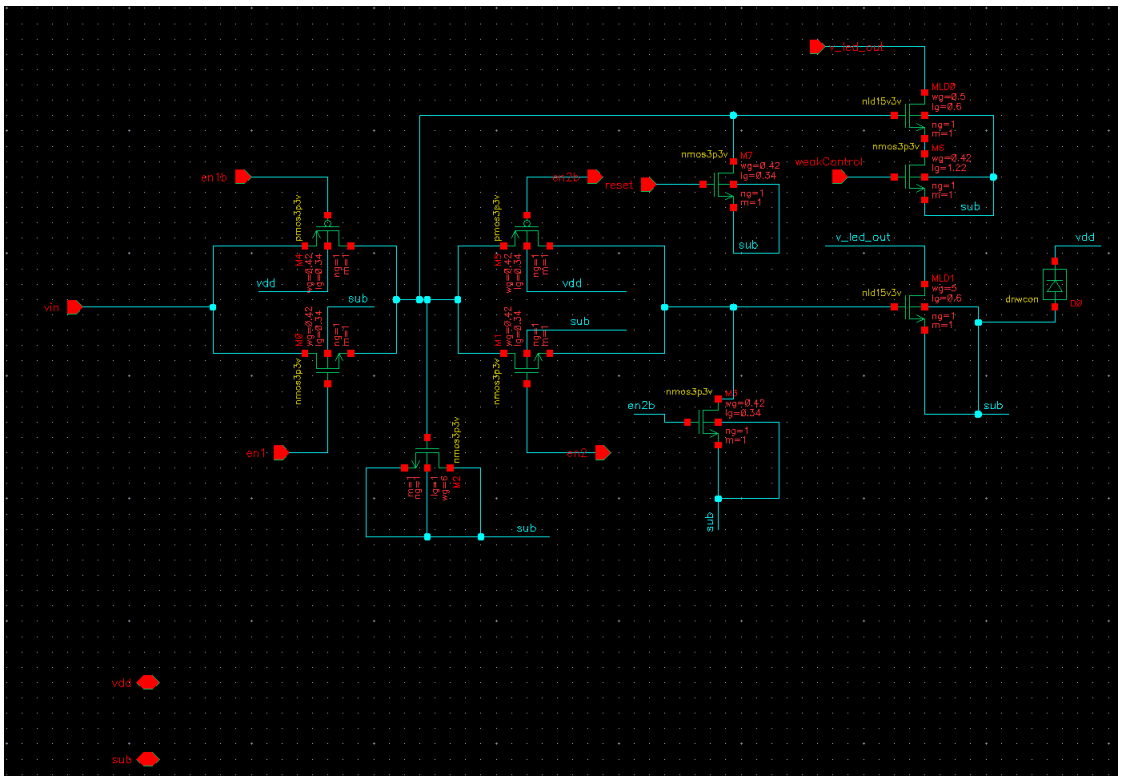


Figure C.7: Circuit schematic for the enhanced drive circuit. This circuit has been derived after many simulations. It contains a pixel-level reset line and a properly sized weak gear with a NMOS in series. If it proves to be effective after testing, it will be implemented in the main design and replace the current drive circuit.

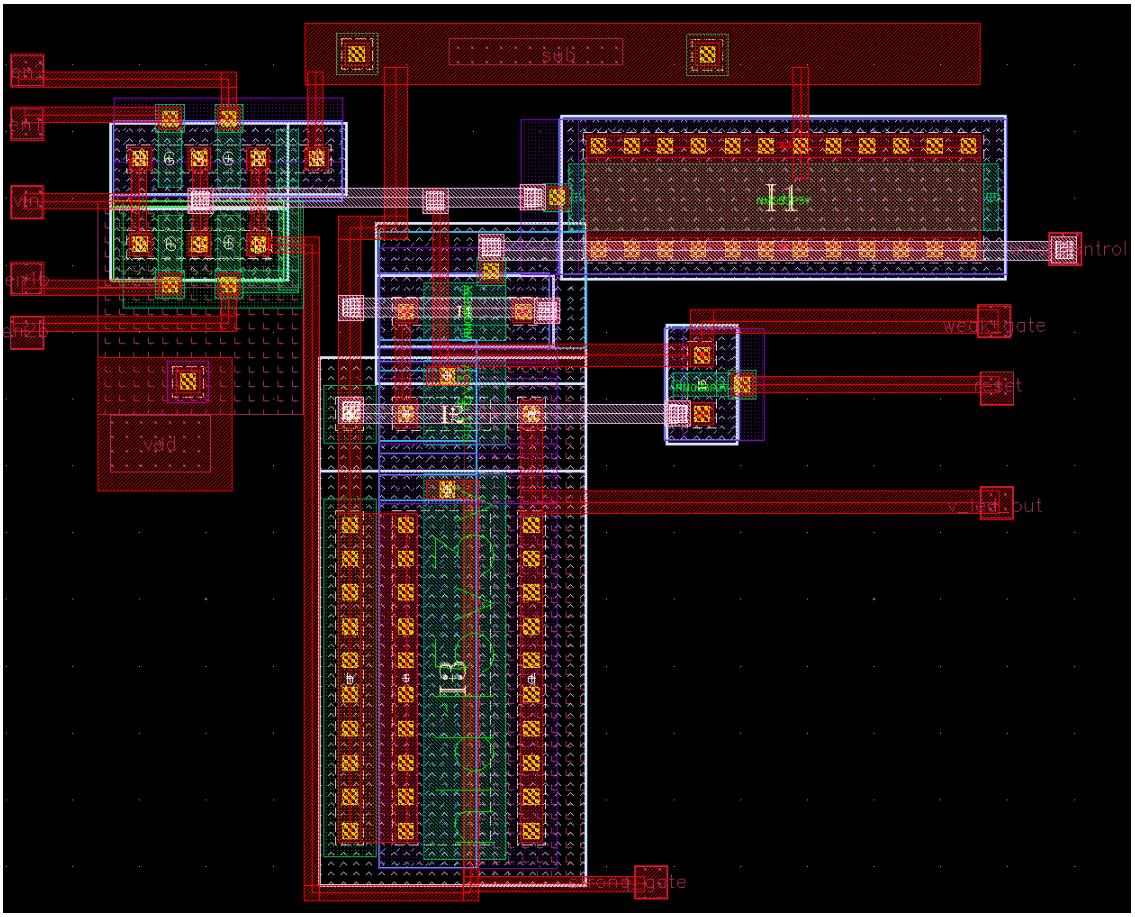


Figure C.8: This is the layout that corresponds to the driver schematic with a reset line and weak gear with an NMOS in series shown in figure C.7

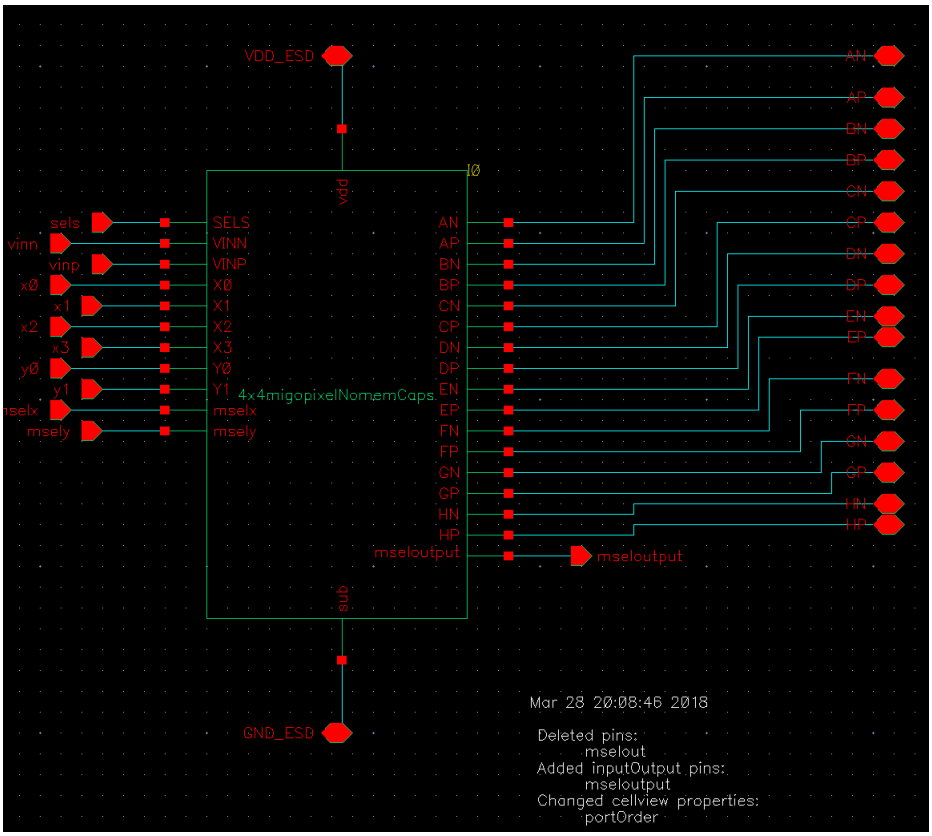


Figure C.9: This is the top cell schematic for the 4x4 RIIC super-pixel. Inputs are on the left side, and all 16 LED outputs plus the telemetry pin are on the right side

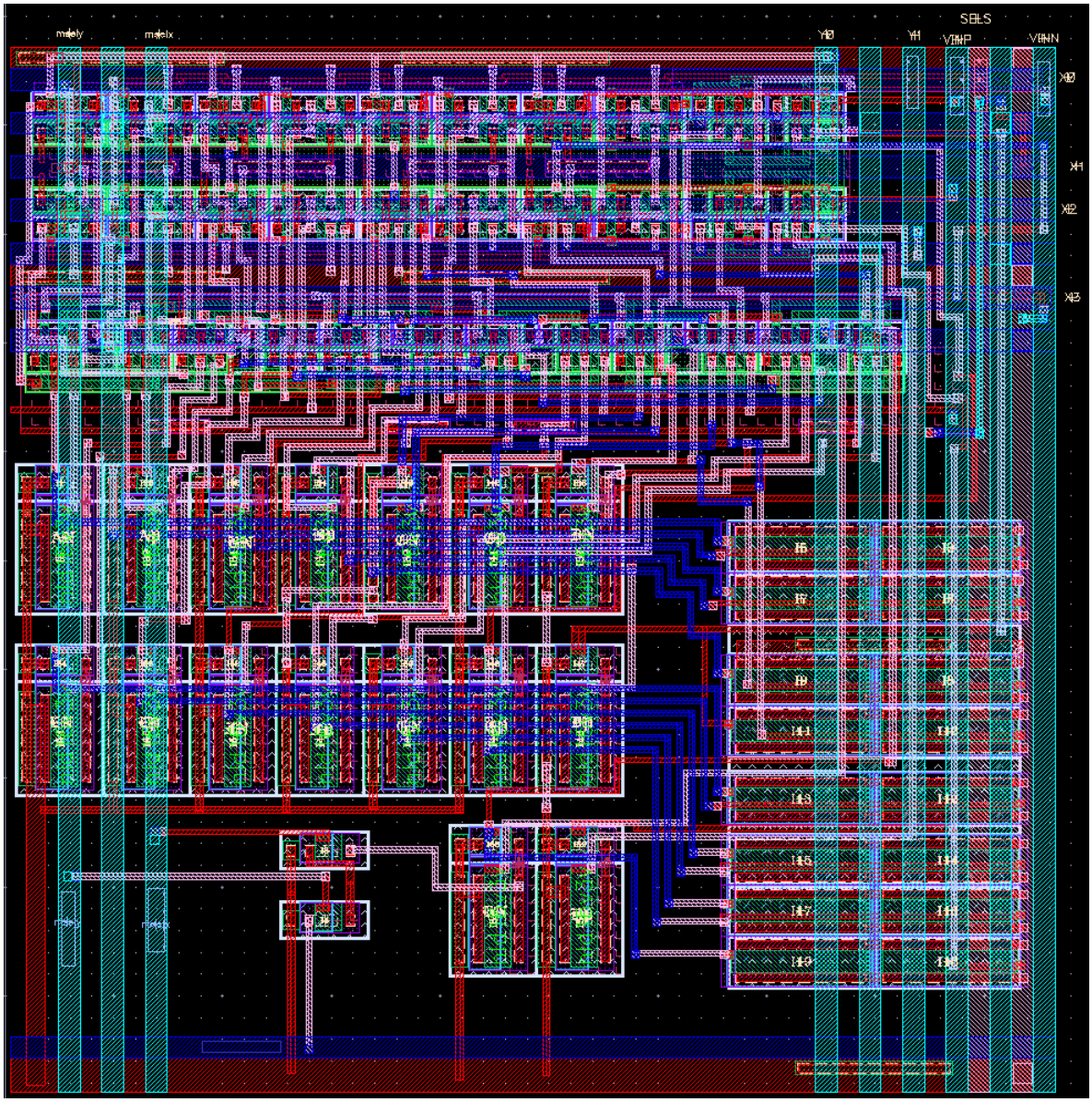


Figure C.10: Layout for the 4x4 RIIC super-pixel submitted for fabrication after passing DRC, LVS and post-PEX simulation tests.

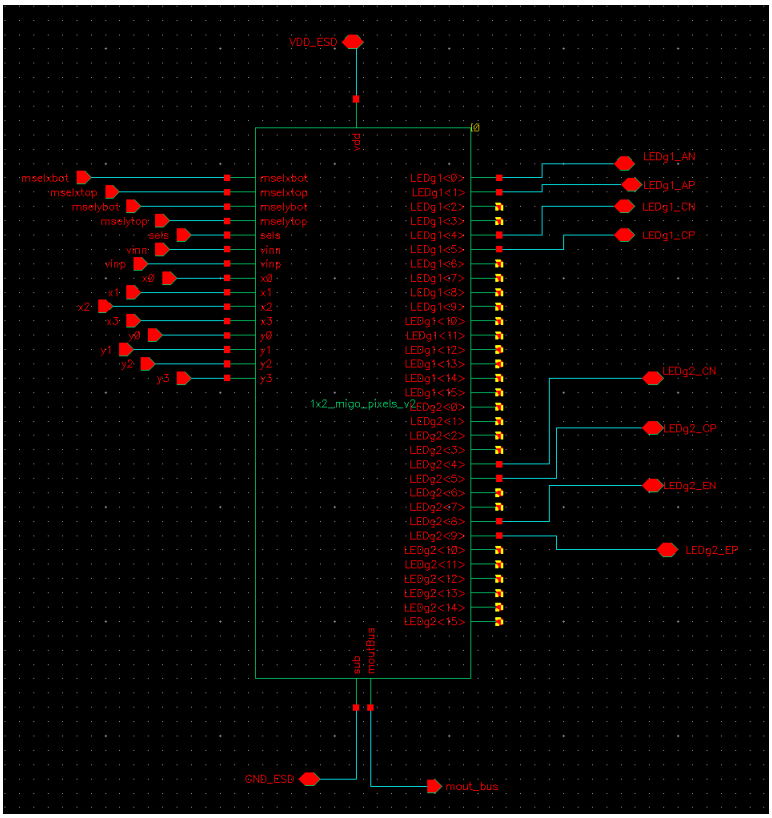


Figure C.11: Top cell for a two-tiled ART-IDEA super-pixels, a total of 32 pixel can be driven with this design.

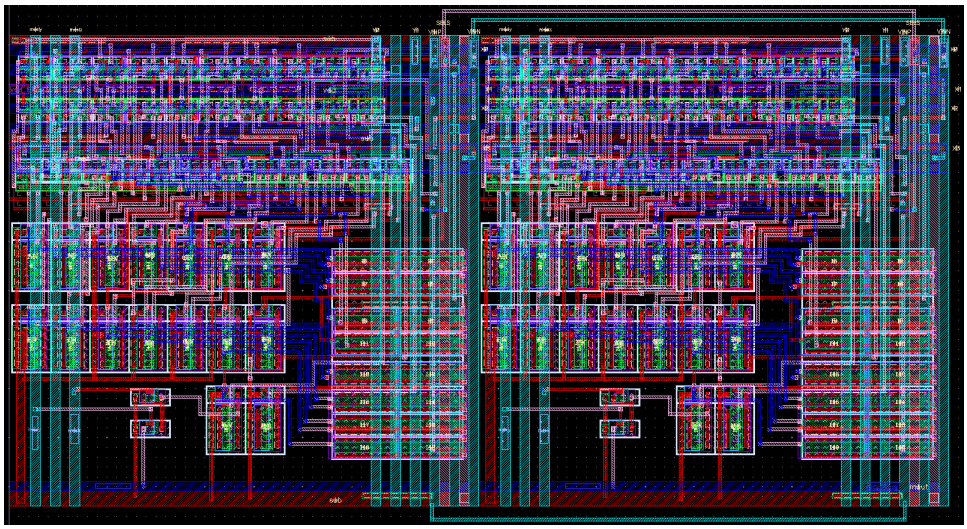


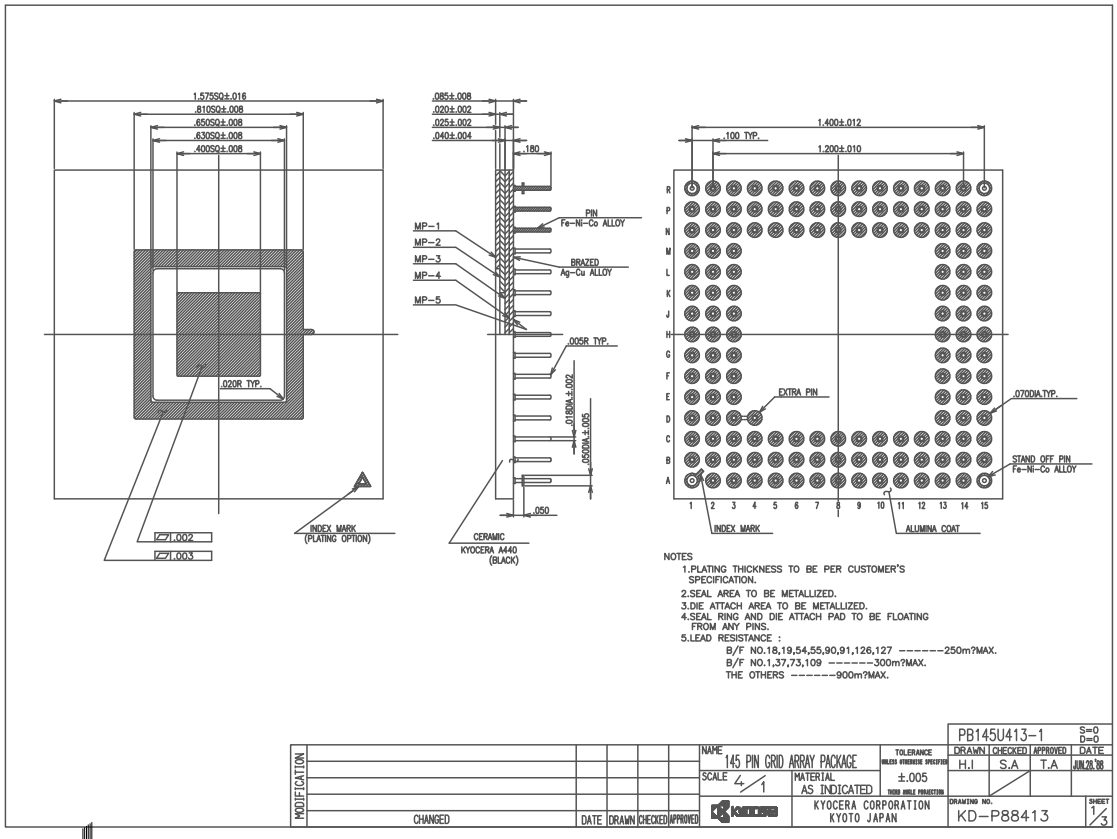
Figure C.12: Layout of two-tiled ART-IDEA super-pixels. This has been done to prove that the design is easily scalable.

Appendix D

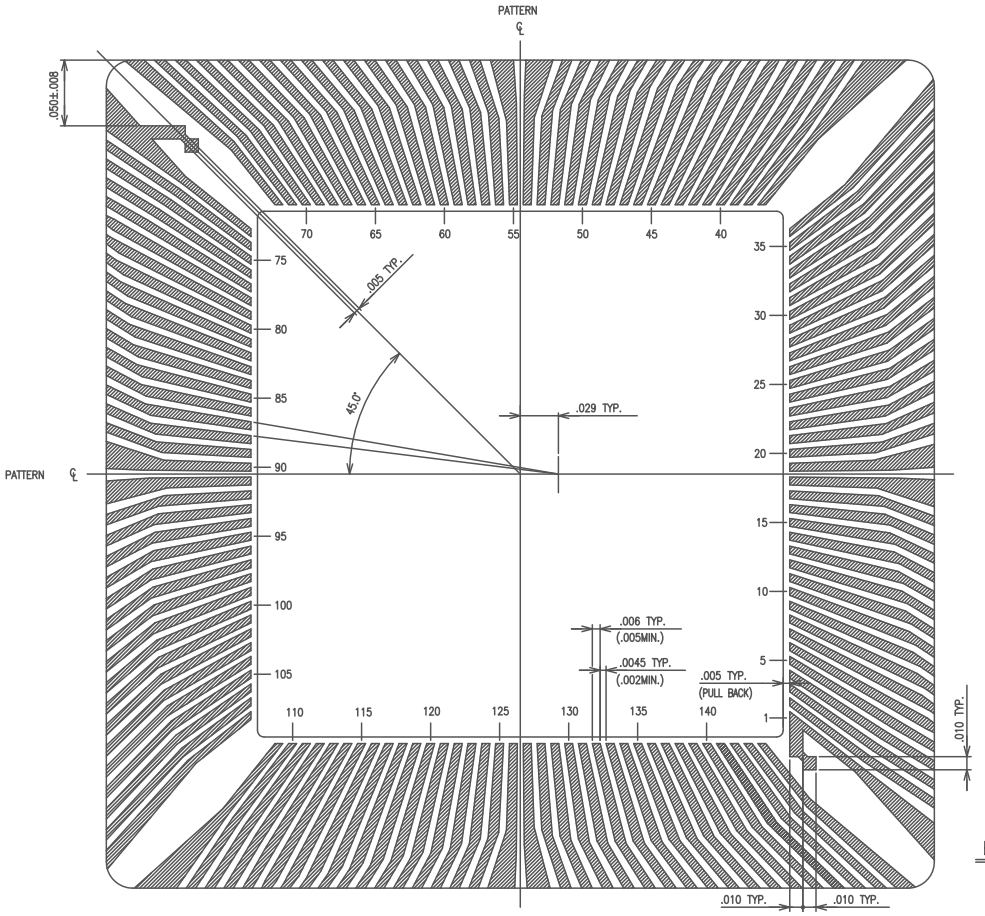
RIIC SUPER-PIXEL PACKAGING

Packaging diagrams shown in this appendix are being used with permission by Steve Ochoa, president of Spectrum Semiconductor Materials, Inc.

SSM P/N CPG14453



SSM P/N CPG14453



BONDING PATTERN

MODIFICATION						NAME	TOLERANCE	DRAWN	CHECKED	APPROVED	DATE
						145 PIN GRID ARRAY PACKAGE	UNLESS OTHERWISE SPECIFIED	H.I	S.A	T.A	JUN.28.'88
						SCALE 20/1	MATERIAL				
	CHANGED	DATE	DRAWN	CHECKED	APPROVED	KYOCERA	KYOCERA CORPORATION KYOTO JAPAN	DRAWING NO. KD-P88413			SHEET 2/3

SSM P/N CPG14453

WIRE BOND PAD / CONNECTOR PIN INTERCONNECTION PLA N

W/B NO.	PIN NO.
1	D3
2	C2
3	B1
4	D2
5	E3
6	C1
7	E2
8	D1
9	F3
10	F2
11	E1
12	G2
13	G3
14	F1
15	G1
16	H2
17	H1
18	H3
19	J3
20	J1

W/B NO.	PIN NO.
21	K1
22	J2
23	K2
24	K3
25	L1
26	L2
27	M1
28	N1
29	M2
30	L3
31	N2
32	P1
33	M3
34	N3
35	P2
36	R1
37	N4
38	P3
39	R2
40	P4

W/B NO.	PIN NO.
41	N5
42	R3
43	P5
44	R4
45	N6
46	P6
47	R5
48	P7
49	N7
50	R6
51	R7
52	P8
53	R8
54	N8
55	N9
56	R9
57	R10
58	P9
59	P10
60	N10

W/B NO.	PIN NO.
61	R11
62	P11
63	R12
64	R13
65	P12
66	N11
67	P13
68	R14
69	N12
70	N13
71	P14
72	R15
73	M13
74	N14
75	P15
76	M14
77	L13
78	N15
79	L14
80	M15

W/B NO.	PIN NO.
81	K13
82	K14
83	L15
84	J14
85	J13
86	K15
87	J15
88	H14
89	H15
90	H13
91	G13
92	G15
93	F15
94	G14
95	F14
96	F13
97	E15
98	E14
99	D15
100	C15

W/B NO.	PIN NO.
101	D14
102	E13
103	C14
104	B15
105	D13
106	C13
107	B14
108	A15
109	C12
110	B13
111	A14
112	B12
113	C11
114	A13
115	B11
116	A12
117	C10
118	B10
119	A11
120	B9

W/B NO.	PIN NO.
121	C9
122	A10
123	A9
124	B8
125	A8
126	C8
127	C7
128	A7
129	A6
130	B7
131	B6
132	C6
133	A5
134	B5
135	A4
136	A3
137	B4
138	C5
139	B3
140	A2

W/B NO.	PIN NO.
141	C4
142	C3
143	B2
144	A1

D/A	NC
S/R	NC
EXTRA PIN (D4)	D3

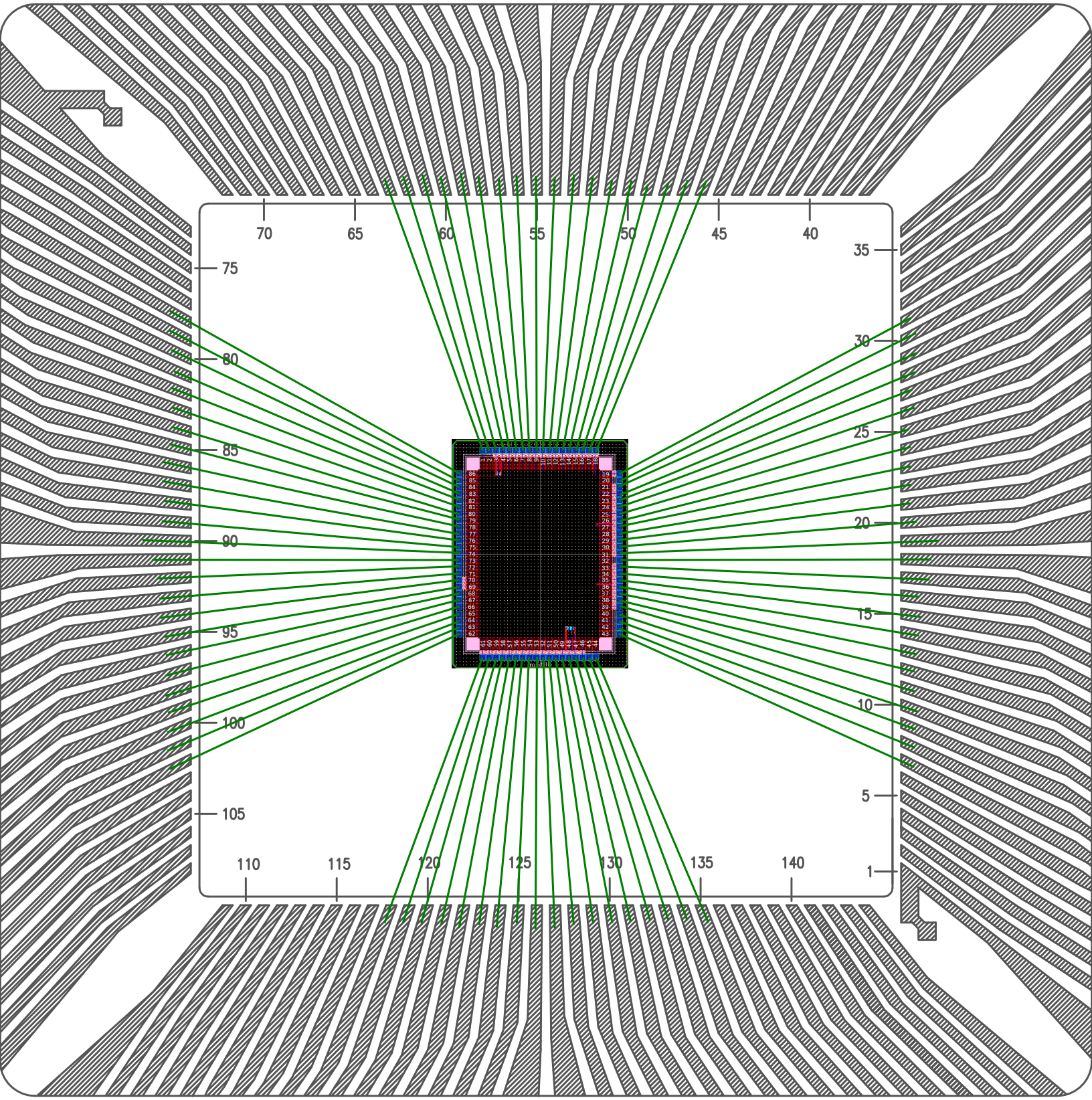
MODIFICATION	CHANGED	DATE	DRAWN	CHECKED	APPROVED

NAME: 145 PIN GRID ARRAY PACKAGE
SCALE: ×
MATERIAL:
TOLERANCE:

KYOCERA CORPORATION
KYOTO JAPAN

DRAWN	CHECKED	APPROVED	DATE
H.I	S.A	T.A	JUN.28.'88

DRAWING NO. KD-P88413
SHEET 3/3


70
65
60
55
50
45
40
35
75
30
80
25
85
20
90
15
95
10
100
5
105
1
110
115
120
125
130
135
140

chipCircuit	Signal Name	type	pin Count	pad number	PGA pin
4x4 super-pixel	GND_ESD	power gnd	1	T0	63
4x4 super-pixel	VDD_ESD	power vdd(3.3V)	2	T1	62
4x4 super-pixel	sels	signal input	3	T2	61
4x4 super-pixel	vinn	signal input	4	T3	60
4x4 super-pixel	vinp	signal input	5	T4	59
4x4 super-pixel	x0	signal input	6	T5	58
4x4 super-pixel	x1	signal input	7	T6	57
4x4 super-pixel	x2	signal input	8	T7	56
4x4 super-pixel	x3	signal input	9	T8	55
4x4 super-pixel	y0	signal input	10	T9	54
4x4 super-pixel	y1	signal input	11	T10	53
4x4 super-pixel	mselx	signal input	12	T11	52
4x4 super-pixel	msely	signal input	13	T12	51
4x4 super-pixel	mseloutput	signal output	14	T13	50
Driver Circuit	en1b	signal input	15	T14	49
Driver Circuit	en1	signal input	16	T15	48
Driver Circuit	en2b	signal input	17	T16	47
Driver Circuit	en2	signal input	18	T17	46
Driver Circuit	vin	signal input	19	R0	31
Driver Circuit	led_out	signal output (LED)	20	R1	30
Driver Circuit	weak_gate	signal input	21	R2	29
Driver Circuit	strong_gate	signal input	22	R3	28
Driver Circuit with Weak control	en1b	signal input	23	R4	27
Driver Circuit with Weak control	en1	signal input	24	R5	26
Driver Circuit with Weak control	en2b	signal input	25	R6	25
Driver Circuit with Weak control	en2	signal input	26	R7	24
Driver Circuit with Weak control	reset	signal input	27	R8	23
Driver Circuit with Weak control	vin	signal input	28	R9	22
Driver Circuit with Weak control	weakControl	signal input	29	R10	21
Driver Circuit with Weak control	strong_gate	signal input	30	R11	20
Driver Circuit with Weak control	weak_gate	signal input	31	R12	19
Driver Circuit with Weak control	led_out	signal output(LED)	32	R13	18
adress decoder	a	signal input	33	R14	17
adress decoder	b	signal input	34	R15	16
adress decoder	sels	signal input	35	R16	15
adress decoder	Y	signal input	36	R17	14
adress decoder	Ybar	signal input	37	R18	13
adress decoder	sels_px_pair	signal input	38	R19	12
adress decoder	sels_px_pairb	signal input	39	R20	11
tiled super-pixel	LEDg_CP	power	40	R21	10
tiled super-pixel	LEDg1_CN	power	41	R22	9
tiled super-pixel	LEDg1_AP	power	42	R23	8
tiled super-pixel	LEDg1_AN	power	43	R24	7

tiled super-pixel	GND_ESD	power	44	B0	135
tiled super-pixel	VDD_ESD	power(only bottom)	45	B1	134
tiled super-pixel	sels	signal input	46	B2	133
tiled super-pixel	vinn	signal input	47	B3	132
tiled super-pixel	vinp	signal input	48	B4	131
tiled super-pixel	x0	signal input	49	B5	130
tiled super-pixel	x1	signal input	50	B6	129
tiled super-pixel	x2	signal input	51	B7	128
tiled super-pixel	x3	signal input	52	B8	127
tiled super-pixel	y0	signal input	53	B9	126
tiled super-pixel	y1	signal input	54	B10	125
tiled super-pixel	y2	signal input	55	B11	124
tiled super-pixel	y3	signal input	56	B12	123
tiled super-pixel	mselxtop	signal input	57	B13	122
tiled super-pixel	mselytop	signal input	58	B14	121
tiled super-pixel	mselxbot	signal input	59	B15	120
tiled super-pixel	mselybot	signal input	60	B16	119
tiled super-pixel	mout_bus	output	61	B17	118
tiled super-pixel	LEDg2_EN	signal input	62	L0	102
tiled super-pixel	LEDg2_EP	signal input	63	L1	101
tiled super-pixel	LEDg2_CN	signal input	64	L2	100
tiled super-pixel	LEDg2_CP	signal input	65	L3	99
null	null	null	66	L4	98
drive transistors	drain	power/output	67	L5	97
drive transistors	source	power	68	L6	96
drive transistors	strong_gate	signal_input	69	L7	95
drive transistors	weak_gate	signal input	70	L8	94
4x4 super-pixel	HP	power/output	71	L9	93
4x4 super-pixel	HN	power/output	72	L10	92
4x4 super-pixel	GP	power/output	73	L11	91
4x4 super-pixel	GN	power/output	74	L12	90
4x4 super-pixel	FP	power/output	75	L13	89
4x4 super-pixel	FN	power/output	76	L14	88
4x4 super-pixel	EP	power/output	77	L15	87
4x4 super-pixel	EN	power/output	78	L16	86
4x4 super-pixel	DP	power/output	79	L17	85
4x4 super-pixel	DN	power/output	80	L18	84
4x4 super-pixel	CP	power/output	81	L19	83
4x4 super-pixel	CN	power/output	82	L20	82
4x4 super-pixel	BP	power/output	83	L21	81
4x4 super-pixel	BN	power/output	84	L22	80
4x4 super-pixel	AP	power/output	85	L23	79
4x4 super-pixel	AN	power/output	86	L24	78

Appendix E

PARTITIONED SVSM - 84-PIN LCC SOCKET

Packaging diagrams shown in this appendix are being used with permission by Steve Ochoa, president of Spectrum Semiconductor Materials, Inc.

The following lists correspond to all of the SLED devices brought out to the pins of the 84-pin LCC package. The lists are divided by quadrant number on the SLED wafer.

DIODevice SLEDSwitchV2-Q1 — SLEDSwitchV2-Q2 —SLEDSwitchV2-Q3 — SLEDSwitchV2-Q4

Quadrant 1:
Pitch = inf um, lane width = 0.0 um, effective pixel width = inf um

Line 74, 206x206um	206 x 206	81	81	81	40, 81
Line 75, 056x056um	056 x 056	81	81	81	44, 81
Line 76, 030x030um	030 x 030	81	81	81	48, 81
Line 77, 106x106um	106 x 106	81	81	81	52, 81
Line 78, 206x206um	206 x 206	81	81	81	56, 81
Line 79, 106x106um	106 x 106	81	81	81	60, 81
Line 80, 056x056um	056 x 056	81	81	81	64, 81
Line 81, 038x038um	038 x 038	81	81	81	68, 81
Line 82, 030x030um	030 x 030	81	81	81	72, 81
Line 83, 038x038um	038 x 038	81	81	81	76, 81
Cathode 84	x	81	81	81	80
Line 01, 030x030um	030 x 030	00, 81	81	81	81
Line 02, 038x038um	038 x 038	04, 81	81	81	81
Line 03, 106x106um	106 x 106	08, 81	81	81	81
Line 04, 038x038um	038 x 038	12, 81	81	81	81
Line 05, 206x206um	206 x 206	16, 81	81	81	81
Line 06, 056x056um	056 x 056	20, 81	81	81	81
Line 07, 030x030um	030 x 030	24, 81	81	81	81
Line 08, 106x106um	106 x 106	28, 81	81	81	81
Line 09, 206x206um	206 x 206	32, 81	81	81	81
Line 10, 406x406um	406 x 406	36, 81	81	81	81

==========

Quadrant 2:

Pitch = 12.0 um, lane width = 3.0 um, effective pixel width = 7.0 um

Line 11, 112x112um	112 x 112	40, 81	81	81	81
Line 12, 021x021um	021 x 021	44, 81	81	81	81
Line 13, 007x007um	007 x 007	48, 81	81	81	81
Line 14, 049x049um	049 x 049	52, 81	81	81	81
Line 15, 112x112um	112 x 112	56, 81	81	81	81
Line 16, 049x049um	049 x 049	60, 81	81	81	81
Line 17, 021x021um	021 x 021	64, 81	81	81	81
Line 18, 014x014um	014 x 014	68, 81	81	81	81
Line 19, 007x007um	007 x 007	72, 81	81	81	81
Line 20, 014x014um	014 x 014	76, 81	81	81	81
Cathode 21	x	80	81	81	81
Line 22, 007x007um	007 x 007	81	00, 81	81	81
Line 23, 014x014um	014 x 014	81	04, 81	81	81
Line 24, 049x049um	049 x 049	81	08, 81	81	81
Line 25, 014x014um	014 x 014	81	12, 81	81	81
Line 26, 112x112um	112 x 112	81	16, 81	81	81
Line 27, 021x021um	021 x 021	81	20, 81	81	81
Line 28, 007x007um	007 x 007	81	24, 81	81	81
Line 29, 049x049um	049 x 049	81	28, 81	81	81
Line 30, 112x112um	112 x 112	81	32, 81	81	81
Line 31, 224x224um	224 x 224	81	36, 81	81	81

==========

Quadrant 3:

Pitch = 18.0 um, lane width = 4.5 um, effective pixel width = 11.5 um

Line 32, 115x115um	115 x 115	81	40, 81	81	81
Line 33, 023x023um	023 x 023	81	44, 81	81	81
Line 34, 011x011um	011 x 011	81	48, 81	81	81
Line 35, 057x057um	057 x 057	81	52, 81	81	81
Line 36, 115x115um	115 x 115	81	56, 81	81	81
Line 37, 057x057um	057 x 057	81	60, 81	81	81
Line 38, 023x023um	023 x 023	81	64, 81	81	81
Line 39, 011x011um	011 x 011	81	68, 81	81	81
Line 40, 011x011um	011 x 011	81	72, 81	81	81
Line 41, 011x011um	011 x 011	81	76, 81	81	81
Cathode 42	x	81	80	81	81
Line 43, 011x011um	011 x 011	81	81	00, 81	81
Line 44, 011x011um	011 x 011	81	81	04, 81	81
Line 45, 057x057um	057 x 057	81	81	08, 81	81
Line 46, 011x011um	011 x 011	81	81	12, 81	81
Line 47, 115x115um	115 x 115	81	81	16, 81	81
Line 48, 023x023um	023 x 023	81	81	20, 81	81
Line 49, 011x011um	011 x 011	81	81	24, 81	81
Line 50, 057x057um	057 x 057	81	81	28, 81	81
Line 51, 115x115um	115 x 115	81	81	32, 81	81
Line 52, 241x241um	241 x 241	81	81	36, 81	81

==========

Quadrant 4:

Pitch = 24.0 um, lane width = 6.0 um, effective pixel width = 16.0 um

Line 53, 128x128um	128 x 128	81	81	40, 81	81
Line 54, 032x032um	032 x 032	81	81	44, 81	81
Line 55, 016x016um	016 x 016	81	81	48, 81	81
Line 56, 064x064um	064 x 064	81	81	52, 81	81
Line 57, 128x128um	128 x 128	81	81	56, 81	81
Line 58, 064x064um	064 x 064	81	81	60, 81	81
Line 59, 032x032um	032 x 032	81	81	64, 81	81
Line 60, 016x016um	016 x 016	81	81	68, 81	81
Line 61, 016x016um	016 x 016	81	81	72, 81	81
Line 62, 016x016um	016 x 016	81	81	76, 81	81
Cathode 63	x	81	81	80	81
Line 64, 016x016um	016 x 016	81	81	81	00, 81
Line 65, 016x016um	016 x 016	81	81	81	04, 81
Line 66, 064x064um	064 x 064	81	81	81	08, 81
Line 67, 016x016um	016 x 016	81	81	81	12, 81
Line 68, 128x128um	128 x 128	81	81	81	16, 81
Line 69, 032x032um	032 x 032	81	81	81	20, 81
Line 70, 016x016um	016 x 016	81	81	81	24, 81
Line 71, 064x064um	064 x 064	81	81	81	28, 81
Line 72, 128x128um	128 x 128	81	81	81	32, 81
Line 73, 256x256um	256 x 256	81	81	81	36, 81

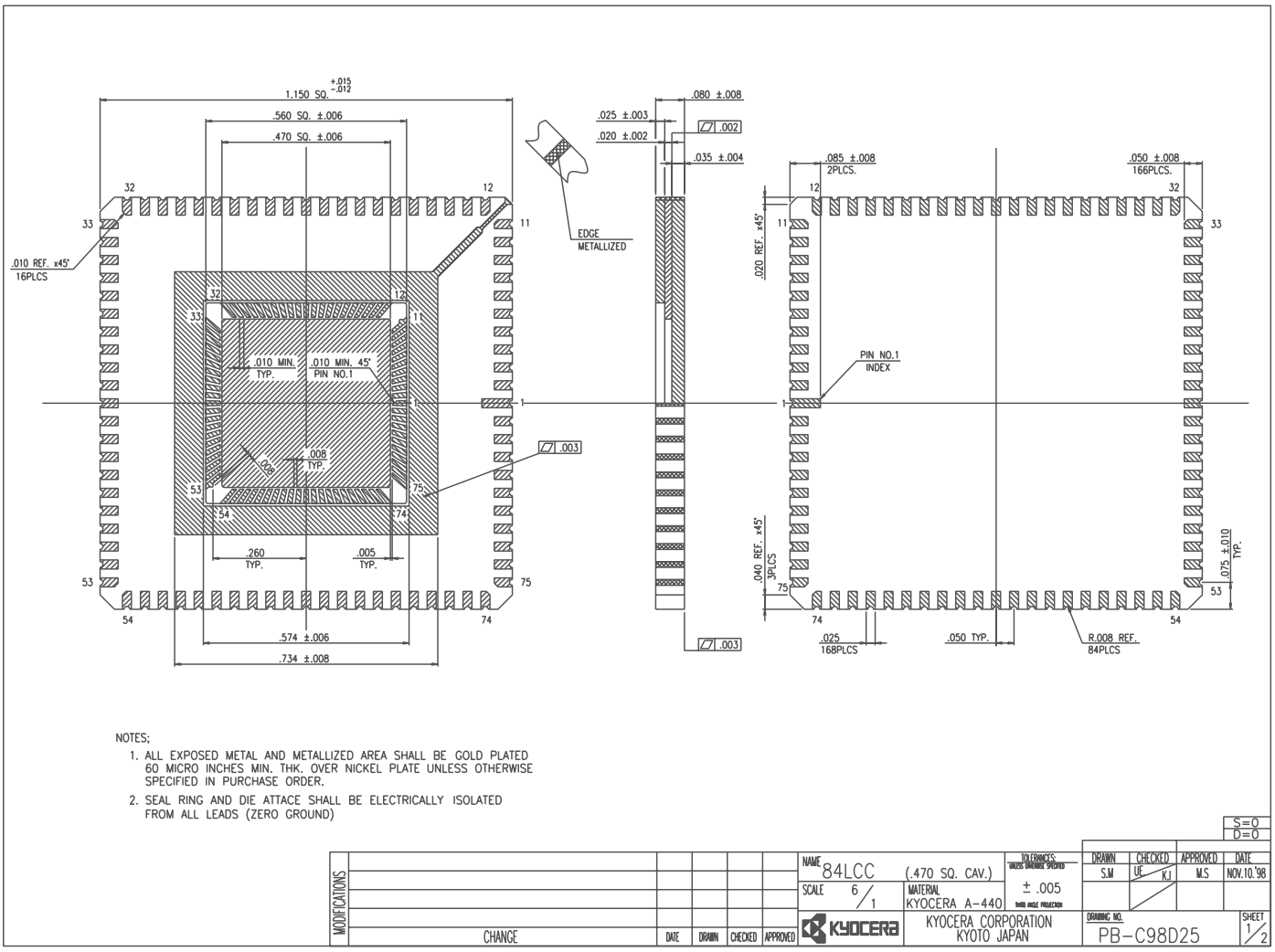
Continuity and cathode checks

Open — — — — —

Open with cathodes — — 81 — 81 — 81 — 81

Cathode 42 short — — — 80, 81 — —

SSM P/N LCC08422



NOTES;

1. ALL EXPOSED METAL AND METALLIZED AREA SHALL BE GOLD PLATED 60 MICRO INCHES MIN. THK. OVER NICKEL PLATE UNLESS OTHERWISE SPECIFIED IN PURCHASE ORDER.
2. SEAL RING AND DIE ATTACE SHALL BE ELECTRICALLY ISOLATED FROM ALL LEADS (ZERO GROUND)

S=0
D=0

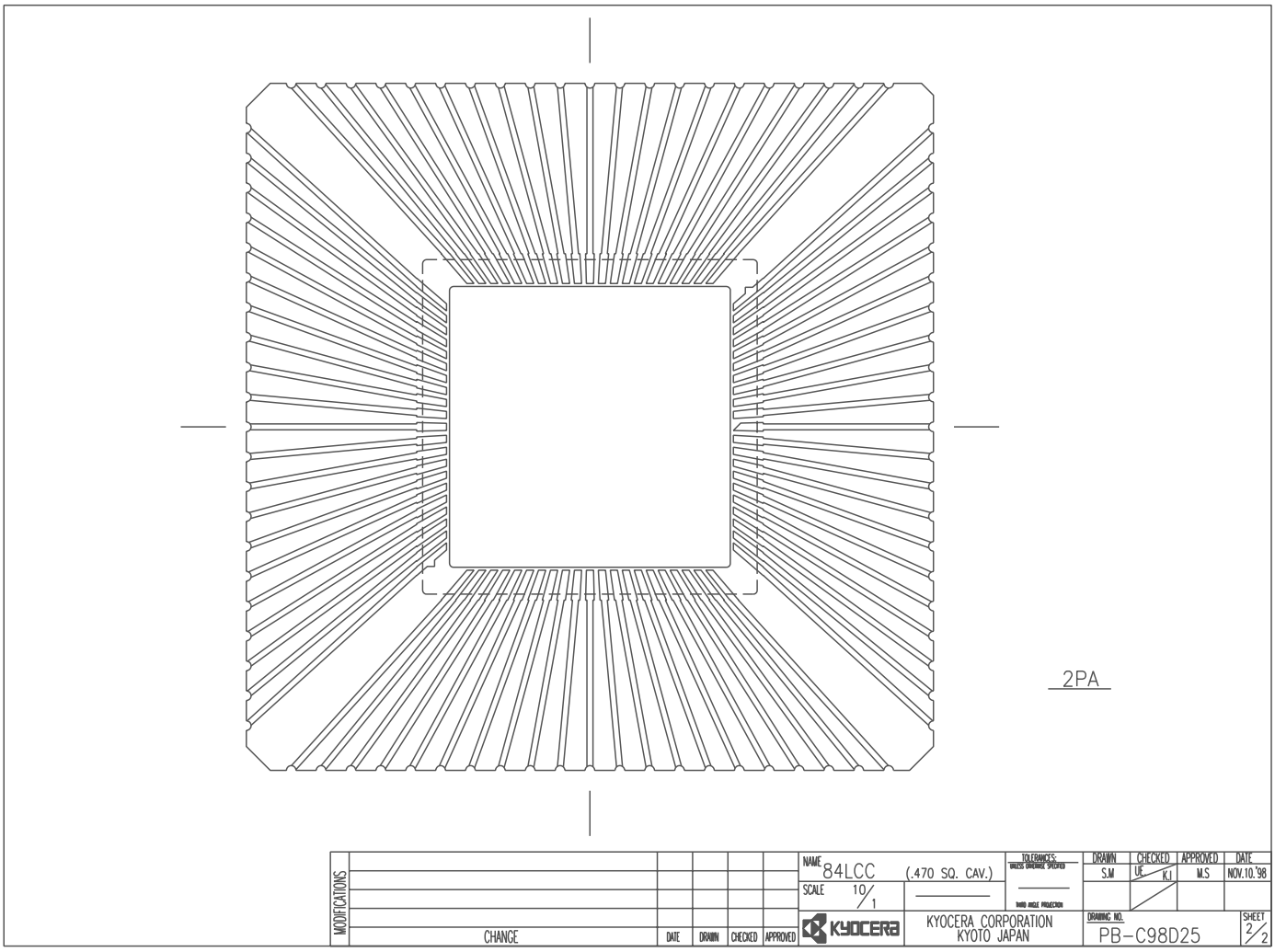
MODIFICATIONS	CHANGE	DATE	DRAWN	CHECKED	APPROVED

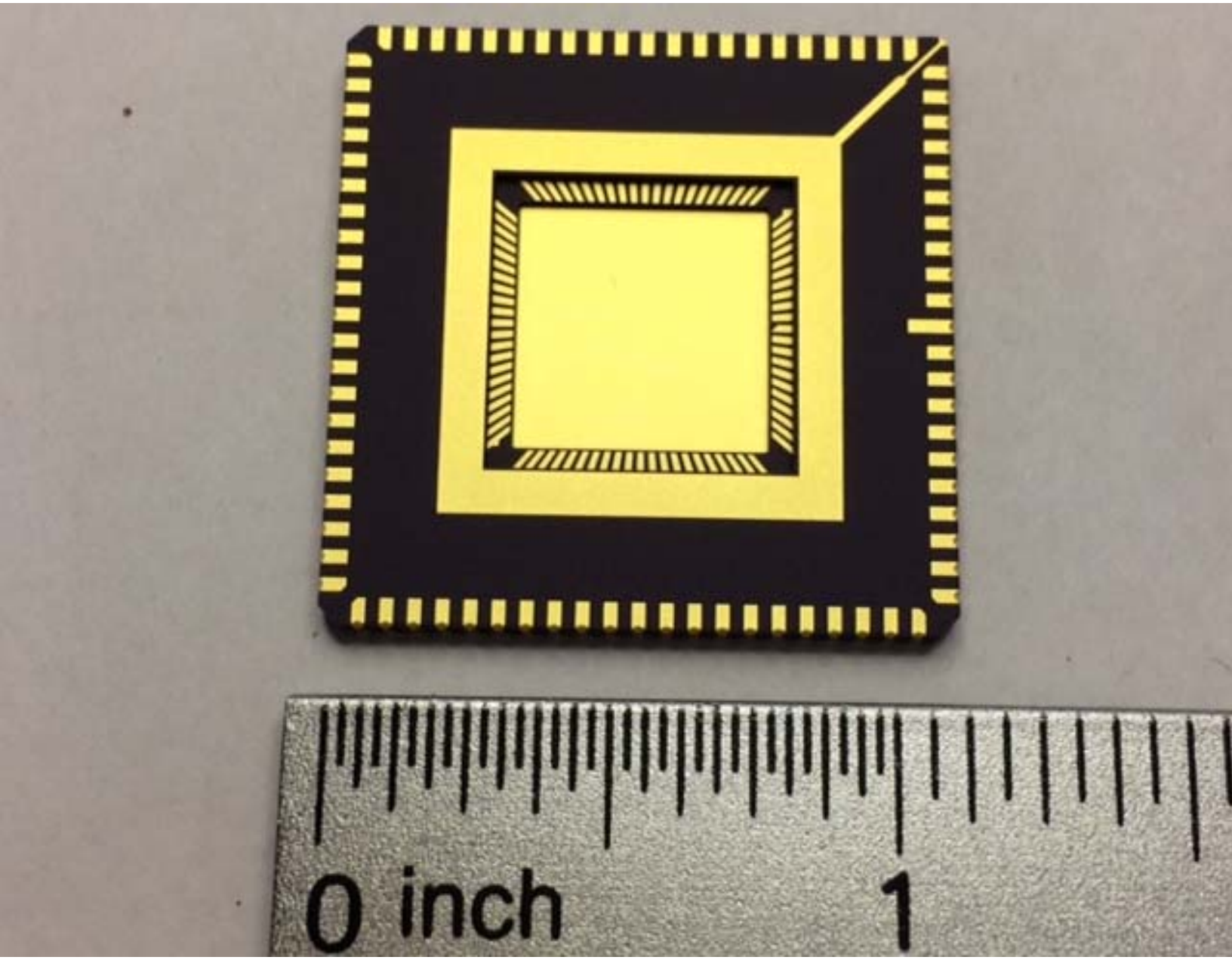
NAME 84LCC (.470 SQ. CAV.)
SCALE 6/1
MATERIAL KYOCERA A-440
TOLERANCES: UNLESS OTHERWISE SPECIFIED ± .005 THIRD ANGLE PROJECTION
KYOCERA
KYOCERA CORPORATION KYOTO JAPAN

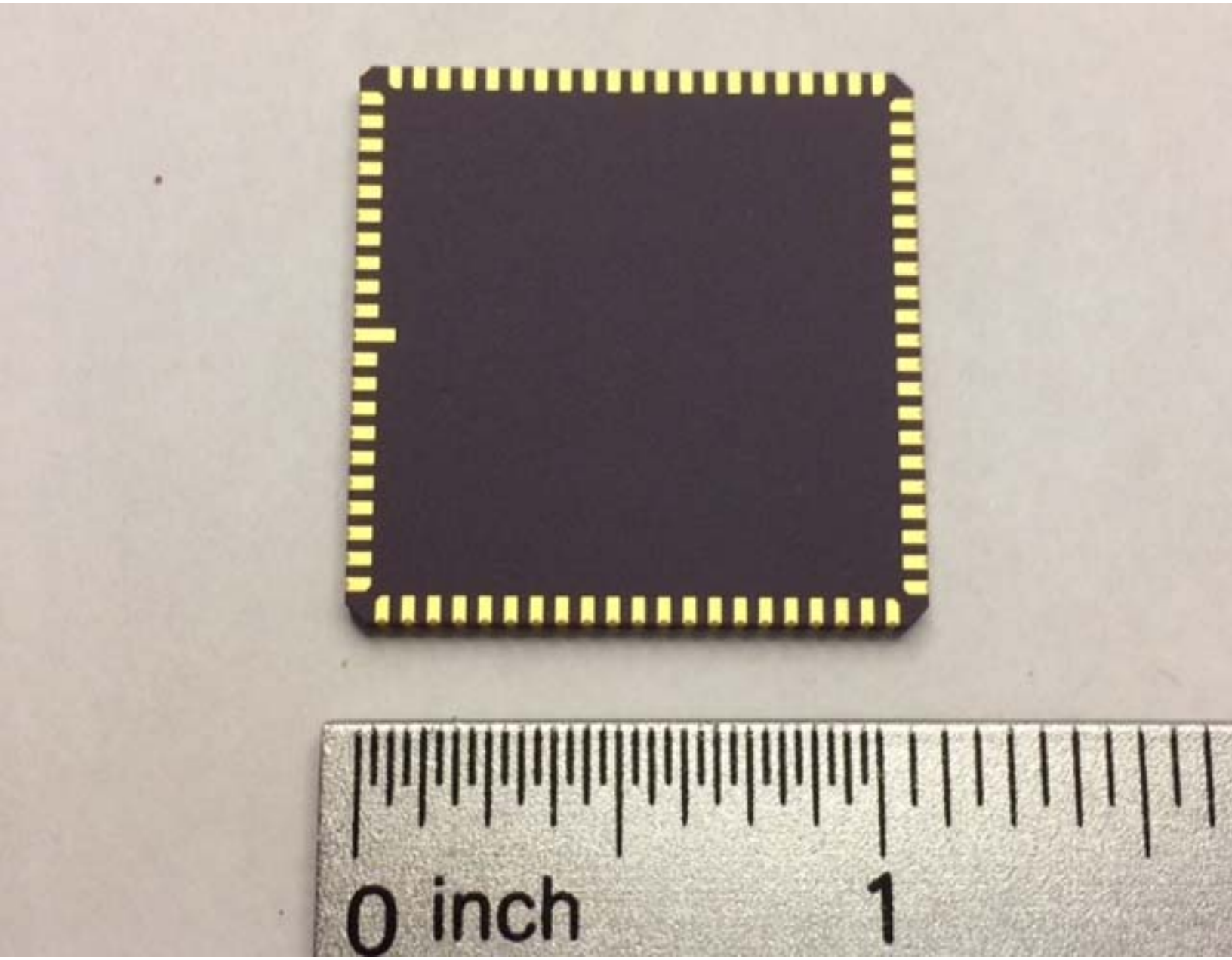
DRAWN	CHECKED	APPROVED	DATE
S.M	UC / K.I	M.S	NOV.10.'98

DRAWING NO. PB-C98D25
SHEET 1/2

SSM P/N LCC08422




0 inch
1


0 inch
1

Appendix F

AUXILARY TEST RESULTS

This appendix contains data collected during testing of the RIIC test chip and the SLED test chips relevant to the work presented. The first section

F.1 RIIC Test Chip Auxilary Results

The ART-IDEA RIIC super-pixel has two analog inputs that control the current output of the drive transistors. These lines are *vinn* and *vinp*. Additionally, each pixel has two gears, strong and weak, selectable via a digital input signal, *sels*. The inner pixels within the super-pixel are addressed in pairs by the x and y addresses. For example, pixel AN and AP are addressed at the same time, but get their analog input value from *vinn* or *vinp*, respectively.

In the RIIC super-pixel, there are a total of 16 pixels. There is a total of 8 pairs denoted with a letter from A-H, and either N or P, depending on the analog line used to drive it. The following plots F.8 through F.12 are sets of 10 curves each for each of the pixel pairs comparing the current output of all the pixels in strong mode.

F.2 SLED Auxilary Test Results

This section has more test results for the SLED test chips, broken down by chip number. SLED test chips that have the prefix AIG739 have a stage active region thickness of 133 nm. SLED chips with prefix IAG740 have a stage active region thickness of 266 nm. Additionally, if the second part of the prefix has the letter A, it means it uses Ti/Pt/Au for the metal contacts. The chip prefixes that have a B use an experimental contact made of Pd/Ge/Au. Note, R&D for experimental contacts has

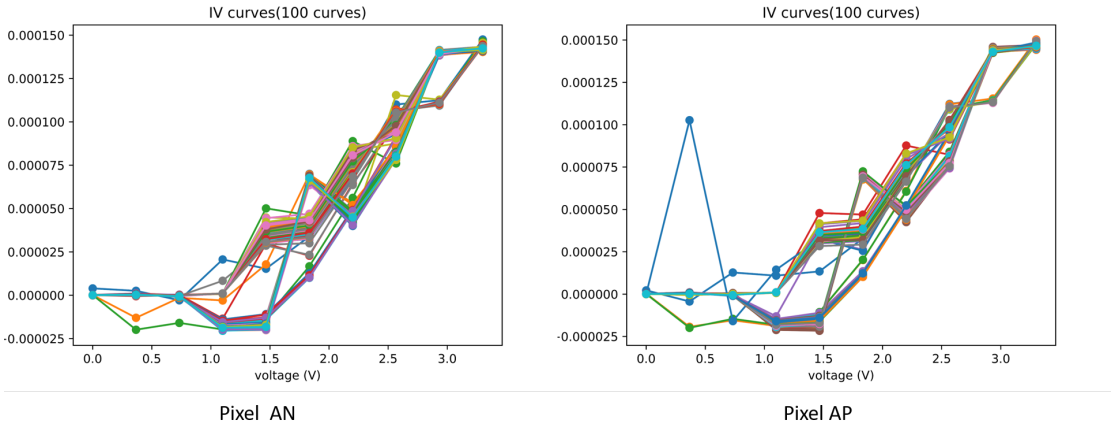


Figure F.1: Left: IV curves for pixel AN swept 100 times. Right: IV curves for pixel AP swept 100 times. This test proves the addressing scheme works, as well as that the analog inputs *vinn* and and *vinp* can control the weak gear current output. The LED power source is set to 5 V and the load used is a macro LED. Note: All 100 AN curves have been collected first with AP off. Then with AN off, the 100 curves on AP have been collected.

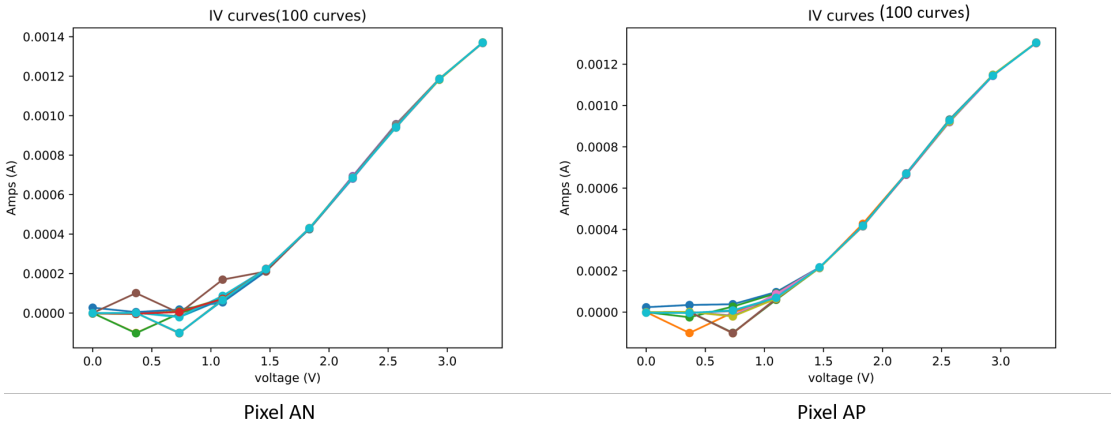


Figure F.2: Left: IV curves for pixel AN swept 100 times. Right: IV curves for pixel AP swept 100 times. This is the same test as figure F.1, but using the strong gear on the driver

not been performed in this work, they were simply used. Figures F.13 through F.17 present some of the relevant data collected during testing.

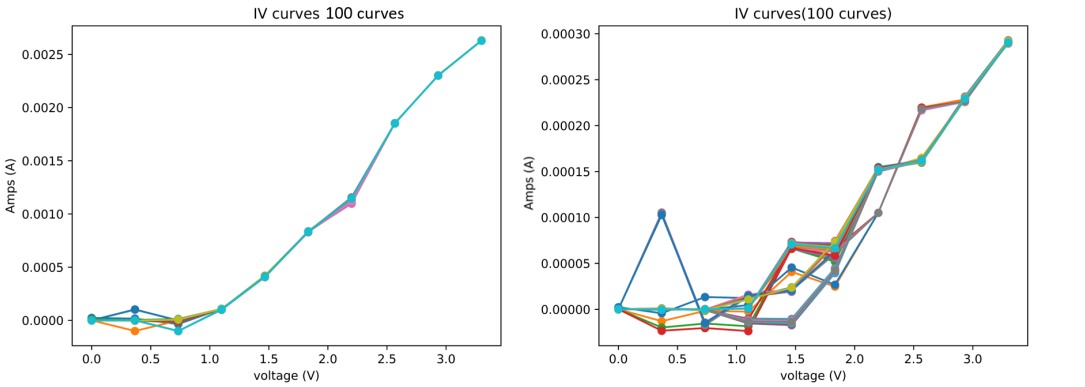


Figure F.3: Left: IV curves for pixel AN and AP in strong mode. Right: AN and AP IV curves in weak mode. For this test, the LED power source has been set to 5 V and the loads are the macro LEDs attached to AN and AP outputs on the test chip. In this test, both AN and AP have been swept simultaneously and, as expected, the current has increased by a factor of 2X.

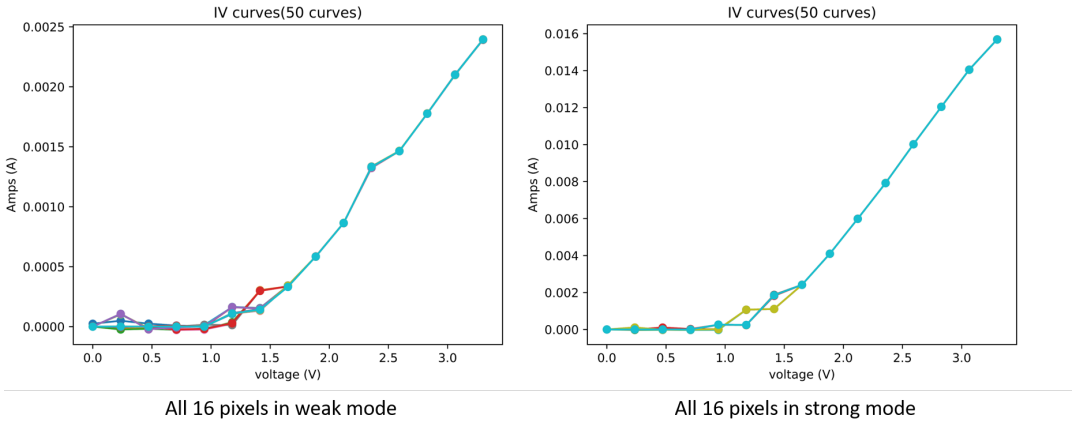


Figure F.4: Left: IV curves for all 16 pixels in weak mode. Right: IV curves for all 16 pixels in strong mode. LED power source set to 5 V, and as load, 16 macro LEDs attached to each of the pixels in the super-pixel. All pixels have been swept at the same time, thus this shows the maximum current used by the entire super-pixel for both gears.

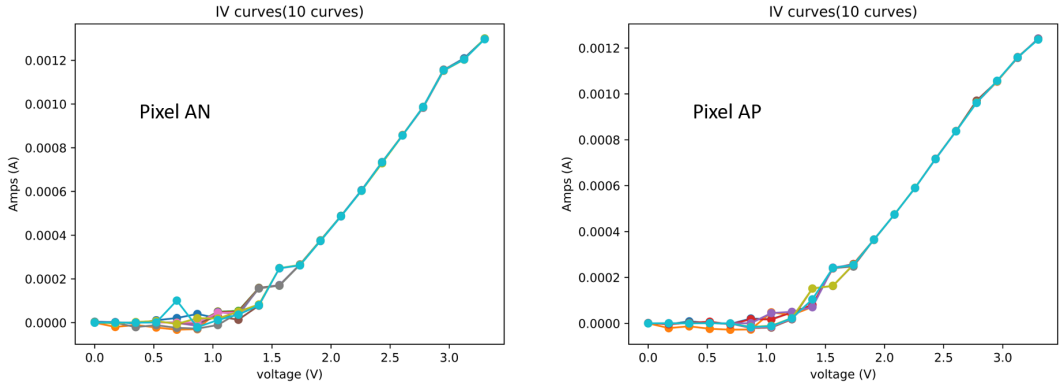


Figure F.5: IV curves comparing the performance of pixels AN and AP. Relative location within the super-pixel, AN is pixel (0,0) and AP is pixel (0,1).

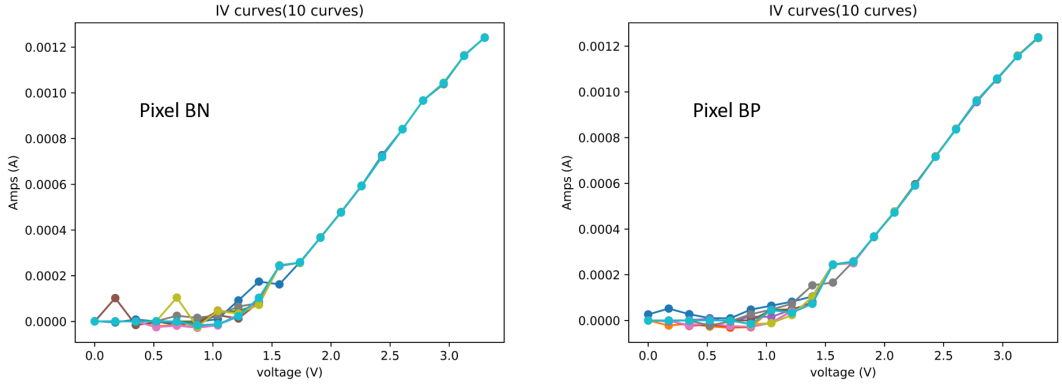


Figure F.6: IV curves comparing the performance of pixels BN and BP. Relative location within the super-pixel, BN is pixel (1,0) and AP is pixel (1,1).

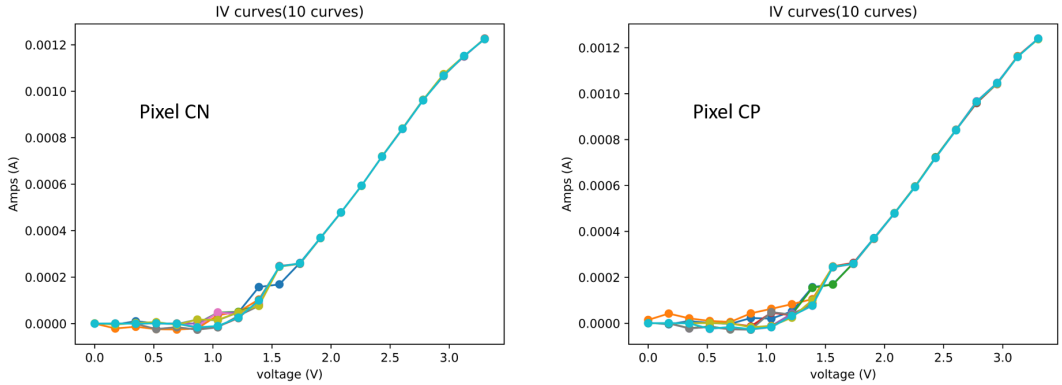


Figure F.7: IV curves comparing the performance of pixels CN and CP. Relative location within the super-pixel, CN is pixel (2,0) and CP is pixel (2,1).

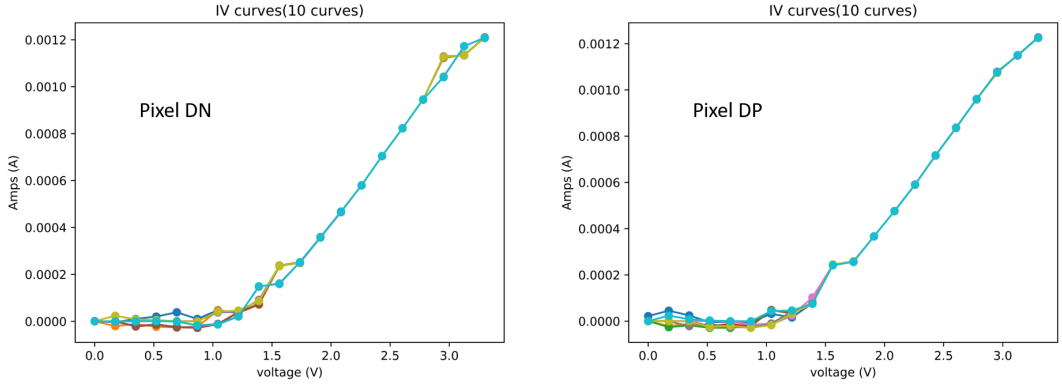


Figure F.8: IV curves comparing the performance of pixels DN and DP. Relative location within the super-pixel, DN is pixel (3,0) and DP is pixel (3,1).

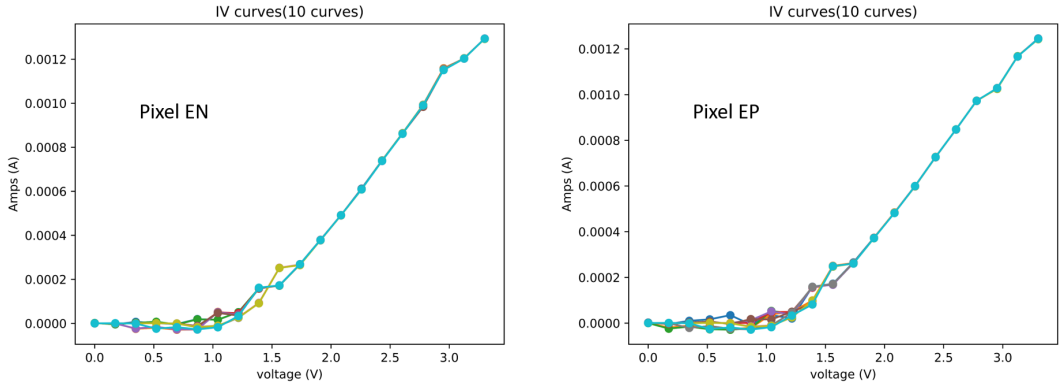


Figure F.9: IV curves comparing the performance of pixels EN and EP. Relative location within the super-pixel, EN is pixel (0,2) and AP is pixel (0,3).

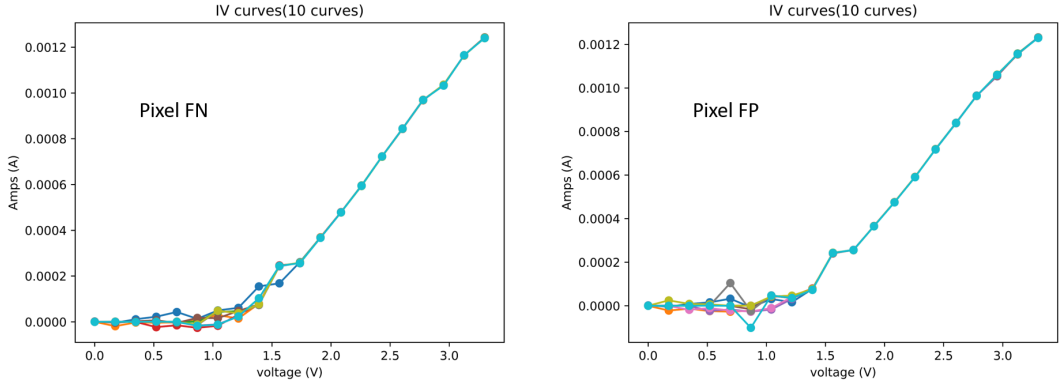


Figure F.10: IV curves comparing the performance of pixels FN and FP. Relative location within the super-pixel, FN is pixel (1,2) and FP is pixel (1,3).

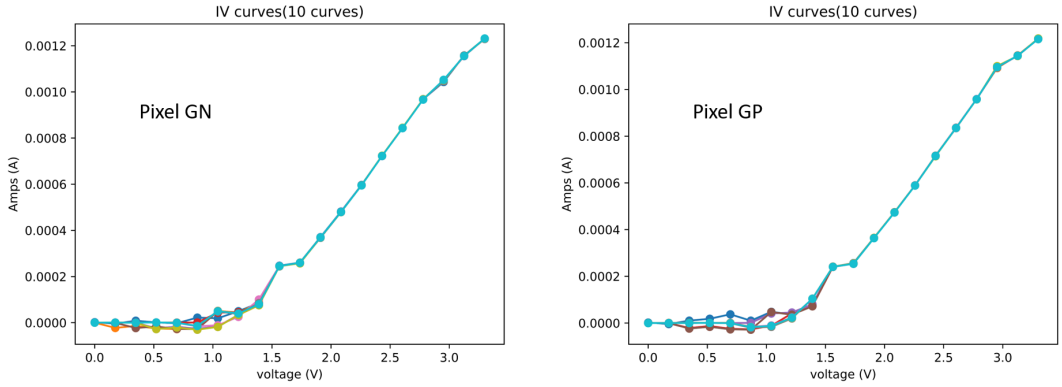


Figure F.11: IV curves comparing the performance of pixels GN and GP. Relative location within the super-pixel, GN is pixel (2,2) and GP is pixel (2,3).

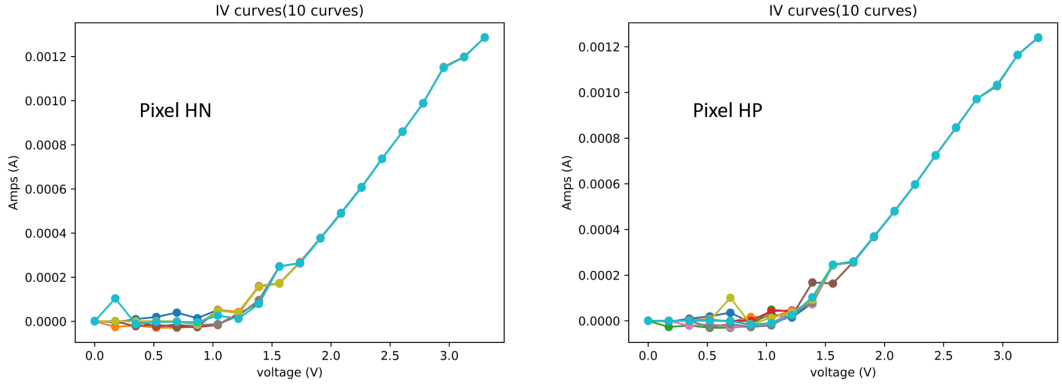


Figure F.12: IV curves comparing the performance of pixels HN and HP. Relative location within the super-pixel, HN is pixel (3,2) and HP is pixel (3,3).

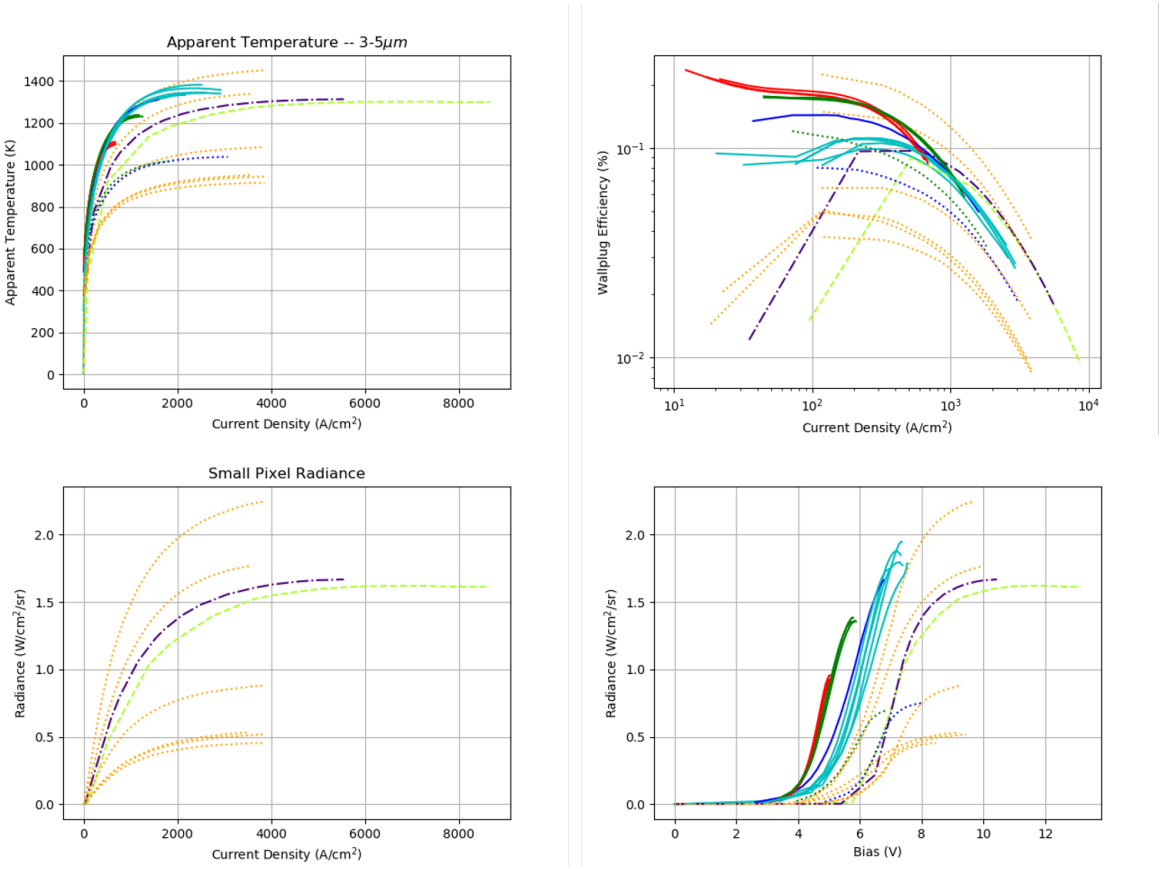


Figure F.13: Relevant data collected for SLED test chip IAG739-A02. Top Left: Apparent temperature as a function of current density. Top Right: Wall plug efficiency of the SLED devices tested. Bottom Left: Radiance vs. Current Density for small-format pixels. Bottom Right: Radiance vs. Bias Voltage.

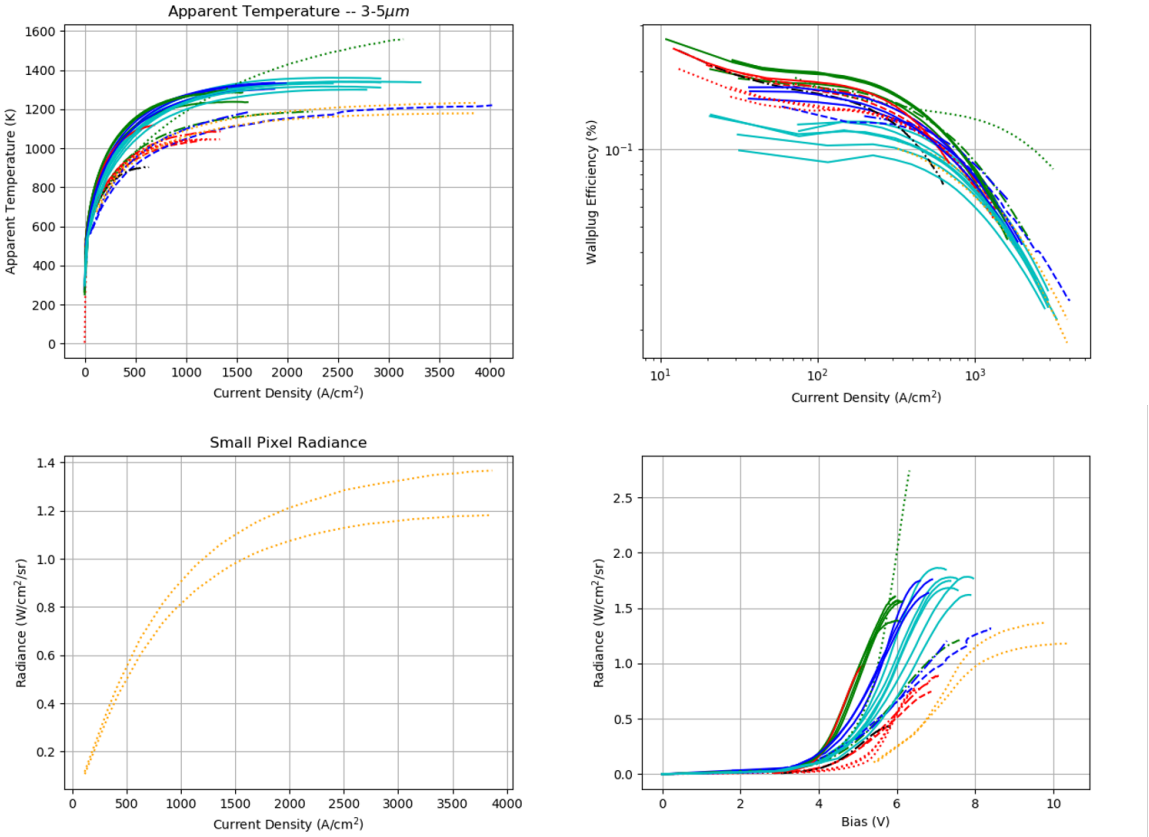


Figure F.14: Relevant data collected for SLED test chip IAG739-A03. Top Left: Apparent temperature as a function of current density. Top Right: Wall plug efficiency of the SLED devices tested. Bottom Left: Radiance vs. Current Density for small-format pixels. Bottom Right: Radiance vs. Bias Voltage.

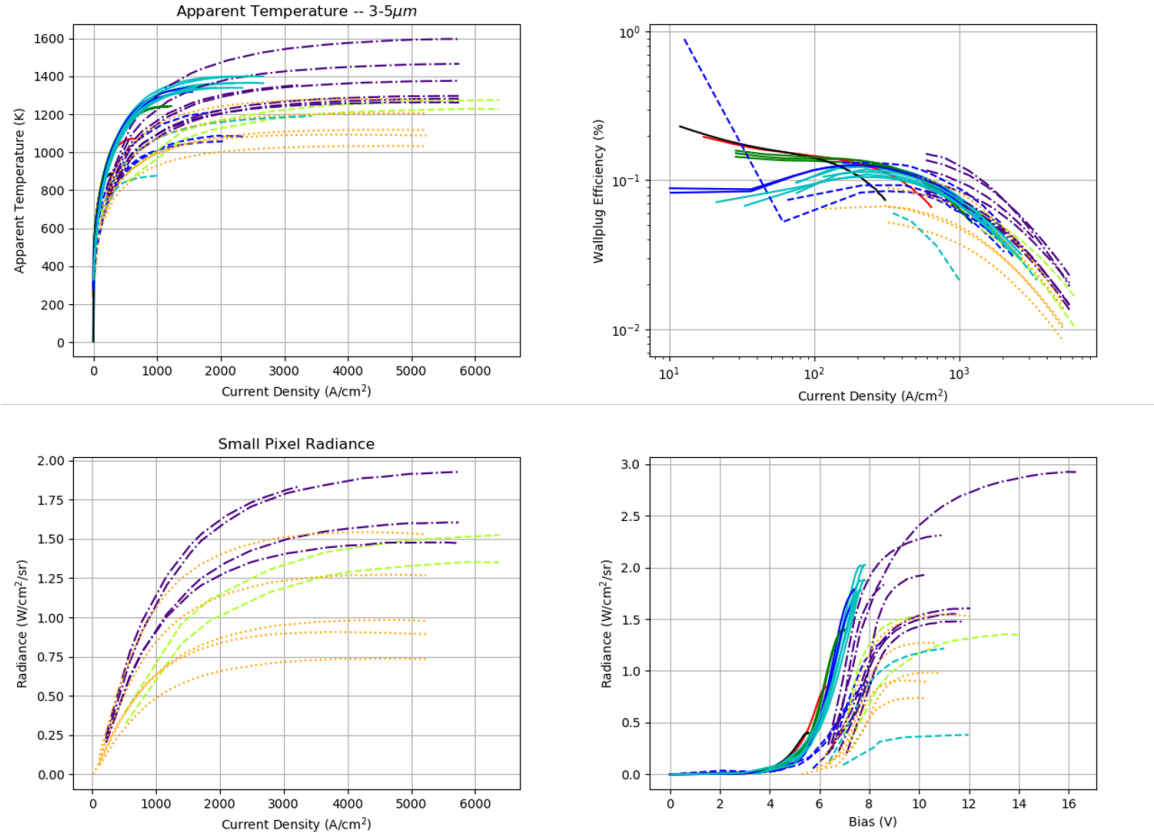


Figure F.15: Relevant data collected for SLED test chip IAG739-A04. Top Left: Apparent temperature as a function of current density. Top Right: Wall plug efficiency of the SLED devices tested. Bottom Left: Radiance vs. Current Density for small-format pixels. Bottom Right: Radiance vs. Bias Voltage.

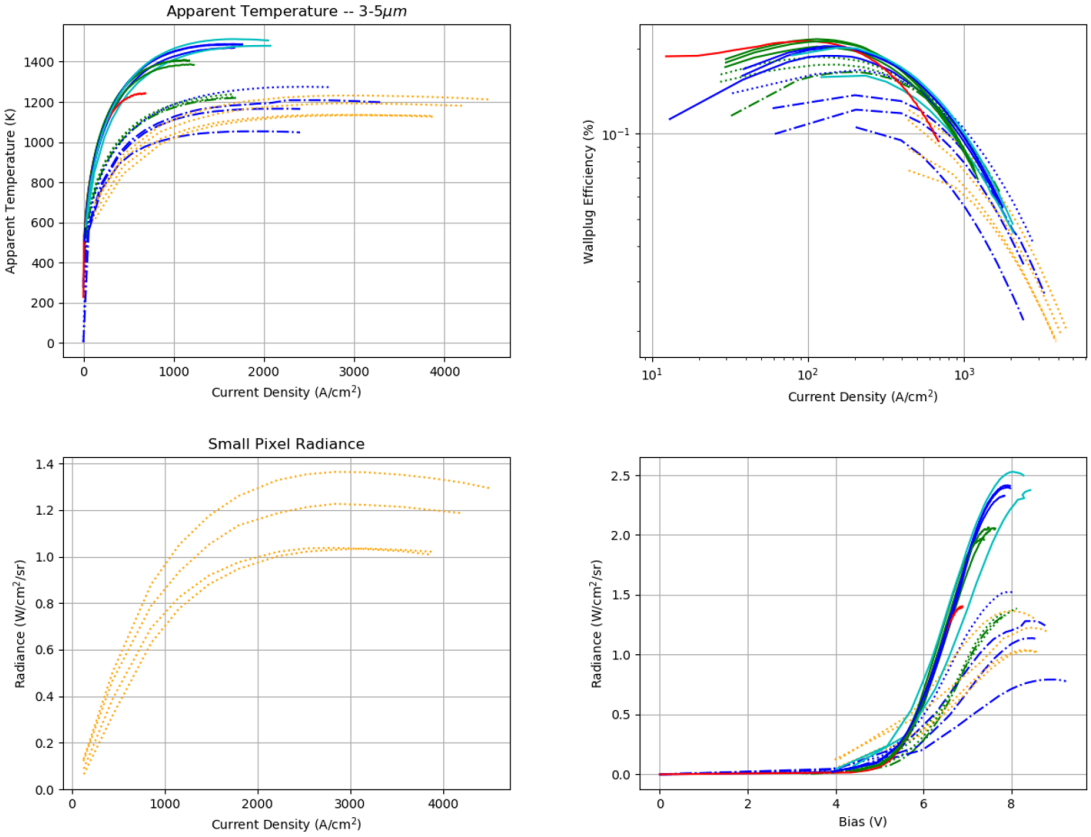


Figure F.16: Relevant data collected for SLED test chip IAG740-A02. Top Left: Apparent temperature as a function of current density. Top Right: Wall plug efficiency of the SLED devices tested. Bottom Left: Radiance vs. Current Density for small-format pixels. Bottom Right: Radiance vs Bias Voltage.

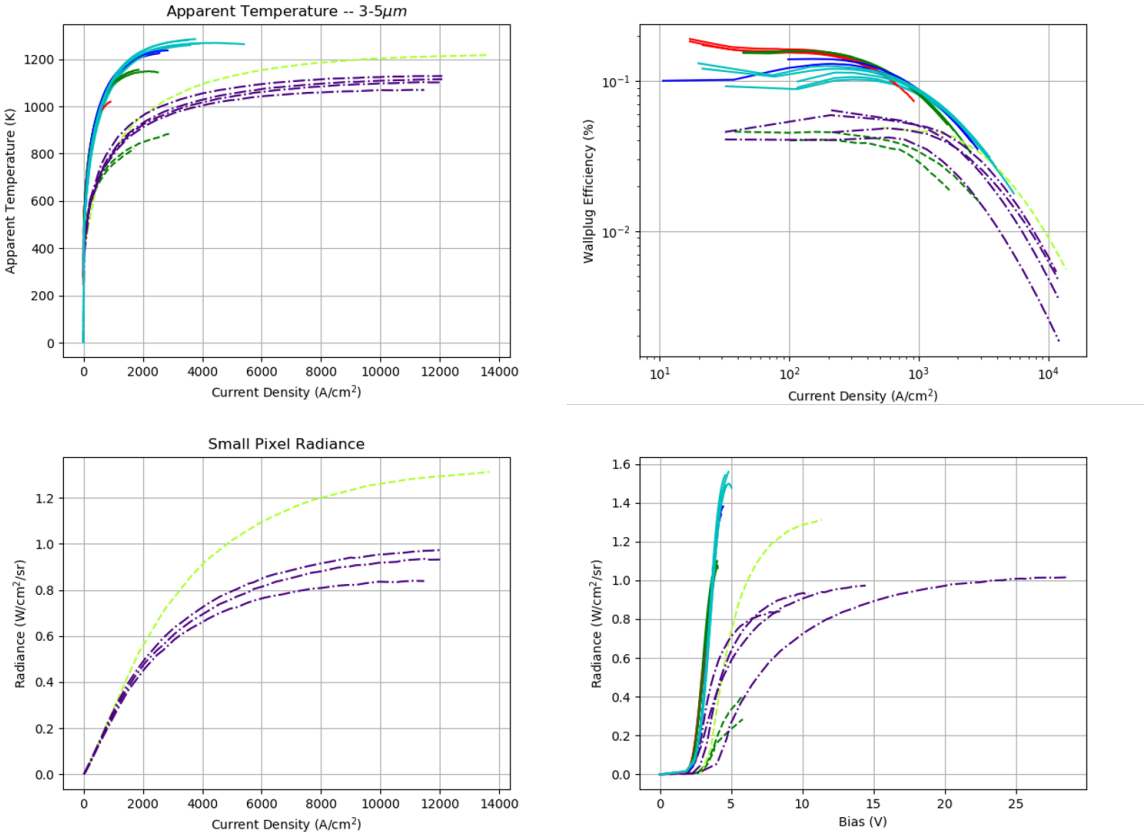


Figure F.17: Relevant data collected for SLED test chip IAG739-B02. Top Left: Apparent temperature as a function of current density. Top Right: Wall plug efficiency of the SLED devices tested. Bottom Left: Radiance vs. Current Density for small-format pixels. Bottom Right: Radiance vs. Bias Voltage.