PROCESSING AND PACKAGING FOR LARGE FORMAT INFRARED LED EMITTER ARRAYS FOR SCENE GENERATION

by

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A dissertation submitted to the Faculty of the University of Delaware in partial fulfillment of the requirements for the degree of Doctor of Philosophy in Electrical Engineering

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INFRARED LED EMITTER ARRAYS

FOR SCENE GENERATION

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ABSTRACT

Infrared light emitting diode (IRLED) arrays are a next-generation technology for infrared scene generation, which can be used for the calibration and testing of infrared (IR) cameras. These LED arrays can function as IR scene projectors (IRSPs) that emit narrowband IR light through individually addressable pixels. LEDs have the potential for faster framerates and brighter light output than the thermal pixel arrays traditionally used. A large team of collaborators in our research group and at the University of Iowa have built a full LED IRSP system that operates at 100 Hz and displays an equivalent blackbody emission of 1350 K within the 3-5 μm band. Since our initial success in 2012, higher temperature, higher resolution and faster framerate arrays have been developed and are currently being tested by our team at the University of Delaware. Most of the development by our team has been on hybrid arrays, which consist of a gallium antimonide (GaSb) emitter flip-chip bonded to a silicon CMOS read-in integrated circuit (RIIC). Building an LED microdisplay to work with custom electronics requires materials processing to facilitate flip-chip die bonding, which presents many challenges. Along with this work, packaging the array in a cryostat needs careful planning and engineering to allow enough heat removal on the array and strong integrity of the analog electrical signals coming in. In this dissertation the processing and packaging of the IRSP systems are described in detail.

Two key improvements that need to be made with our IRSP systems are dynamic range of light output and heat removal. The RIIC requires innovations in its design to both scale down in size and improve dynamic range of the LED's emission.

Part of implementing these innovations is modelling and improving the RIIC, specifically the transistors and pixel circuit used to power the LEDs. To reduce heating, an investigation into etching a lens shape to the output surface of each LED hopes to show a path to decreased reabsorption of emitted light.

Lastly, infrared light is used to transmit signals for chip-to-chip communication. Normally, optical interconnects require additional optical components to generate and direct light, but by using bond wires as transmission lines, optical connections can be made between CMOS chips without additional wave guiding components. A theoretical loss analysis for a two wire optical transmission line is presented. Experiments to show IR light transmission through the two wire transmission line have been attempted without any success yet at this time.

Chapter 1

SUPERLATTICE LIGHT EMITTING DIODES

Introduction

Infrared scene projectors (IRSPs) are useful tools for tuning and calibrating IR detector systems. Because of the IR light emitted by heat on the surface of objects, imaging at these wavelengths can be advantageous to visible wavelength imaging, especially for example at night, when visible wavelength energies are too low for reliable detection. It is more difficult to create systems that have strong, coherent emission of IR light than it is to develop IR detectors because of the nature of the IR sensitive materials. There are also many challenges associated with light emission that detection does not have, including light extraction, directionality, and thermal dissipation. Even more, the electronics used to drive an IRSP must be strong enough to display bright emission from the light emitting diodes (LEDs) while also being dynamic over the wide range of light energies [1]. Building an IRSP then requires an engineering team that understands optics, device physics, semiconductor processing, electronic circuit design, and software development.

To begin, chapter 1 of this dissertation will cover the background and processing for the development of the first 512 x 512 pixel fully addressable LED IRSP system. Chapter 2 will cover some of the design and testing of the circuitry advancements for the next generation of IRSP RIICs. Chapter 3 will cover new experimentation for the future of improved efficiency in the light output of the IRSP systems. This improvement is hoped to be achieved by altering the surface of the

LED array, improving light extraction. Chapter 4 will cover a different application of infrared light from semiconductors: the investigation of a novel idea for chip-to-chip optical communication. Finally, chapter 5 will conclude this dissertation by summing up the major contributions.

Infrared Light and Semiconductors

Figure 1 IR light image seen by a Flir camera. High temperatures show up very bright to an IR detector.

Visible wavelengths that humans can see make up only a small portion of the electromagnetic spectrum from 390-700 nm. Just beyond these wavelengths the infrared exists, showing heat as bright light as shown in figure 1. Due to surface charges, everything above zero Kelvin emits energy in the form of electromagnetic

radiation, with intensity and peak wavelength depending on its temperature. The radiance is given by Planck's Law:

$$B_{\upsilon}(\upsilon,T)=\frac{2h\upsilon^{3}}{c^{2}}\frac{1}{e^{\frac{h\upsilon}{k_{B}T}}-1}, \tag{1.1}$$

where υ is frequency, T is temperature, c is the speed of light, and h is Planck's constant.

As temperature increases, the object will emit more energy with the peak wavelength getting shorter, as shown in figure 2 [2]. This energy is apparent as visible light in the glow of a fire or the sun because of their high temperatures. Even though their peak wavelengths and most of their energy are in the visible spectrum, the intensity levels in the infrared and longer wavelengths still increase with temperature. Because of these shorter increments in intensity, materials that are specifically sensitive to infrared light can be used to sense temperature levels.

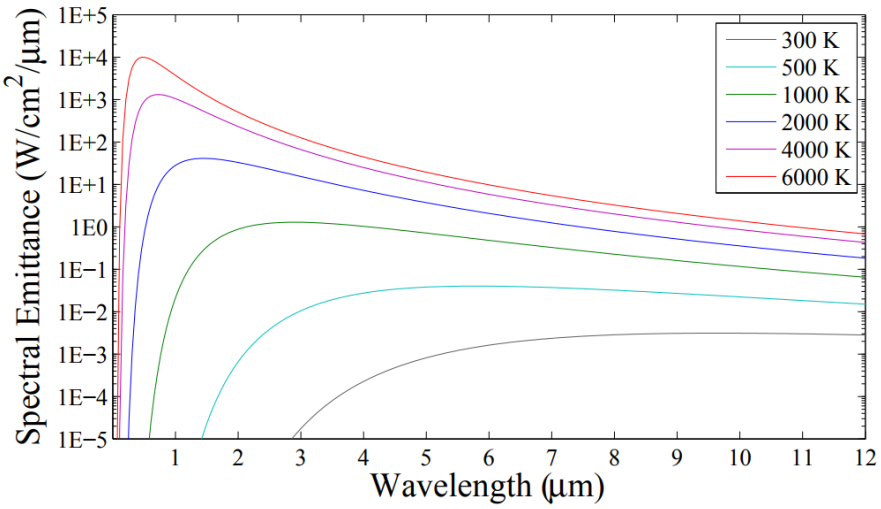

Figure 2 Spectral radiance as a function of wavelength for different temperatures [2]. At higher temperatures, more intensity is emitted at the shorter wavelengths.

While the IR spectrum covers wavelengths from 0.75 to 1000 μm, the bands closer to visible light are of the most interest for the work discussed here. Particularly, the mid-wavelength infrared (MWIR, 3-8 μm) has good atmospheric transparency, except around 4.3 μm where CO_2 gas will absorb radiation. Assuming the material has the correct energy band levels it can be used as a photodetector by converting the energy from the thermal radiation into electrical current. This conversion happens when electrons occupying lower energy levels are excited to higher ones. In semiconductor materials, electrons occupy most of the energy states (the valence band) below a forbidden energy band gap. In typical semiconductor materials, there are no electron energy levels in this gap. Above this gap (the conduction band) are energy states that are mostly unoccupied. Due in large part to the doping of

semiconductor materials with other elements, there are several holes (unoccupied states) in the valence band, and mobile electrons in the conduction band.

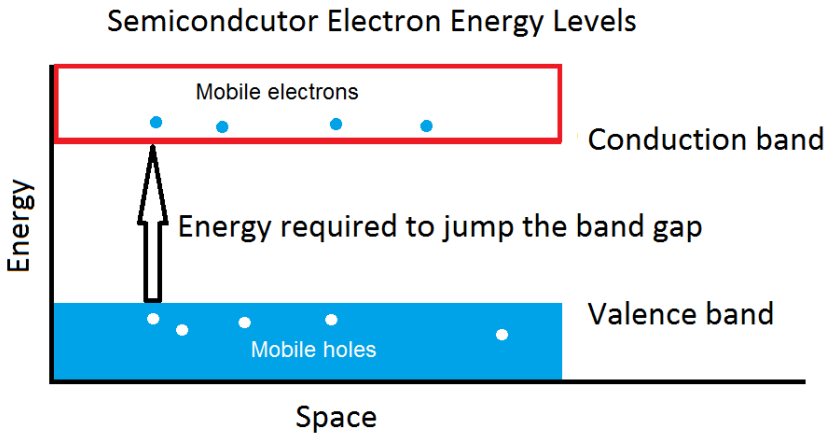

Figure 3 Energy levels in a semiconductor material. The top conduction band is empty with a few free carriers (electrons), and the bottom is full with a few holes (energy states unoccupied by an electron).

A photon of light will have a wavelength directly proportional to its energy shown in the Planck–Einstein relation:

$$E = h\nu \tag{1.2}$$

where E is the energy, h is the Planck constant, and ν is the frequency. When this wavelength corresponds to an energy level greater than that of the band gap, it can excite an electron into the conduction band. In the case of a photodetector, this electron is swept away by an electric field and registered as current.

Microdisplays

For standard use, IR focal plane arrays (FPAs) will take in a wide angle of light from a scene and measure light intensity with a two dimensional array of detectors. This concept is shown in figure 4 [2], where light is refracted through lenses to form a detectable image of the correct size to match size of the array. If the light source is instead a microdisplay, the microdisplay output must first be collimated and refocused onto the detector. In figure 5 [2], a video signal through the microdisplay can simulate a wide angle view. The ability to drive video makes the microdisplay ideal for testing and calibrating an IR camera inside a controlled environment. This setup shown in figure 5 is referred to as hardware in the loop (HWIL).

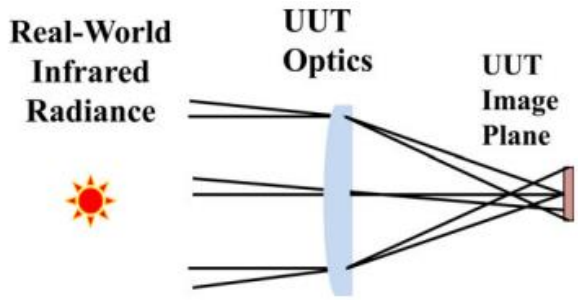

Figure 4 Real world imaging of infrared light onto a unit under test (UUT) [2].

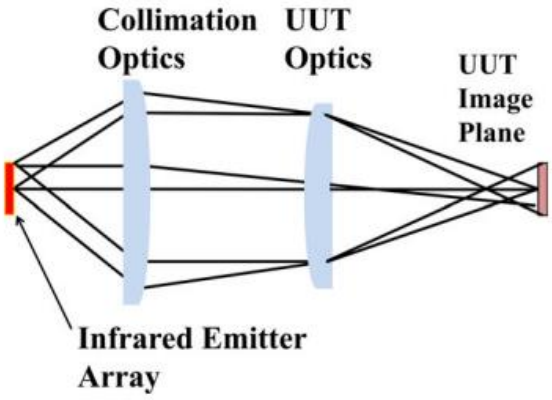

Figure 5 HWIL IR scene projection onto a unit under test (UUT) [2].

Thermal Pixel Arrays

One way to generate infrared radiation is to use a blackbody emitter. Scaling this idea to a two dimensional IRSP, this means creating an array of individually addressable resistors, small enough to represent pixels in a microdisplay. To "light" a pixel, the user drives current through the resistor generating heat and IR light. These thermal pixel arrays (TPAs) have existed as a technology since the 1980s, and are still being developed today [3-6]. Their emission is very wide band, and covers the entirety of infrared wavelengths. Because the TPA's pixels have to actually heat up to the temperature they are projecting, representing very hot objects becomes an increasingly difficult challenge. Having the resistor material reach a high enough temperature is costly in time and power. Furthermore, the thermal cycle time that each pixel must undergo limits the read out framerate of the TPA IRSP system.

Infrared Light Emitting Diode Arrays

A technology that does not suffer the same inherent problems as TPAs is based on infrared light emitting diodes (IRLEDs). LEDs emit light by controlling an electric

current through a p-n junction of a material with a direct bandgap. Just as a photodiode can turn light into current, LEDs can turn current into light. When energized electrons in the conduction band recombine with holes in the valence band, their energy can be released in the form of light at a wavelength corresponding to the energy of the bandgap, creating a light output that is narrowband around a specific wavelength, different from broadband blackbody emitters.

A key requirement for a semiconductor to emit light efficiently is that it has a direct bandgap, as shown in figure 6. While indirect bandgaps may emit light with the combination of a phonon and photon being released, the probability of this happening is much lower [7]. With direct bandgap materials, such as gallium arsenide (GaAs), gallium nitride (GaN), indium antimonide (InSb) and other III-V materials, light emission is probable when free electrons relax to the valence band. While other materials such as silicon [8-13] and germanium [14-17] have been engineered for light emission, the challenges in reaching the efficiency of other materials makes them less attractive as sources.

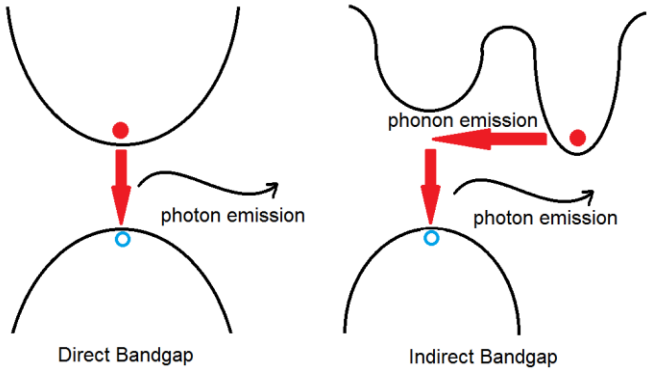

Figure 6 Direct and indirect bandgaps in terms of energy levels vs. k space. Direct bandgaps allow for photon emission without the need for a phonon emission as well, making light output more probable.

The nature of a semiconductor light emitting diode creates what is called an apparent temperature of its light output. A 3-5 μm filter is common on many MWIR detectors. At these wavelengths, a detector will see a certain amount of energy that corresponds to an object of a certain temperature. Using this correlation, an LED emitting high energy in the 3-5 μm range may appear to be a certain temperature to that detector while not actually being that hot. This temperature is called an apparent temperature, and depends on the wavelengths being imaged. The maximum apparent temperature over a given spectral range is a useful metric for evaluating an IRSP, as users may want to display extremely hot objects to their detectors.

Superlattice Light Emitting Diodes

Because of the demand for improved IRSP systems, research into new technology has grown [18-23]. Much of this research centers on IRLEDs [19-23], including initial investigations that would eventually lead to a superlattice light emitting diodes (SLEDs) IRSP systems. First, at the University of Iowa, cascaded

superlattice diodes were tested for their output and spectral emission [21]. Later, similar devices to those diodes would be shown with improved quantum efficiency, displaying apparent temperatures greater than 1400 K to a 3-5 μm narrowband detector [24]. At the University of Delaware, a read-in integrated circuit (RIIC) was then bonded to the SLEDs to form a hybrid emitter [25], leading to the development of a 68x68 SLED array flip chip bonded to a RIIC [26].

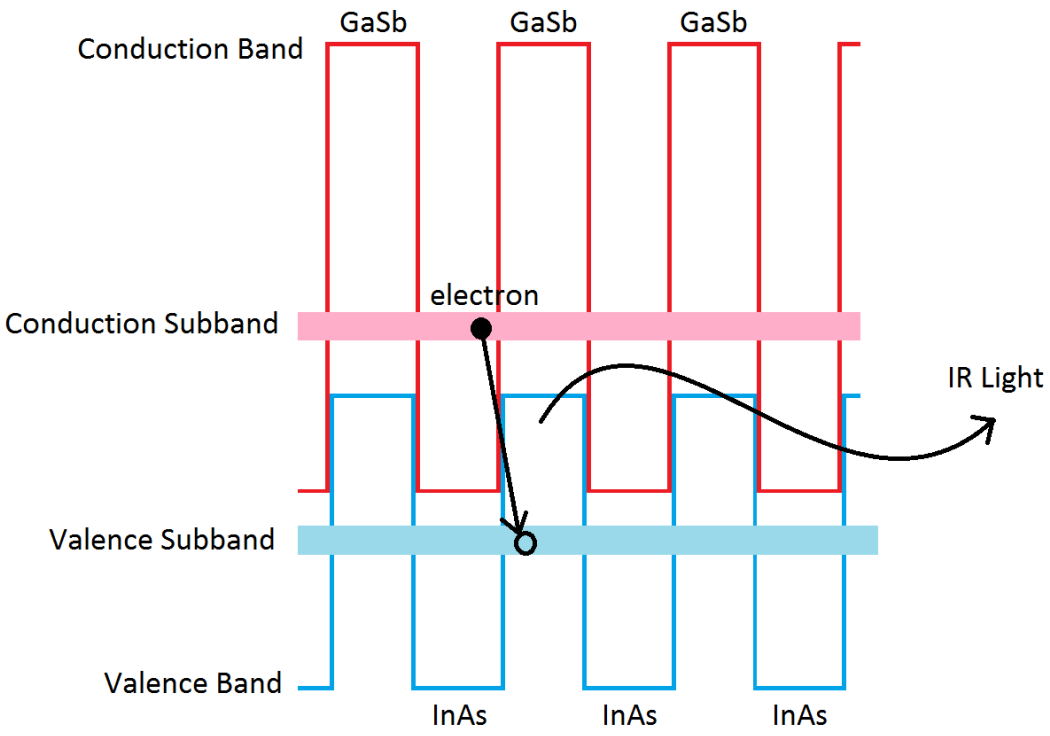

Figure 7 Band structure of a type II superlattice. The electron relaxes and energy is emitted in the form of a photon.

The final goal of the SLEDs project was to create a 512 x 512 pixel array that would emit strong IR light in the 3-5 μm band, displaying video at 100 Hz. Previous testing showed that the cascaded InAs/GaSb type-II superlattice LEDs would display apparent temperatures up to 1350 K [27]. A Type II superlattice repeats alternating layers of two different materials, each layer only a few nanometers wide [28]. This short spacing allows for electron tunneling between the mismatched band structures shown in figure 7. Here subbands are formed because of the effect of the quantum wells, so an electron may move between the gallium antimonide (GaSb) valence subband and the indium arsenide (InAs) conduction subband. By driving current through these junctions, electrons moving along the conduction band can relax to the valence band, emitting light. The energy levels of the subbands depend on the energy band differences of the alternating materials. Because of this dependence, the wavelength output can be tuned by layer thickness during MBE growth [29]. More detailed information on the physics and development of these type II super lattices is available but will not be discussed here [2].

The design for the SLEDs system was to take a 3" wafer with a molecular beam epitaxy (MBE) grown SLEDs array on it, and flip-chip bond it to a silicon RIIC. Flip-chip bonding for optoelectronic components to silicon CMOS has been developed in the past [30] and was implemented at a large scale in the SLEDs array. The hybrid chip was aligned so that each pixel on the array lined up with its own matching pixel circuit on the RIIC. Each of these matching pixel circuits on the array and RIIC would be 48 x 48 μm, with a large centered anode contact and smaller common cathode contacts. The hybrid was flip-chip bonded and packaged by Teledyne Scientific Co. Once hybridized with indium bump bonds, the array and

RIIC were mounted on a balanced composite substrate (BCS). This BCS, bonded to the silicon side of the hybrid, would help match the coefficient of thermal expansion (CTE) to the GaSb array, to prevent cracking when the array would be thermally cycled between 77 K and room temperature. The stack-up is diagrammed in figure 8 [31].

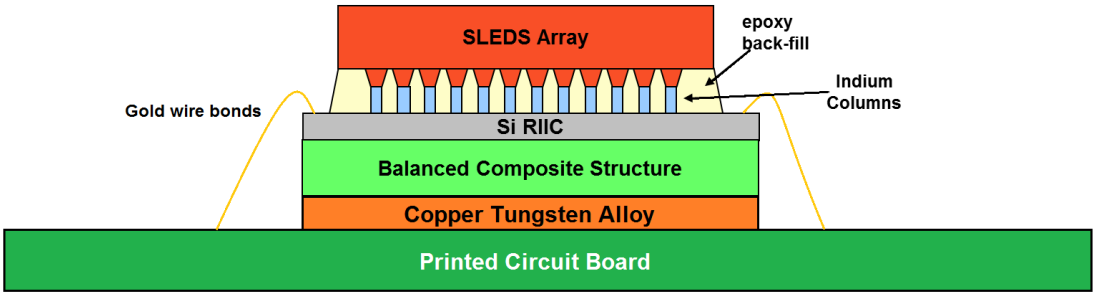

Figure 8 SLEDs hybrid stack-up [31]. The red SLEDs array and gray silicon RIIC layers make up the hybrid. The hybrid is mounted to the BCS and wire-bonds allow for connecting to the hybrid through the PCB.

The stack-up was then epoxied to a copper-tungsten (CuW) plate designed to match the CTE of the hybrid. Metal wire-bond pads along the outside of the RIIC were still exposed, allowing for gold wire-bonds to connect the hybrid to a PCB that the CuW plate was mounted to. To allow for use at 77 K, a dewar holding liquid nitrogen thermally connected to a cold finger was placed in contact with the CuW plate, while another PCB carried the signals and power required for the hybrid's operation. This PCB could be accessed electrically through the back of the Dewar, where the custom support electronics could be easily plugged in with four 50-pin IDE

cables. These support electronics would include digital control signals, as well as analog voltages from digital to analog converters (DACs) and amplifiers.

The resulting project involved a large amount of work including hybrid processing, electronic circuit design and assembly, as well as software and firmware development. One of the first steps of development would be processing the GaSb wafers with the superlattice layers into SLEDs chips ready for hybridization. The end goal for each 512 x 512 pixel array was to create anode and cathode metal contacts. The anodes contacted the top surface of the emitter chip, and the cathodes contacted 4.24 µm deep into the material where the last stage of the superlattice layers end. A stack-up of the wafer layers is shown in figure 9 [27].

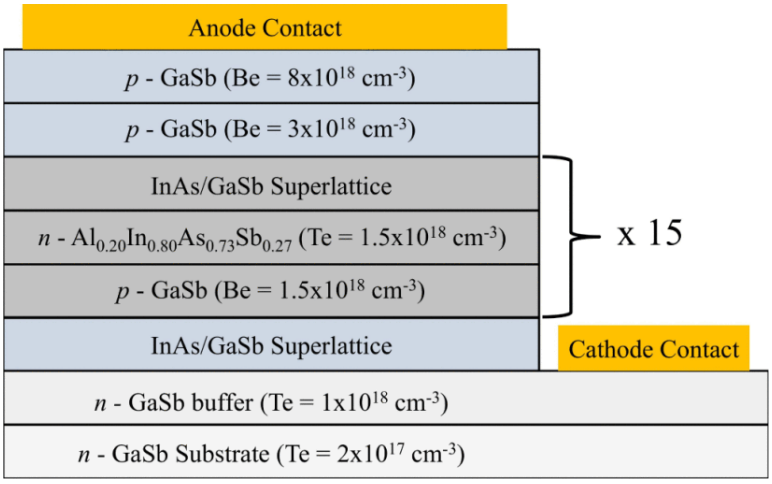

Figure 9 SLEDs growth layers. The p-n junction and superlattice layers repeat to form 16 stages. The p-type layers at the top are 140 nm thick, the InAs/GaSb superlattice layers are about 200 nm thick, and the p and n type layers making up the p-n junctions are 30 nm each, together making up 60 nm per stage. The total of these layers creates a 4.24 µm difference between contacts [27].

SLEDs Array Processing

SLEDs arrays were grown on 3” GaSb wafers with 16 superlattice layers [27]. The SLEDs processing is shown by diagram in figure 10.

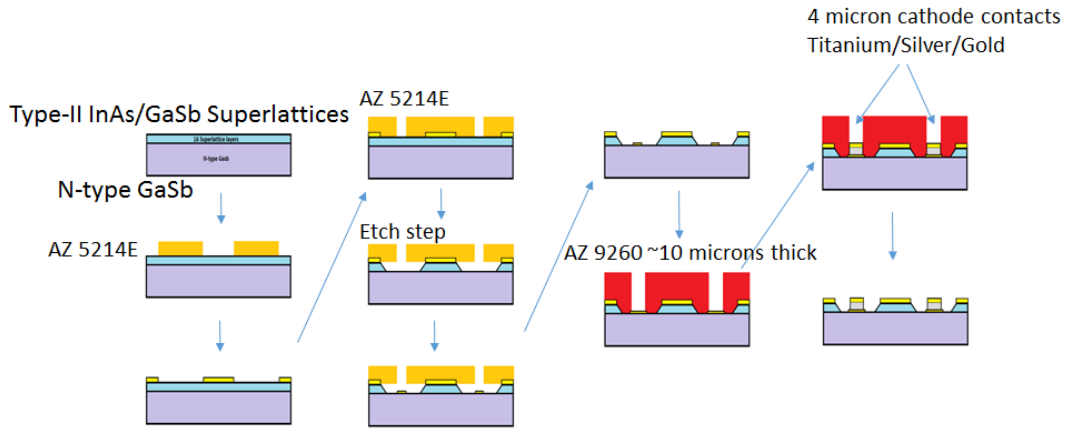

Figure 10 Side view diagram of SLEDs processing steps in preparation for flip-chip bonding.

Anode Contact

The processing for the SLEDs array started with the first electrical contact designed to match the RIIC: an octagon shaped anode pad shown in red in figure 11. First, the wafer was dipped in a mixture 1 part photoresist developer AZ400K and 4 parts DI water for one minute to remove any unwanted material of the surface of the wafer in an effort to guarantee strong metal adhesion. This step was done with a little agitation, and after the wafer was rinsed with acetone, methanol, and isopropanol (AMI) before blow drying and inspection.

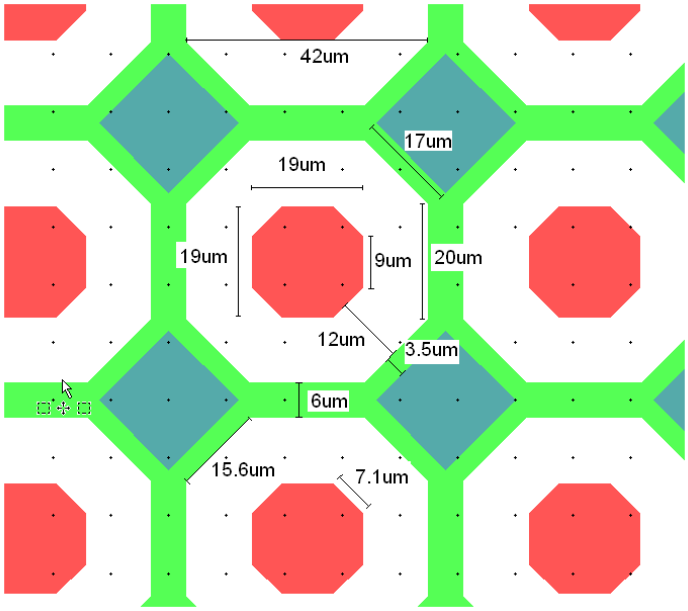

Figure 11 Top down diagram of the SLEDs array mask layers. The red mask creates the anode contacts. The green mask creates the cathode rails. The dark green mask creates the cathode pillars.

Assuming the wafer passed visual inspection with a clean surface, it was then cleaned again with AMI at 3000 rpm on a Headway PWM32 spinner for roughly 10 seconds for each solvent, and then allowed to spin dry. Then photoresist AZ 5214E was applied, and the wafer was spun at 3000 rpm for 40s to uniformly distribute the coating. After this resist spinning, the wafer was soft baked for 1 minute at 90° C, and allowed a few minutes to cool. Once baked, the anode mask was aligned and contacted to the wafer using a Karl Seuss MJB 3 mask aligner, and the wafer was exposed for 18 seconds with 365 nm light at 275 W. After exposure, the photoresist was developed in AZ 400K:DI water, 1:5, for 20-25 seconds, only being removed from the developer once the wafer was visually clear of the photoresist layer, plus an

additional 10 seconds. The wafer was immediately rinsed with DI water after development.

The high ratio of DI water to developer was used because of challenges with over or under developing at a higher concentration. Finding the correct timing was difficult, and leaving any photoresist in an undesirable place could eventually lead to metal delamination. To finish lithography, the wafer was dipped in HCl:DI water 1:10 for 30 seconds to etch away unwanted surface material, followed by blow drying with nitrogen.

Next, the wafer was loaded into a thermionics VE-100 e-beam and thermal evaporation system for deposition of 7 nm of titanium and 150 nm of gold to provide an anode contact for flip-chip bonding. The titanium was evaporated with an e-beam source and the deposition rate kept under 1 Angstrom per second. The gold was evaporated with a thermal source with a deposition rate at or less than 2 Angstroms per second to ensure a uniform layer. Once removed from the evaporator, the chip was soaked in acetone for at least 30 minutes, and a spray-bottle of acetone would be used to rinse off any of the remaining metallic layer on the photoresist. If liftoff problems persisted, agitation in an ultrasound bath would help significantly, but this was used as a last resort because the aggressive agitation would delaminate some of the anode contact metal.

Wet Etch

For the cathode fabrication, the wafer was cleaned with an AMI rinse on the spinner again before applying the same AZ 5214E photoresist recipe as for the anode, making sure it was aligned so the cathode rails surrounded the anode contacts. It was critical that the alignment was precise to within about 2 μm as these would need to

align for flip chip bonding, as well as providing at least 10 μm of space for lateral etching.

To create mesas as shown in the fifth step of figure 10, the wafer had to be wet etched in the areas left uncovered by the cathode patterned photoresist. The recipe for etching was 55:3:10 $C_6H_8O_7$ (citric acid):H_3PO_4 (phosphoric acid):H_2O_2 (hydrogen peroxide). This etch was performed at 40° C with a magnetic stirrer running to help improve uniformity by increasing the etchant flow across the surface of the wafer. It should be noted that outside of the array areas on the wafer etched first, moving inward, making uniformity across the entire wafer difficult. After removal, the wafer was rinsed with DI water and then dipped in HCl:H_2O 1:10 for 30 seconds to clean the surface. After drying with nitrogen, the wafer was ready for the cathode rail deposition. A layer of 7 nm of titanium and 150 nm of gold was deposited similarly to the anode contact, to cover the bottom of the etched out "valley" area.

Cathode Contact

The last step was to create cathode pillars that came up to the same height as the anode contacts. To create the cathode, the wafer was cleaned on the spinner with AMI, and AZ 9260 was spun onto the wafer at 2000 rpm for 50 seconds. This photoresist was chosen because at the given spin speed, it has a thickness of about 10 μm, and the metal deposition would be about 4 μm thick. It was important to get a thick layer of photoresist all over the entirety of the wafer before spinning to guarantee a uniform result. After spinning, it was soft baked at 110° C for 2 minutes. Then, the cathode mask had to be aligned to exactly where the cathode rails intersected, as shown in figure 11. Misalignment would result in problematic shorting of part of the LED, as well as make flip chip bonding more difficult. A misaligned cathode contact

can be seen in figure 12, where the cathode creeps up the walls of the mesa and shorts out some of the SLEDs layers.

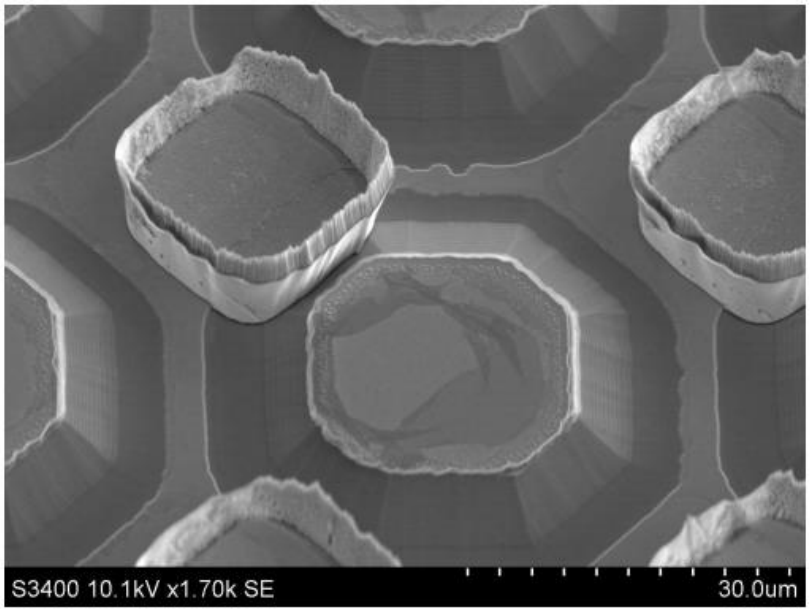

Figure 12 Misaligned cathode contact causing LED shorting and misaligned indium bump contact to RIIC.

Once aligned, the resist was exposed for 45 seconds with 405 nm light at 275 W. After exposure, the resist was developed in AZ 400K:H_2O 1:3 for 1 to 2 minutes. While agitating the mixture, the photoresist removal had to be carefully monitored visually to determine the timing of the removal from the developer. The removal was performed quickly after the photoresist was cleared away to prevent overdevelopment. Finally the wafer was dipped in HCl:H_2O 1:10 for 30 seconds right before loading for cathode metal deposition.

The cathode metal deposition that would complete the processing of the SLEDs wafer was 7/3850/150 nm of titanium/silver/gold, totaling about 4 μm. Due to excessive heating of the evaporator when run for too long, this evaporation had to be done in several steps, and took at least 8 hours of operating the VE-100. The silver deposited at around 5-7 angstroms per second. The gold was not deposited faster than 2 angstroms per second. Liftoff was exceptionally difficult due to the thickness of the metal layer, but generally would be fine if left overnight to soak in acetone. Given that everything was done correctly, the metal layer would come off as one clean sheet, leaving behind only the small cathode pillars. An image of the resulting array contacts is shown under microscope and a Zygo interferometer in figure 13.

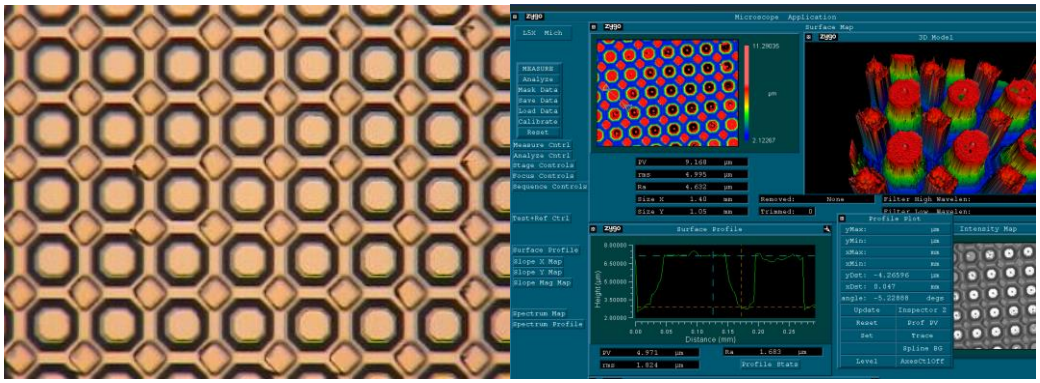

Figure 13 Gold anode and cathode contacts after processing. The left shows a microscope image. The right shows a top-down Zygo output image, where the anode and cathode contacts are shown to be at similar heights, which is ideal for flip-chip bonding.

Challenges

There were many challenges during processing that led to the tweaking of the recipe. The first challenge was the fact that GaSb is very brittle, making it difficult to

process without cracking. The biggest issue was on the spin-coater, where the vacuum pulled through the chuck would bend the wafer enough to crack it and leave a mess of shattered of material. The solution to this issue was to replace the O-ring sealed chuck with a flat, metal only chuck. Though it seems trivial, the O-ring seal led to the destruction of several expensive 3" GaSb wafers.

The next challenge was delamination of both the anode and cathode contact after photoresist lift-off. The cause of delamination remains unknown, due to the difficulty of reproducing the problem, and inconsistent results. Initially the anode and wet etch lithography was done with NR9-1500py negative resist using RD6 for 10 seconds to develop. However once delamination and photoresist yield were found to be issues, AZ 5214E was chosen as the photoresist, providing better results. The recipe was also changed to start with an oxygen reactive ion etching (RIE) step prior to spinning to help ensure metal contact by removing any organic material on the wafers surface. On top of that, the titanium layer thickness was increased from 5 nm to 7 nm, because the titanium acts as an adhesion between the GaSb surface and the silver or gold.

Etch rate consistency was also an issue, because having the same depth in the material was critical for flip chip bonding as well as efficient light output across the wafer. It is desirable to etch deep enough to ensure the electrical current pass through all 16 LED stages. However, etching too deep can cause an undercut of the anode contact through the lateral etching, leading to delamination of the anode contact. An example of the etch undercut is shown with SEM in figure 14.

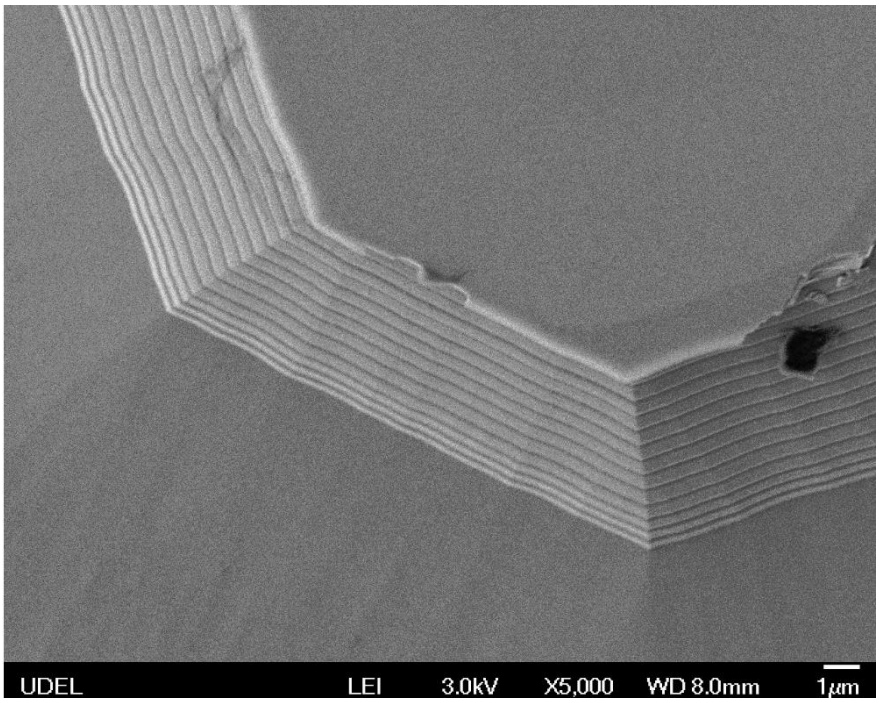

Figure 14 Corner of SLEDs emitter layers topped with gold anode contact after wet etching. The wet etch undercuts the anode contact, causing delamination in some cases.

To help guarantee the accuracy of the etch timing, two large "etch windows" were added to the photolithography mask, off to the side of the arrays. These windows, would allow the viewer to clearly see the LED layers being etched away, especially with the help of a zoomed-in camera. Once the last layers were removed, the proper depth 4.24 μm had been reached. The etch windows were successful in giving a visible indication of etch rate, but only at their location on the outer edge of the wafer. After inspection of early test wafers, it was clear that there was a disparity in the edge depth across different regions. To help correct this non-uniformity, a simple magnetic stirrer was added to stir the etchant.

Finally, looking back at figure 12, the strange bowl shape at the top of the cathode contact seems to be problematic at first. This shape is caused by the thick photoresist layer having sloped sidewalls, leaving metal depositions that match the bowl shape that is formed. This "bowl" was finally judged to be a non-issue, and even possibly beneficial as indium bumps would be placed inside the bowls for flip-chip bonding and the extra metal would be crushed away.

Project Results

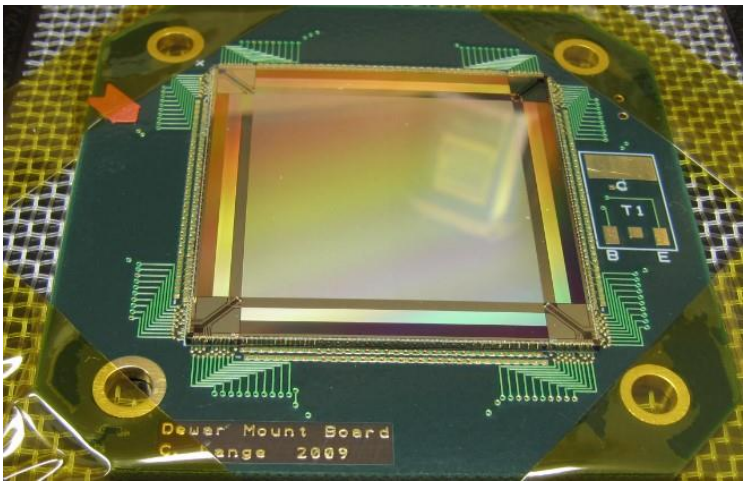

Figure 15 Mounted hybrid from Teledyne Scientific Co. The gold area in the center is the pixel array, about 2.45 cm long per side. Outside the array are address selection circuitry and wire-bond pads, making for a 3.3 x 3.3 cm hybrid. Wire-bonds connect the hybrid along the darker edges to the green PCB.

Once finished processing, a completed wafer would be sent to Teledyne Scientific Co. for hybridization. The RIICs chosen for hybridization were tested at the University of Delaware using probe cards with probes contacting the outer pads to

determine which had the most operating pixels and the best I-V curves. The mating SLEDs chips were chosen by visual inspection for the least amount of processing defects. The rest of the hybridization process included dicing the SLEDs wafer to cut the chips out, indium bumping and flip-chip bonding to the RIIC. After flip-chip bonding, the back of the hybrid was cut down to 50 μm total thickness using a mechanical fly cutter to sweep across the array at the perfect height and mill away extra material [27]. After fly cutting, an anti-reflective coating was put on the emitting backside to increase light extraction. The hybrid was wire-bonded to a PCB with a hole cut out of the middle to allow a metal stack-up to thermally contact the bottom of the chip. The hybrid on its PCB was then sent back to University of Delaware to be mounted in a cryostat dewar for operation and testing. Figure 15 shows a finished wire-bonded hybrid on its PCB.

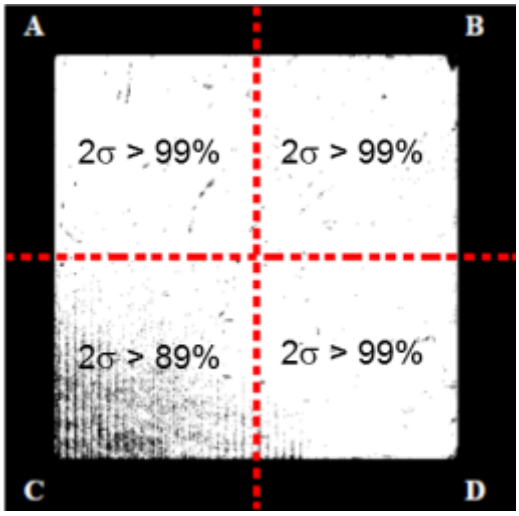

Figure 16 Yield map of a SLEDs hybrid, showing 512 x 512 pixels at a 48 μm pitch. Three of the quadrants have over a 99% yield while the bottom left has 89%, possibly due to poor adhesion during flip-chip bonding.

The results of processing several 3” wafers led to the yield of one successful SLEDs wafer, with four 2.45 x 2.45 cm arrays. The arrays on this wafer were used to create three 3.3 x 3.3 cm SLEDs hybrid chips, which were used in a functional, 100 Hz SLEDs system. The array had a pixel yield greater than 99%, and, when cooled to 77 K, could emit at an apparent temperature of 1370 K in the 3-5 μm band [27]. The SLEDs system was the first 512 x 512 IRLED flip-chip bonded array and system. A visual map of the hybrid yield is shown in figure 16.

System Description

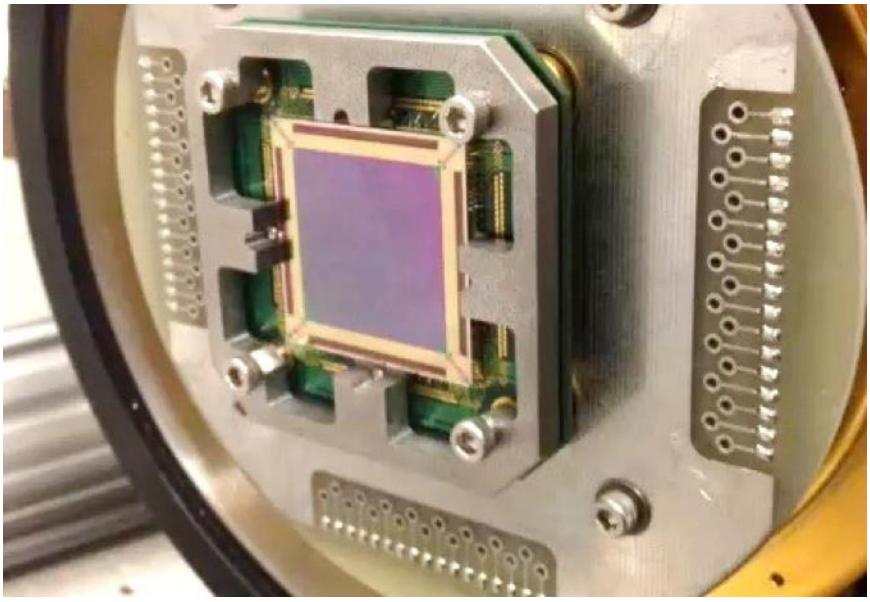

Figure 17 Hybrid chip clamped down and screwed into dewar. The green PCB has metal pads on the bottom side, where electrical spring contacts are aligned beneath. The PCB is clamped down, electrically connecting the PCB to the dewar, and IDE cables connect to the back of the dewar.

A finished SLEDs hybrid is shown in figure 17, where the board and hybrid are mounted into a cryostat dewar with the front opened. Figure 18 shows the closed Dewar, along with an open custom support electronics (CSE) case displaying the electronic PCBs and cables needed to drive the system.

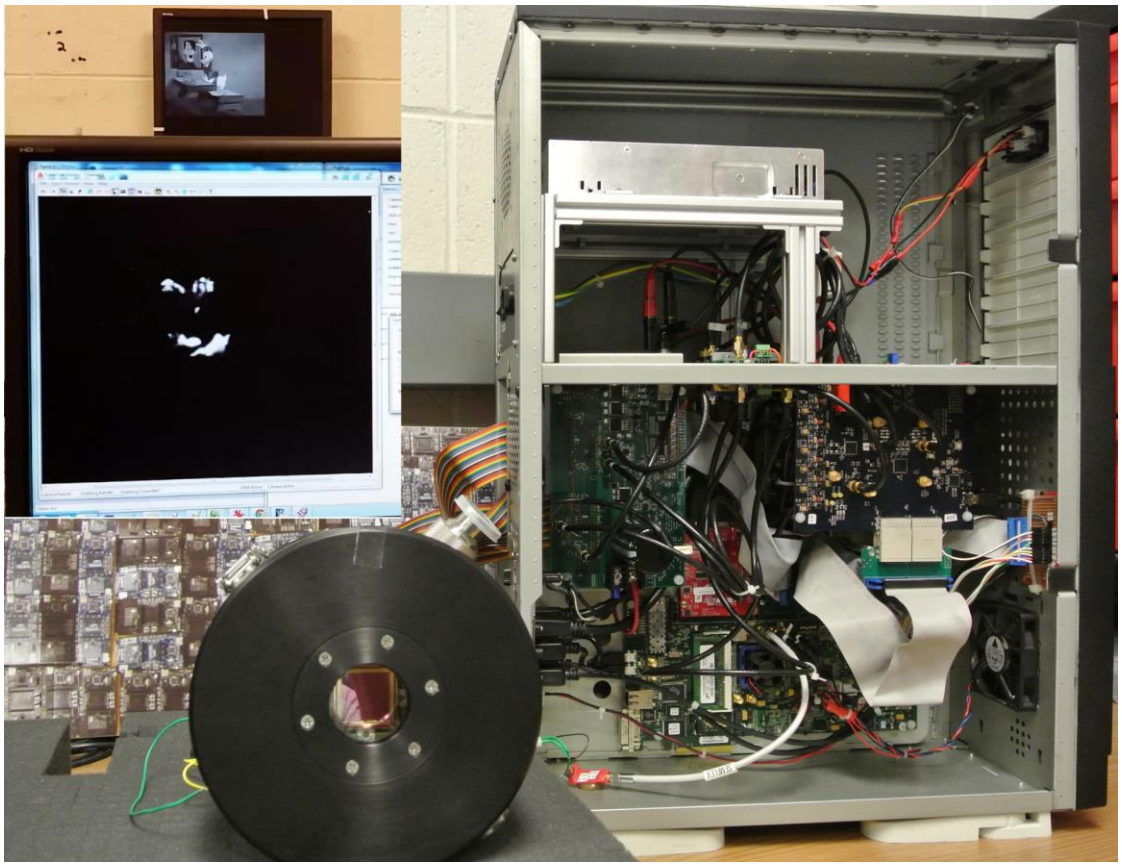

Figure 18 SLEDs chip mounted in hybrid. The smaller screen in the top left shows the original video to be replicated, and the larger screen shows the processed output sent to the array. The open computer case houses the custom support electronics (CSE).

Figure 19 is a block diagram of the SLEDs array and CSE system. An image is sent via digital video interface (DVI) to a field programmable gate array (FPGA) that sends digital signals to a DAC. The output analog signals are then amplified, and sent through an interface board to the dewar. The data is divided into four quadrants, and an output monitor visibly shows the user the image that is being sent from the FPGA to the array. The output monitor is a result of image processing on the FPGA, and is not the array's infrared output reading.

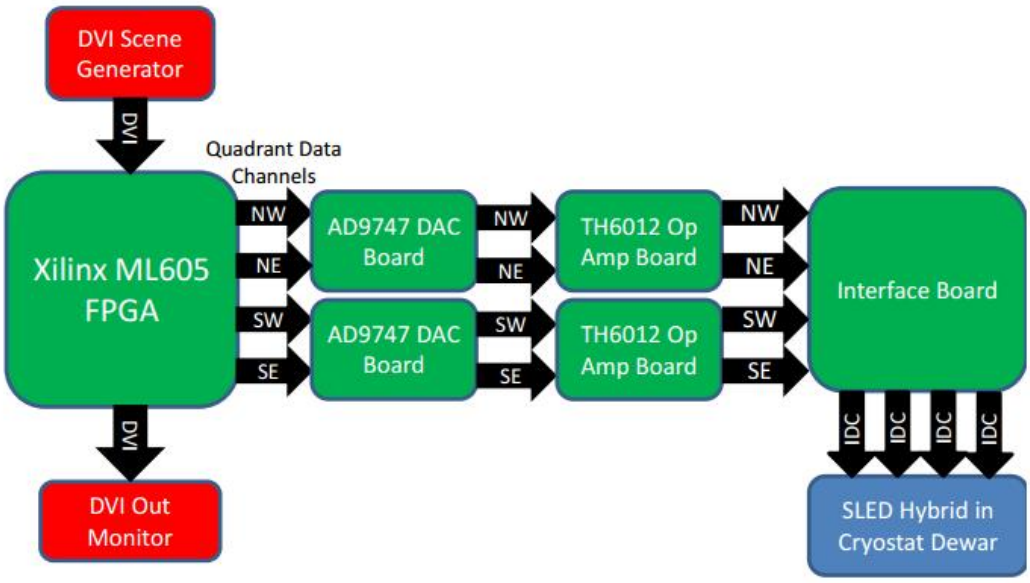

Figure 19 Block diagram of SLEDs CSE. The FPGA drives the array through a DAC and amplifier.

When connected, the CSE was able to display video, as shown on the screen in figure 18. Despite being a full cartoon image with background, only the brightest spots are displayed on the video. This output is because after non-uniformity

correction (NUC), the dynamic range of display is limited, leaving the dim background black [31]. Figure 20 shows an IR camera's reading of the pixel array, where pixels have been lit to show the dynamic range of brightness after NUC.

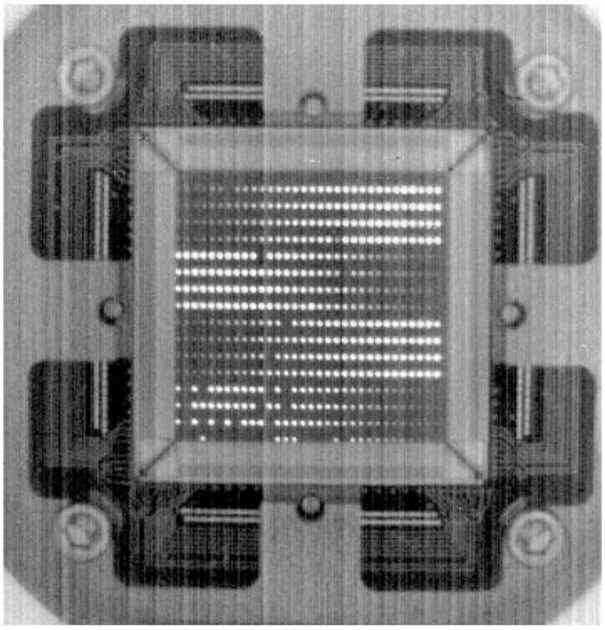

Figure 20 Pixel array viewed by an IR camera. The brightness varies across each row to show dynamic range after NUC.

Future Challenges

While there were several improvements to be made in the future generations of SLEDs chips, two of the biggest issues will be discussed here. The first significant problem with the array was a lack of ability to show very bright (or hot) objects with good dynamic range and very dim (or cool) objects using the same pixel and drive transistor [31]. The current coming from the drive transistor in the RIIC could be well modulated at the levels needed for higher apparent temperature, but then it was

impossible to control at the lower levels. The lack of dynamic range is attributed to the CMOS RIIC's drive transistor. The solution to this dynamic range problem is discussed in chapter 2.

The second problem was that as the pixels were left on, the efficiency of the light output decreased due to an increase in temperature (or build of up heat) [27]. There were several solutions proposed to fix the thermal problem. The BCS used to attach the hybrid to its plate is designed for detectors, where thermal issues are not nearly as significant [31], meaning its thermal conductivity could be low and still remove any small amount of heat from the detector array. A different means of attaching could decrease thermal resistance between the array and liquid nitrogen held in the dewar. Beyond improving the attachment method, increasing light extraction from the array removes heat caused by the light's reabsorption. This extraction is increased by altering the smooth, highly reflective surface on the emitter side, mitigating the reflection of light back into the hybrid. Some options for this solution are discussed in chapter 3.

Chapter 2

READ-IN INTEGRATED CIRCUIT CHARACTERIZATION

In order to show the IRLED technology would develop into the state of the art, the next generations of SLEDs technologies needed improvement. Generally, the goal for these microdisplays is to create them with as high a framerate and resolution as possible. Adding different output wavelengths is also desirable. To take the next step after the first SLEDs IRSP system, the next systems would split into two projects that improved the microdisplays in two different ways: one adds another wavelength to each pixel, and one quadruples the resolution.

The first design was the "Two Color SLEDs Array" (TCSA), a project whose goal was to create a 512 x 512, 48 μm pitch pixel array with two emitters per pixel, at two different IR wavelengths, which meant creating a pixel with two sets of drive circuitry and two stacks of superlattice layers. The layers would be grown at different thicknesses to engineer different wavelength emissions [2].

The second design was originally titled "Nightglow Superlattice Light Emitting Diodes" (NSLEDs), because the original design was to have it be a short wave infrared (SWIR) emitter, and the weak emission of the upper atmosphere seen at night is in the SWIR spectrum. This design was changed to make the array another MWIR emitter, but the NSLEDs name was kept for the project. This emitter would have an improved RIIC design as well as an improved NSLEDs array chip process to allow for a 1024 x 1024 pixel resolution in the same chip area, meaning the 48 μm pixel pitch of the SLEDs design was reduced to a 24 μm pitch for NSLEDs. This

resolution increase was considered to be an important step in reaching the eventual goal of these projects: creating a 2048 x 2048 pixel IRSP system.

These projects create huge challenges on both sides of the hybrid chip. The processing for an array of 24 μm pitch becomes much more difficult as feature sizes decrease and two etches are needed for TCSA to reach the proper depths in the superlattice layers. On the RIIC side, the same pixel circuitry that drove the original SLEDs array must be enhanced and shrunk at the same time to accommodate the new IRSP design. Improvements must also be made to solve the dynamic range problem of the SLEDs system. To improve future RIIC design, being able to model and understand transistor and circuit performance at both room temperature and 77 K is vital because the IRSP systems are intended for testing and use at both temperatures. This chapter will discuss the designs for the pixels and focus on the adaptations made for the RIIC and testing their circuitry.

SLEDs RIIC

While a read-out integrated circuit (ROIC) is mated to a photodetector array to read out the photon count absorbed by it, a read-in integrated (RIIC) circuit mates to an emitter allowing the user to control the current through the LEDs. The RIIC for SLEDs has a two dimensional array in the center with metal pads matching the metal contacts of the SLEDs array chip to facilitate indium bump bonding. Under these metal contacts, each pixel has an identical circuit to drive its LED. A sample of a 120 x 120 μm RIIC pixel is shown in figure 21. A voltage signal goes through a pixel selection circuit (giving the x and y location of the pixel) to the gate of a drive transistor sending current through the LED. In sensors, the ROIC pixel size has been

scaled down to a few microns, but for a RIIC pixel, scaling down is more challenging because of the high voltage and current drive requirements of the transistors.

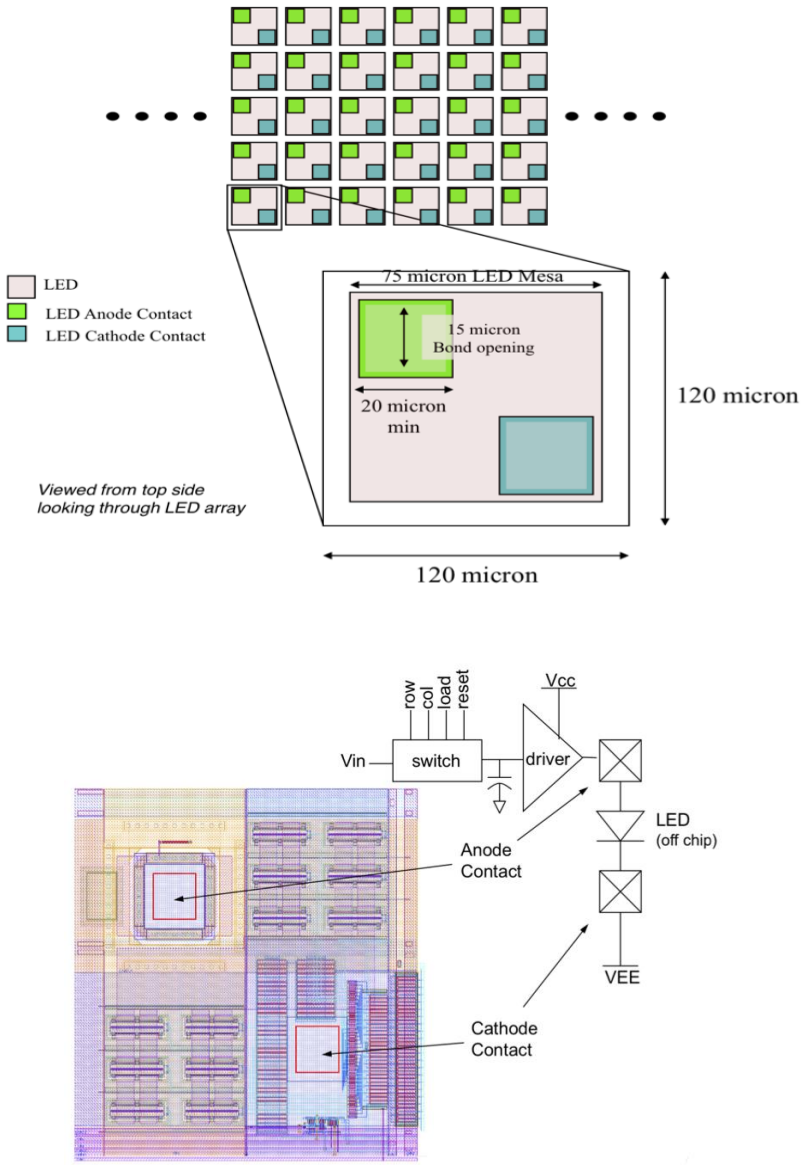

Figure 21 Sample of 120 μm pixel pitch RIIC. The top shows the metal pads for anode and cathode connections. The bottom shows the layout and the block diagram of the circuit.

The original SLEDs layout is show in figure 22. In the large red center square, the 512 x 512 array occupies a majority of the space. Outside the center square, colored purple and pink, address decoding circuitry and wire-bond pads complete the layout. A blown up pixel is shown within, where corresponding elements of the circuit diagram in figure 23 are circled in different colors. The transmission gate circled in blue will pass the analog 0-5 V control signal when the x and y coordinate of the pixel are selected. The analog control signal connects to the gate of the PMOS drive transistor circled in green, and modulates its drain current to power the SLED. This drive transistor occupies about 80% of the space. A monitor control circled in red allows for the voltage across the SLED to be read through an external pin during operation. The monitor contains two PMOS transistors for the x and y selection signals. The monitor would ideally have NMOS transistors as well to form the same transmission gate, but limited space did not permit for this. Most of the 48 x 48 μm space is then occupied by necessary circuitry, leaving no room to add additional functionality, or shrink down to a 24 μm pitch.

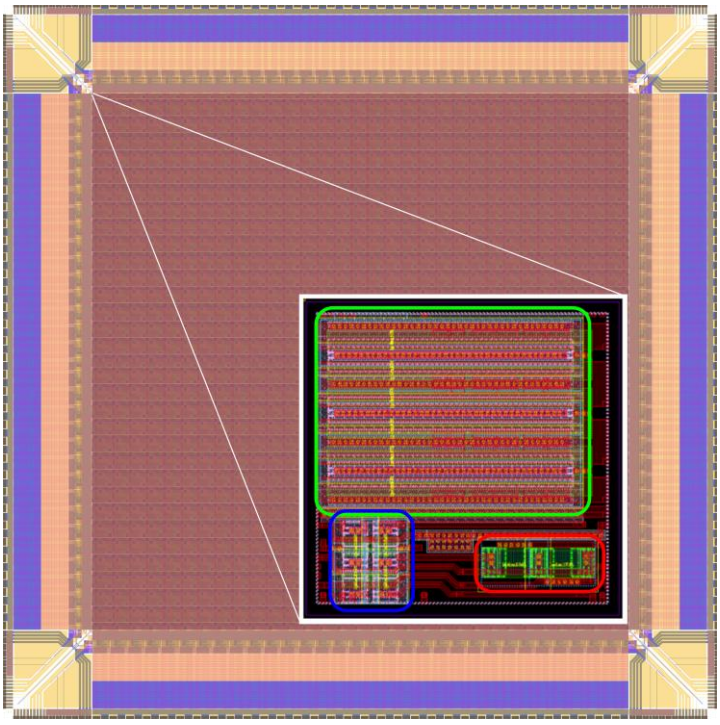

Figure 22 Layout of SLEDs RIIC. The large central region is a 512 x 512 array of pixels, and the periphery is address decoding circuitry and wire-bond pads. The enlargement shows a single pixel layout, with its matching circuit diagram shown in figure 23.

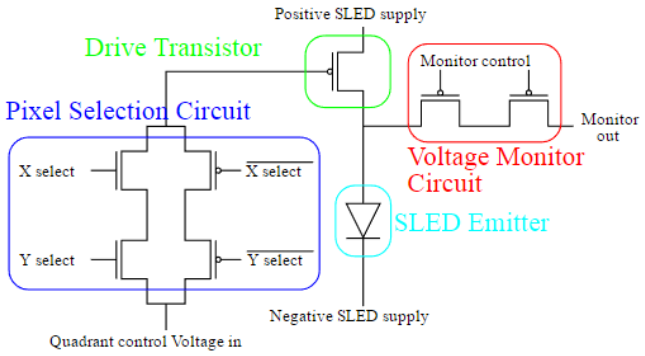

Figure 23 Circuit diagram of the pixel. The colored circles match the layout image. The pixel selection circuitry allows the control voltage to modulate the drive transistor's gate when turned on. The drive transistor pushes current through the SLED emitter. The voltage monitor reads out the voltage across the SLED.

TCSA and Initial RIIC Improvements

The TCSA emitter chip design is diagrammed and shown in figure 24 [32]. Here there are three levels of contact on the array, with all metal contacts coming up to the top. This layout avoids the requirement of a long metal deposition. The first anode contact for the first wavelength of emission is connected to the top set of superlattices. When this anode is electrified, the cathode, which extends to the middle step between them and is electrically isolated from the top GaSb surface with an oxide layer, will pull current through the top layers. The second anode, which is electrically isolated from the top GaSb surface and connected to the bottom substrate, will drive current through the bottom set of superlattices when turned on. This design allows for practical two-color emission [32].

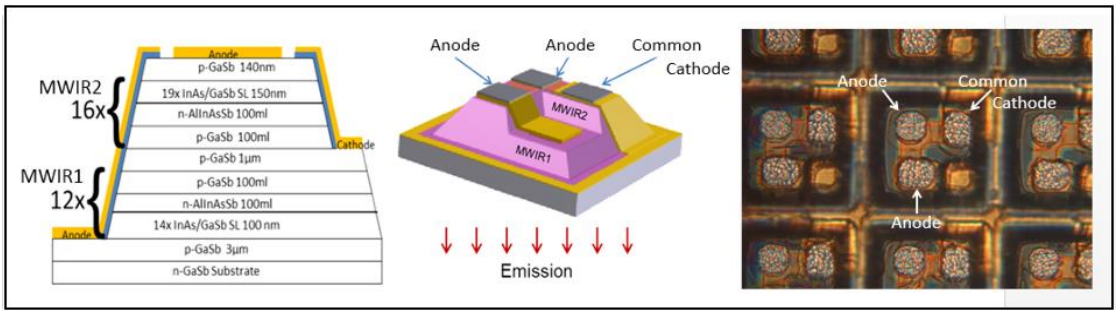

Figure 24 TCSA emitter chip SLED layers on the left. A diagram of the processing is in the middle. A picture of the results of processing is on the right. The three contacts allows for emission at two different wavelengths.

Changing Transistors

The TCSA pixel design requires the RIIC to have more drive transistors that will not fit using the same design as the first SLEDs microdisplay. However, the first microdisplay had all the SLED cathodes connected, meaning the drive transistor connected to the anode had to be PMOS to push current through the SLED from the anode side. This design choice creates an opportunity for improvement in subsequent generations, because NMOS transistors have better carrier mobility as free electrons can move faster than free holes. This mobility difference makes the PMOS transistors occupy four times more space their NMOS equivalent to generate the same current [33]. Additionally, PMOS transistors require the region under their layout have n-type doping (an n-well), making for an extra 10-20% increase in space requirement. By changing the circuit design to have NMOS transistors pulling current through the SLED from the cathode side, a much larger area was freed up in the RIIC pixel.

To improve space efficiency further, it was thought that standard cell transistors in the AMIS C5N 0.5 µm [34] process might be reduced in size beyond the recommended minimum channel length. In order to test this theory, the new transistor

layout was designed with shorter gate lengths. To test the effectiveness of reducing standard cell transistor size beyond the recommended limits, a test chip was fabricated with several reduced channel length versions of the high voltage transistors. Transistor drain currents increased with decreasing gate lengths. The transistors operated well all the way down to 2 microns, which was the minimum gate length tested. This change to non-standard transistors made testing the pixel circuits even more important because the functionality of these transistors in a circuit was unknown.

Improving Dynamic Range

The limited dynamic range discussed at the end of chapter 1 comes from a single drive transistor being responsible for not only the brightest spots but also the dimmer background [31]. A few milliamps of current are required for the SLEDs to replicate very hot objects near the top of its brightness range, but for dim backgrounds around 300 K, only a few microamps are required. These microamp currents are down at the "knee" of a transistor's I-V curve, making modulation using the gate voltage nearly impossible.

One way to add dynamic range was to add multiple drive transistors [1]. To start as a simple step in the TCSA and NSLEDs systems, a simple dual-drive transistor design, one strong and one weak (in terms of output current) was implemented. In TCSA, the strong drive transistor was 42 μm and wide with a gate length of 2 μm. The weak drive in TCSA was two transistors setup in cascode. The first transistor was 4 μm wide with a 2.5 μm gate length, with its source connected to the drain of the second transistor. The second transistor had a width of 0.8 μm and a gate length of 3 μm. In NSLEDs, the strong drive transistor was 18 μm wide with a gate length of 2 μm, while the weak transistor was 4 μm wide with a 2.4 μm gate length. The strong

drive transistor would be used to show very bright spots and the weak drive transistor would be used show dimmer areas. In figure 25, this dual-drive concept is illustrated with simulated log-linear I-V curves of each transistor. The strong transistor's curve is more linear above 1 mA and the weak transistor's curve is more linear above 1 μA [1].

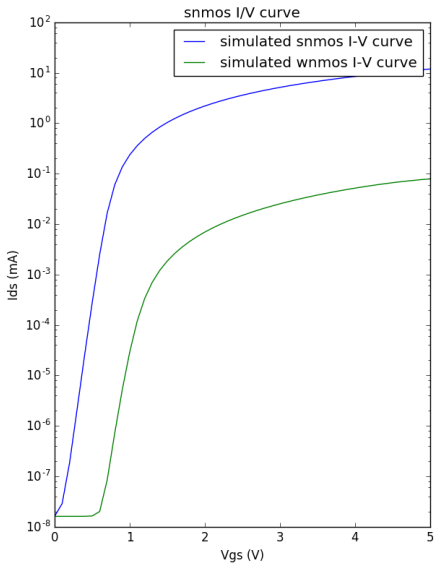

Figure 25 Simulated log-linear plot of a strong and weak transistor's drain current vs. gate voltage. The strong transistor can easily modulate the mA output while the weak transistor can easily modulate the μA output using the gate voltage [1].

The TCSA hybrid circuit diagram is shown in figure 25. Each LED has a pair of drive transistors as planned. If the top transistors are fully off, the strong or weak transistor at the bottom will act as a current source pulling all of the current through the red LED. If the top transistors are fully on, they themselves will act as a current source, pushing current through the blue LED and providing all of the current for the

bottom transistor. By modulating the gate voltage then on the top transistor, some fraction of the current will go through the red LED and some through the blue LED, allowing for simultaneous operation. Testing the strong and weak transistor current output at room temperature and 77 K would help correction of temperature effects during operation and future RIIC design by providing real data to compare with simulation.

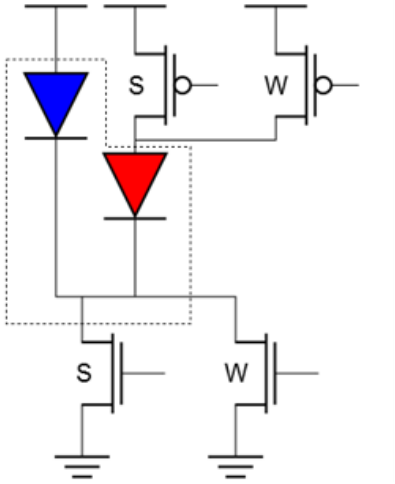

Figure 26 Circuit diagram of the TCSA hybrid. The "S" and "W" stand for strong and weak drive transistors, respectively. The top transistors drive current into the blue LED and the bottom transistors pull current for both LEDs.

NSLEDS and Future Scaling

Scaling and Yield

Reducing the pixel size was critical not only for NSLEDs, but for future IRSP systems, because two following IRLED array projects have a resolution goal of 2048 x 2048 pixels, making a decreased pixel pitch absolutely necessary because of yield

issues as explained below [35-37]. The yield of silicon chips limits the size of the RIIC from a cost efficiency perspective [33]. To explain, the first SLEDs RIIC was designed for a 512 x 512, 48 μm pixel pitch array and had a die size of 3.3 cm x 3.3 cm, or 10.89 cm^2. This die size put 16 chips on an eight inch silicon wafer and the returned yield was about 90%. Using a simple Poisson yield model:

$$Y = e^{-A*D}, \tag{2.1}$$

where Y is yield, A is chip area, and D is defect density, equation 2.1 solves for a defect density of roughly 0.01 cm^{-2}. If the same 48 μm pixel pitch is scaled to a 2048 x 2048 pixel resolution, the die size becomes at least 10 cm x 10 cm or 100 cm^2, placing only a single chip on the eight inch wafer. The same defect density of 0.01 cm^{-2} then gives an expected yield of 36.8%. A single defect ruins an entire wafer's yield, making the process extremely expensive. Further, processing the LEDs becomes nearly impossible, because it requires at least an eight inch GaSb wafer and perfect feature alignment across it. Building the system becomes much more difficult as well because the packaging must accommodate a huge hybrid, forcing it to include a cryostat with a large chamber, window and PCB for mounting. For the reasons given above, scaling down the pixel pitch to 24 μm was considered necessary, not only for NSLEDs but for future IRSP systems.

Shared Transistor Layout

The transistor changes discussed were still not enough to create a single RIIC pixel layout at a 24 μm pitch because the PMOS and NMOS drive transistors occupied too much space. Again, scaling down the 48 μm pixel pitch to 24 μm, as well as increasing the number of drive transistors, created a spatial layout problem. This problem led to an innovation for NSLEDs that would group pixel components for

more efficient layout. Figure 26 shows the NSLEDs test pixel layout, where a 96 μm x 24 μm area matches to four LED pixels.

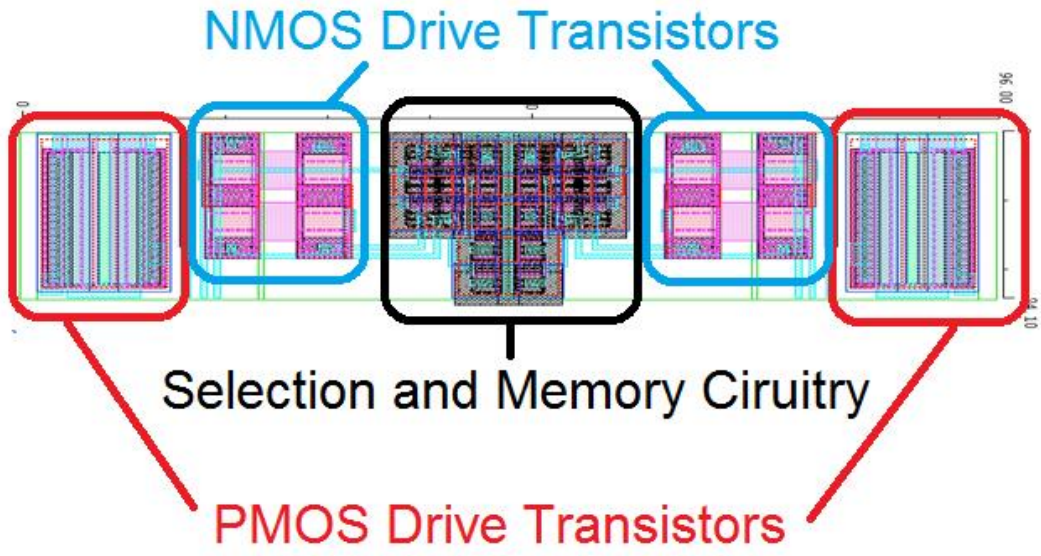

Figure 27 The NSLEDs test pixel layout. Grouping of common elements for four LED pixels allows for a much more efficient layout. Both weak and strong PMOS and NMOS transistors occupy the same spaces containing enough circuitry for four SLED pixels.

By grouping four pixels into one panel 96 μm x 24 μm in size, high voltage and low voltage transistors were able to share space, as well as PMOS and NMOS transistors, reducing overall well sizes. This novel "shared transistor" layout made possible a final 24 μm pixel pitch on the array. The final layout had a shared 2 x 2 pixel layout, rather than a 4 x 1 pixel layout in the test pixel. The shared transistor allowed for the development of the NSLEDs microdisplay, and was a large step on the path to the future of LED IRSP systems.

Testing

Characterizing the transistors for the TCSA and NSLEDs RIIC required the manufacturing of test chips. These chips would include individual transistors as well as RIIC pixel circuitry with the necessary inputs and outputs. The setup would need to allow for cryogenic cycling, where 77 K performance could be verified. The experimental devices were packaged in LCC84M ceramic packages from MOSIS [38]. These packages were flat with 84 metal pin pads on the bottom side. This package would be clamped down to the inside of the cryostat dewar, contacting its 84 pins to the dewar's metal electrical contacts. The signals were then routed through the dewar to pins outside of its vacuum chamber.

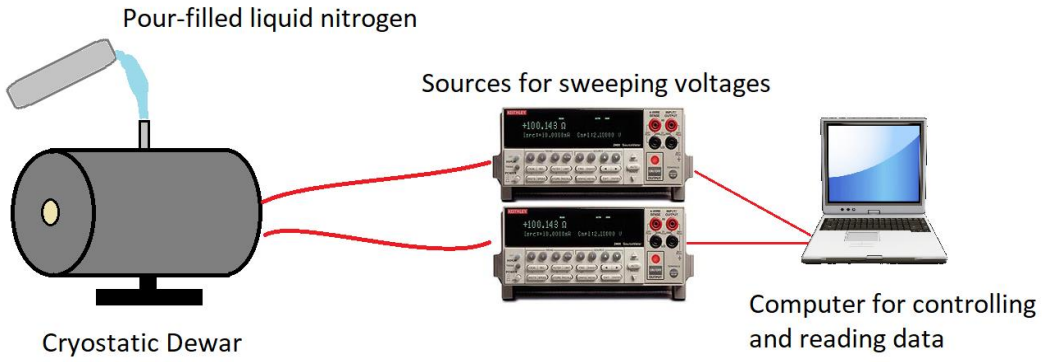

Figure 28 Test setup allowing for temperature cycling while two dimensionally sweeping the transistor voltages and reading current. The test chips are mounted in a pour-filled dewar for low temperature readings.

Two Keithley 2400 source meters were then wired to pins in the back of the dewar. Using RS-232 serial control, the Keithleys were programmed to quickly sweep the gate and drain voltage, and read the drain current. This sweep would generate several I-V curves of the unloaded drive transistor's drain current vs. drain voltage at

different gate voltages. A diagram of the setup is show in figure 27. Because these circuits did not have electrostatic discharge (ESD) protection, it was important to take care in grounding everything to prevent destroying the circuits with high voltage "shocks." This lack of ESD protection caused the failure of many chips during testing. The final NSLEDs and TCSA RIICs had built in ESD protection, so grounding was not an issue while evaluating fully fabricated devices.

Results

Characterization Results

The TCSA and NSLEDs pixels had 4 drive transistors that needed testing: one strong NMOS, one weak NMOS, one strong PMOS, and one weak PMOS. Beyond the transistors, the two novel pixel layouts were tested to show proper operation, with expected levels of current from strong and weak transistors. In this dissertation, only the TCSA pixel circuit is discussed. All tested pixels and transistors showed an increase in current magnitude at 77 K versus room temperature, due to an increase in carrier mobility caused by a decrease in lattice scattering [39-40]. To test pixels, all necessary pixel inputs including digital selection signals and bias voltages were fed into the pixel circuit, and the output drain current was measured either from the strong or weak drive transistor. The setup essentially placed a current reader where the LED would connect in a hybrid. For the transistors, the gate, source, drain and bulk were connected to their appropriate sources or ground. All PMOS outputs show a reverse current as current flows form source to drain.

The threshold voltage V_T in a transistor describes the voltage difference between the gate and source needed for a current channel to form at the surface of the

transistor material just under the gate [41]. The TCSA pixel's PMOS output transistor gates are connected in cascode to an NMOS transistor acting as a current source, shown in figure 29. The analog voltage level provided to the pixel connects to this NMOS transistors gate. Finding V_T for the pixel circuit means finding the minimum input analog voltage that provides a non-zero drain current on the drive transistor of the pixel circuit, normally connected to the LED. Once drain current flows, it increases in a linear fashion with an increased drain voltage until that current reaches saturation. The drain voltage where the linear region ends and the saturation region begins is V_{Dsat} [42]. In all measurements shown, 50 steps were taken on the input voltage ranging between 0-5 V, meaning all estimated values of the pixel's V_T are only accurate to 0.1 V increments. In all measured pixel outputs, V_T increased at the lower 77 K temperature, as expected [40, 43].

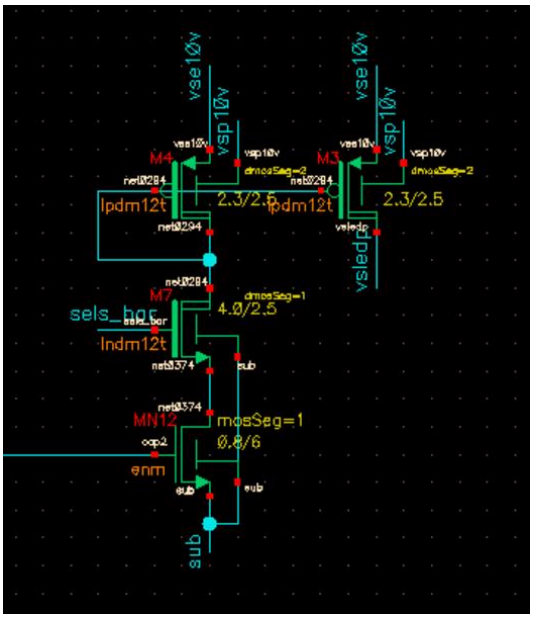

Figure 29 TCSA weak PMOS output transistor circuit. Analog voltage level comes in to the gate of the bottom NMOS transistor. The bottom two transistors act as a current source to modulate the gates of the PMOS current mirror on top, where vsledp is the connection to the LED anode.

Figure 30 shows the single pixel operation of the strong and weak TCSA NMOS drive transistor at 77 K. This is a sample of what was found for all NMOS and PMOS pixel drive operation: that the weak version of the transistor's drain current was about two orders of magnitude less than the strong. The pixel's V_T for the strong output is roughly 0.9 V, while for the weak output it is roughly 1.3 V. In addition, V_{Dsat} has a maximum of about 6 V for the strong output and about 2 V for the weak output.

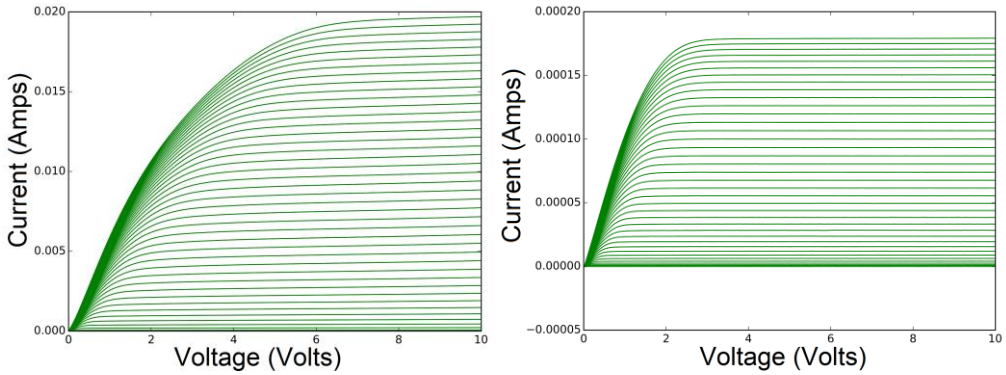

Figure 30 77 K operation of the strong (left) vs. weak (right) TCSA NMOS pixel operation. As designed, the strong NMOS drain current increases up to 20 mA, while the weak NMOS drain current is about two orders of magnitude less.

In figure 31, the TCSA strong PMOS pixel drive is shown for room temperature and 77 K. The maximum current magnitude increases from about 6.5 mA to close to about 11.8 mA when decreasing the temperature, a significant increase of about 81.5%. For the strong output, the pixel's V_T is roughly 0.8 V at room temperature, and roughly 1.2 V at 77 K.

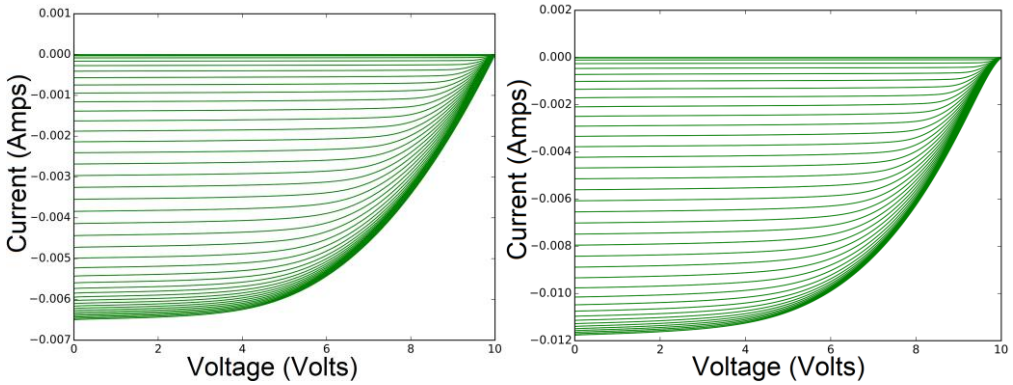

Figure 31 TCSA pixel operation of strong PMOS output at room temperature (left) and 77 K (right). Decreasing the temperature shows an 81.5% increase in current.

In the weak PMOS pixel output, shown in figure 32, the current jumps from about 57 μA to 135 μA, a 137% increase, showing a large difference between the weak and strong PMOS operation that needs accounting for during temperature correction modelling. For the weak output, the pixel's V_T is roughly 1 V at room temperature, and roughly 1.3 V at 77 K.

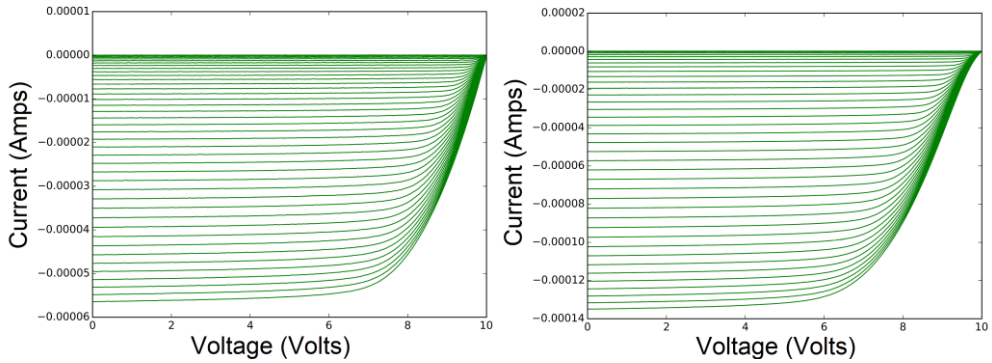

Figure 32 TCSA pixel operation of weak PMOS output at room temperature (left) and 77 K (right). Decreasing the temperature shows a 137% increase in current.

The sample of data presented confirms the temperature dependence of the RIIC pixel operation. The known shift in threshold voltage and drain current during operation will be useful for generating an advanced NUC that accounts for temperature dependence during operation by using a temperature sensing diode on the array itself [44]. The data captured provides the information needed by the system software to shift voltage input levels when operating at 77 K vs. room temperature. The Keithley sweeping code and data acquisition scripts provide the basis for future full temperature sweeping as well. The LED radiation also has a temperature dependence, because increasing the temperature from 77 K will decrease radiative recombination and increase Auger recombination. Understanding all temperature sensitive elements of the IRSP will help maintain a uniform output while the array operates.

Future Work

More complete characterization of the RIIC and its components is required for IRSP LED performance improvement. The first step is to complete the I-V curves for all pixel and drive transistor elements at room temperature and 77 K. The second step is to create a test setup to add temperature steps for the I-V curves to completely understand the RIIC's temperature dependence. The third step would be to measure individual pixel output on the IRSP array and factor in the temperature. Using all of the data described, a NUC that is sensitive to changing temperature can be integrated into the software responsible for modulating the input analog voltage. Lastly, modeling the transistors and full pixels in SPICE provides more accurate simulations for future RIIC design.

Chapter 3

LENSLETS FOR LIGHT EXTRACTION

Overview of Light Extraction Problem

As discussed before, overheating of the SLEDs array became a serious issue affecting the performance of the system. Because SLEDs are a new and undeveloped technology, their efficiency in converting electrical energy into light energy is still very low [27]. Ideally all electrons relaxing from the conduction to valence band will release energy in the form of photons. In reality, some portion of the energy is being lost as phonons in these devices, but the estimated internal quantum efficiency for these devices was about 70%. Despite this internal quantum efficiency, the external quantum efficiency was less than 1%, because once that light was emitted internally, it could then be reabsorbed before escaping the substrate. The well-known major contributor to the low external efficiency of IRLED devices is total internal reflection [45-46], where light emitted at a more lateral angle would reflect off the smooth back surface. There is also some Fresnel reflection that is to be expected at the refractive index boundary.

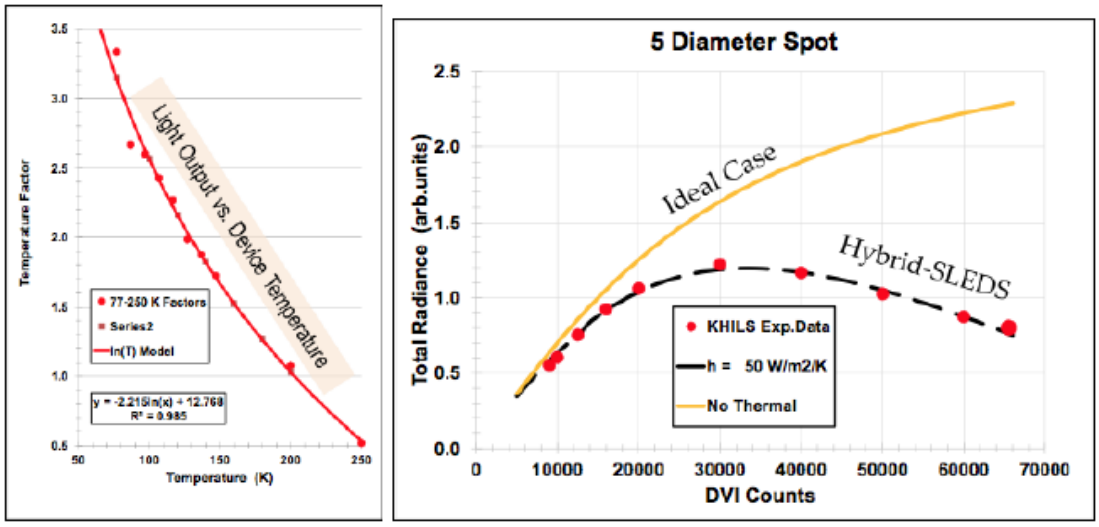

Figure 33 The graph on the left shows the device's light output declining as operating temperature is increased. This decline corresponds with the graph on the right, where increased current (DVI counts correspond to gate voltage on the SLED's drive transistor) is expected to increase device temperature and thus decrease total radiance.

This result of the problem is demonstrated in figure 33, where on the left the intensity of light output as read by an IR camera in one spot begins to decrease as time allows the pixel's thermal energy to build up. On the right side of figure 33, the orange line shows the ideal case of total radiance, whereas the SLEDs performance shows a decrease with increasing gate voltage on the drive transistor (DVI counts). Figure 34 shows that the greater the pixel area of operating pixels, the lower the emission intensity becomes due to greater concentration of heat. In figure 36, the light output decreases despite the DAC voltage and total current through the pixel increasing.

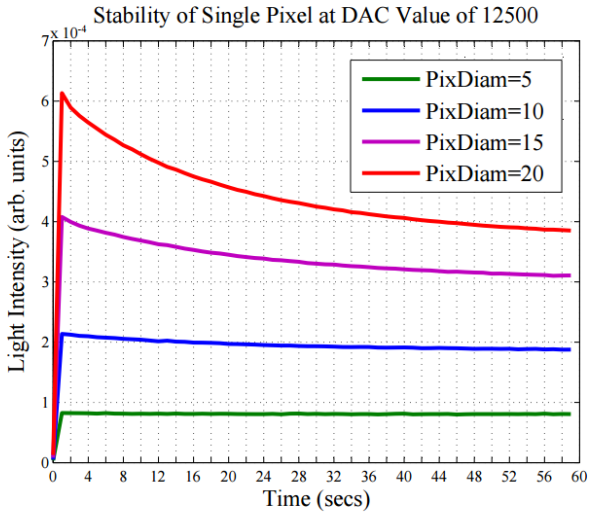

Figure 34 Light intensity vs. time for different spot sizes. As more adjacent pixels are operating, the worse the output over time.

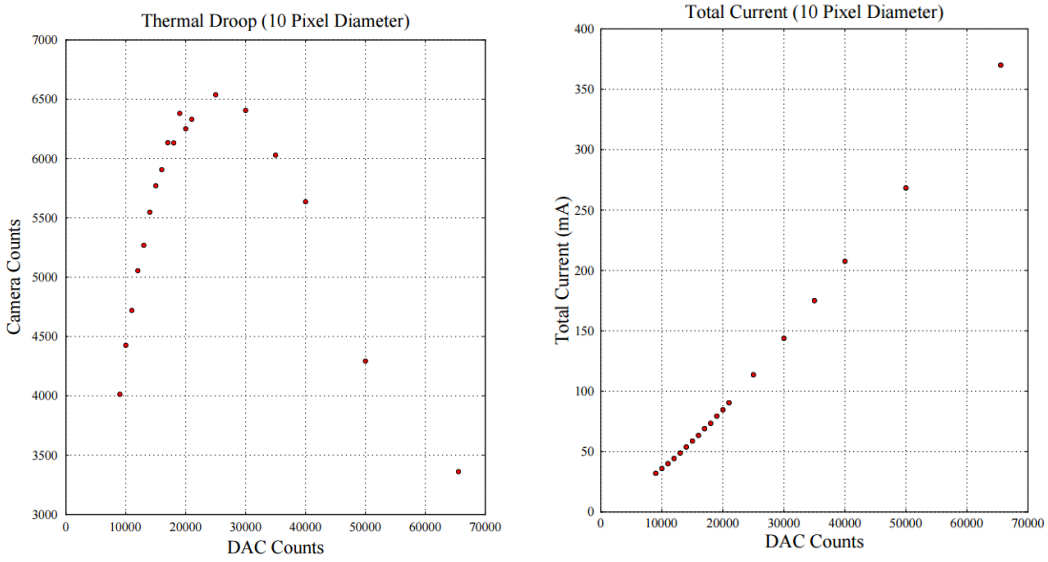

Figure 35 Light output on left as read by camera counts vs DAC counts (DAC counts correspond to analog voltage on the SLEDs drive transistor). At about 25,000 DAC counts, light output begins to decrease despite increasing current through the SLEDs pixel as shown on right.

The heat generated by reabsorbed light makes the SLED device's radiative recombination decrease. Also, the efficiency droop in LEDs is caused by other factors including Auger recombination and radiative recombination saturation that are aggravated by low light extraction [47-50]. Because of this added burden of reflection, any incremental improvement in light extraction will have a greater impact improving performance. All areas of performance enhancement were considered, starting with removing the BCS and using a more thermally conductive medium [31]. In addition, a new cryostat design was implemented to allow for a more direct and stronger thermal connection between the hybrid and liquid nitrogen heat sink [51].

Addressing the light extraction on the back end of the emitter array, where total internal reflection was considered to be the largest thermal problem, surface roughening and surface patterning were investigated as a means of increasing efficiency. Surface roughening has increased light extraction on other LED systems [52-56]. Additionally, adding a cone shape has been shown to greatly improve light output [57-58]. Adding lenslets (small pixel sized lenses) to the emitting surface on an LED has also shown not only stronger light extraction, thereby improving thermal dissipation [59-60], but has also decreased the angle of emission [61] and improved coupling [62].

Adding lenslets to the back side of the emitter as shown in figures 36 and 37 would not only decrease the reflection of the emitted light, but would also help focus more light coming from each pixel to a smaller target. This focusing is beneficial for a microdisplay system leading to a sharper display from the perspective of the target optics. Understanding the benefits of using lenslets would start with developing recipes to show what kind of lens shapes are achievable in the relevant materials.

Lens shapes in GaSb were investigated as GaSb was the SLEDs material in the existing hybrids. Although much has been done in terms of etching III-V materials including GaSb [63-69], it is difficult to find much on GaSb pattern transfer. Papis et al. developed GaSb lens shapes using various methods, including argon and oxygen ICP etching [70], but attempted replication showed no GaSb etching using a similar gas chemistry. Because of the lack of useful information, a series of experiments was planned to develop an etch recipe for creating GaSb lenslets.

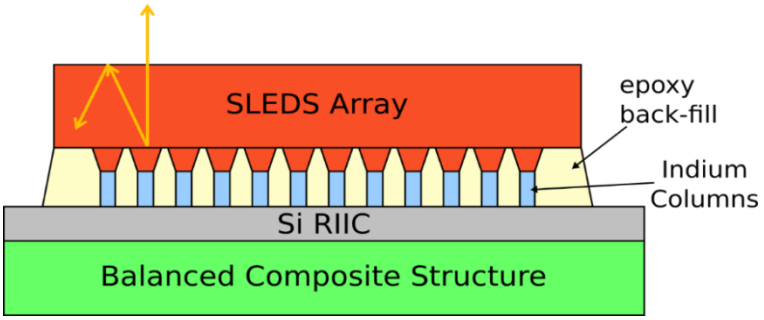

Figure 36 LEDs emit light where much is reabsorbed due to total internal reflection.

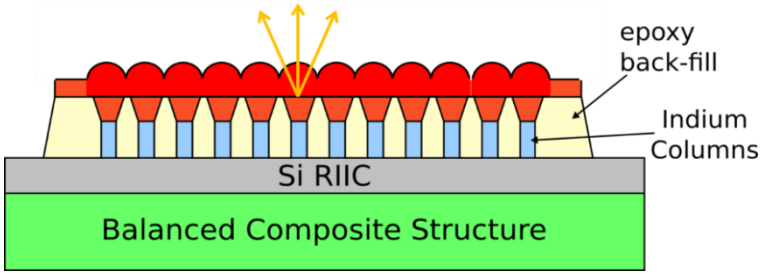

Figure 37 LEDs with lenslet shape etched into the surface have stronger light extraction and focus light from a pixel through its lens.

Photoresist Reflow for Forming Lenslet Shape

Developing a recipe for patterning the lens shape in photoresist was the first goal of this investigation. To make a large lens shape, a photoresist that could leave a thick layer would be preferable as a starting point. The photoresist shape can be changed with thermal reflow [70-79]. While the photoresist is removed by physical plasma bombardment, its etch rate may not be fast enough. If the etch rate is indeed not fast enough, adding oxygen to the gas chemistry would increase it, as the oxygen plasma removes photoresist and other organic material from the surface of the semiconductor. The etch rate of the photoresist could then be altered by assuming it would increase or decrease with the oxygen flow rate [79].

Photolithography

The positive resist AZ 4620 was chosen for its thick layering and some previous experience with its recipes. For the material, 2" GaSb wafers were chosen to match most closely the bulk material for the applicable devices [27]. The wafer was spun at 3000 rpm and cleaned with AMI, with about 10 seconds for each solvent, and allowed ample time to dry. Once dry, the wafer was stopped and AZ 4620 was applied spiraling outwards until a thick layer covered the entire wafer to ensure good distribution. Then, the wafer was spun at 100 rpm for 10 seconds to slowly spread the photoresist. Immediately after that, the spin speed was increased to 1700 rpm for 20 seconds. Once coated, the wafer was soft baked at 110° C for 2 minutes. After soft baking, the wafer was left in its Fluoroware case with the lid slightly ajar to allow for the resist layer to rehydrate. It had to be ensured that it was not exposed to any high frequency visible or ultraviolet light during this time, as that would develop the positive resist.

To pattern the resist, the same repeating octagon shaped mask used for the SLEDs anode would be used as the basis for the reflowed lens. The resulting lens would be roughly the correct size for a 48 μm pitch LED array. The wafer pattern was exposed with 405 nm light at 275 W for 65 seconds. For development, a 1:3 mixture of AZ 400K:DI water was used until the pattern became visually clear. Development usually took about 80 seconds, immediately after which the wafer was rinsed with DI water for 2 minutes, and blow dried with nitrogen. After drying, the wafer was left again with the lid slightly ajar for 24 hours to allow any remaining water to evaporate.

Reflow

The dry, patterned wafer was then ready for the reflow of its photoresist into a lens-like shape. Before reflow, the photoresist thickness was measured at about 8-9 μm. There were two methods used for reflow. The first was a slow, steady heating of the wafer in a vacuum oven with the temperature finally reaching 180° C. Once temperature was reached, the wafer was left for 1 hour before removal from the oven and cool-down at room temperature. Due to the concern that this temperature could possibly be overheating the photoresist, the second method was to simply use a hotplate at 145° C for 5 minutes. The temperature, timing and hotplate use were chosen based on research of similar processes [76-78]. It was observed that baking at 180° C for 5 minutes versus 1 hour showed no noticeable difference in shape upon SEM inspection. In the same way, there were no noticeable photoresist shape differences for a hot plate set to 140° C or 145° C for times of 1, 3, 5 or 10 minutes.

Results of Photoresist Reflow

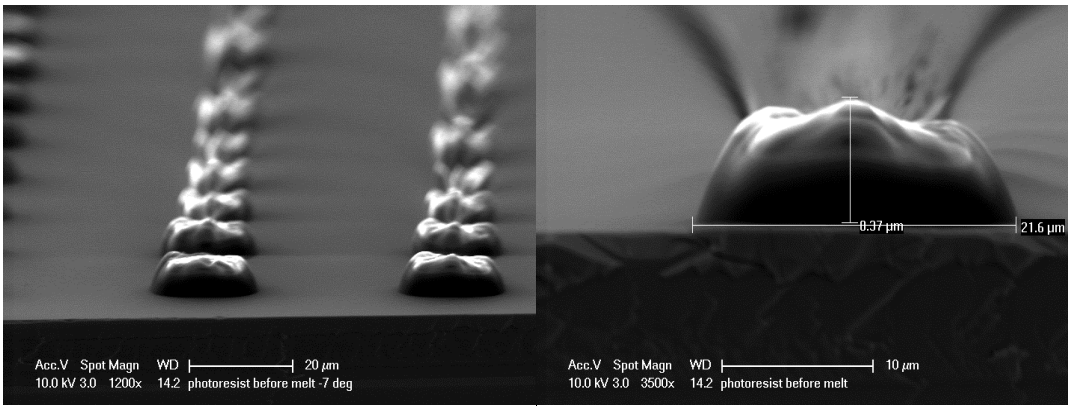

Figure 38 Photoresist pattern after lithography but before reflow.

The resulting photoresist after lithography are shown through scanning electron microscopy (SEM) in figure 38, where the height is non-uniform but averages around 8 µm tall. After reflow, the photoresist lens shape was about 12.7 µm tall, as shown in figure 39. For all SEM images of photoresist, the bright spots on top of it as well as the distortion around it are caused by electrons from the SEM's beam building up charge on the resist. Normally this charge would dissipate as in figure 40, but lingered without metal coating due to the low conductivity of the AZ 4620. During initial Zygo measurements of photoresist thickness, it was apparent that different areas of the same GaSb wafer had lenses of slightly varying height and width, due to the uneven distribution of resist thickness after spinning and development. The variance of photoresist thickness required that careful measurements take place before etching to set correct etch timings.

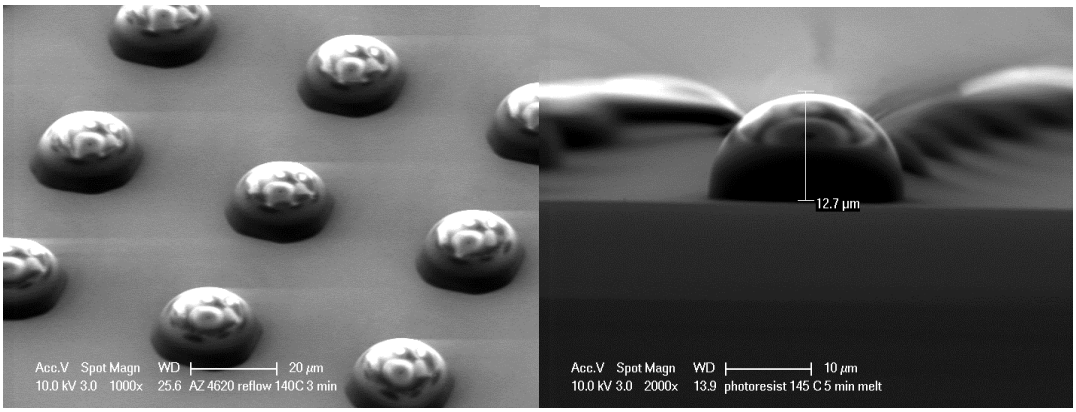

Figure 39 Photoresist lenslets after reflow.

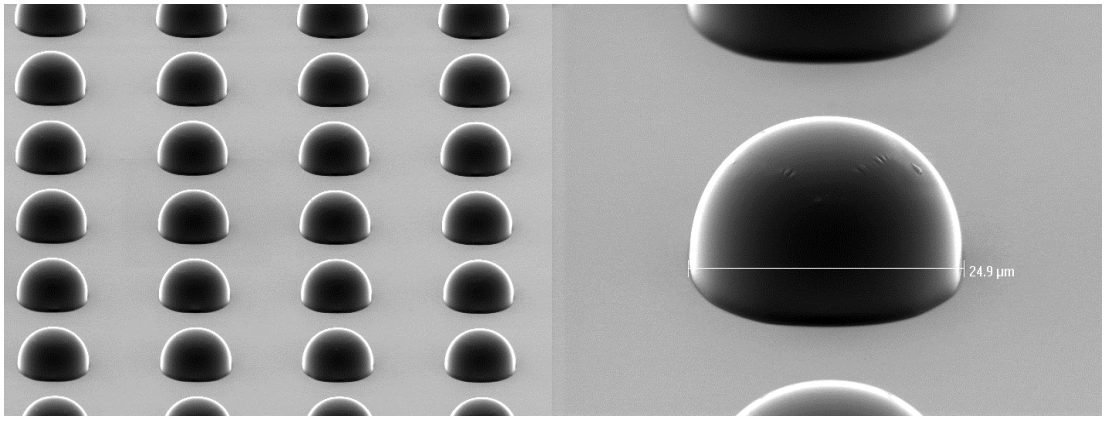

Figure 40 Photoresist lenslets coated in 50 nm of titanium using e-beam evaporation. Metal coating removes the charge build-up and distortion.

Reflow Recipe Change

In doing ICP etch experiments with these lenslets, it was observed that the photoresist lens pattern was being non-uniformly removed causing a strange etch pattern that resembled thick stems coming from the base of the lens. The resist peeling apart both after 10 and 45 minutes of the same recipe is shown in figure 41. The GaSb remaining after 90 minutes of etching is show in figure 42, where a bowl

like shape is formed due to the photoresist transfer failure. This failure led to a very fragmented and ruined GaSb lens that resembled more of a strange bowl shape.

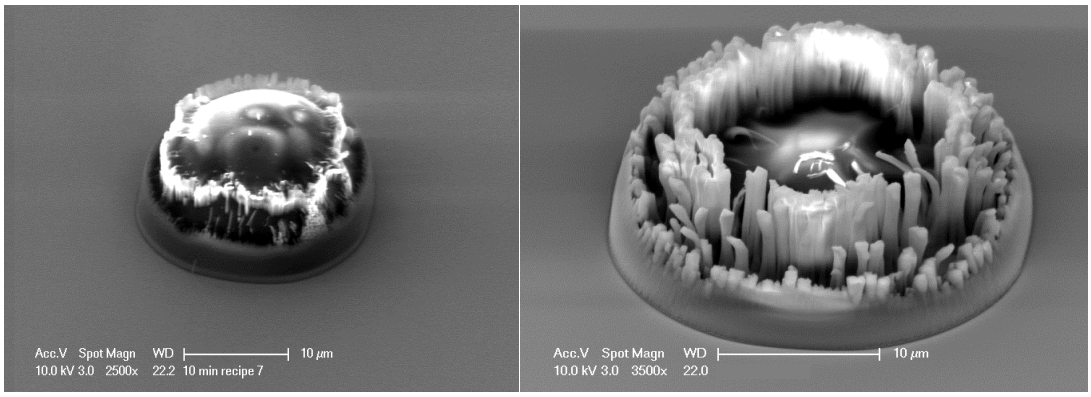

Figure 41 SEM of ICP etch after 10 minutes (left) and 45 minute (right). The gas chemistry is $Ar/Cl_2/O_2$ 25/20/10. The resist peels up in strands ruining the pattern transfer, resulting in a strange looking GaSb pattern.

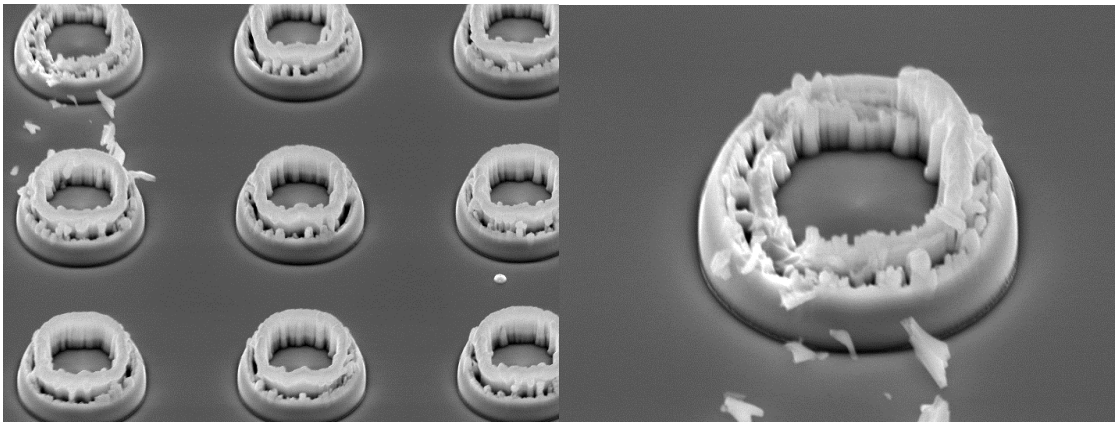

Figure 42 Resulting pattern transfer after 90 minutes of etching with the same recipe as in figure 41.

Once the oxygen flow rate from the ICP was decreased, the lens shape was maintained well throughout etching, as shown in figure 43 where the pattern transfer is

about half way done and the lens shape can be seen in both GaSb and photoresist. Also shown on the right of figure 43, the resist was removed by being exposed to 5 minutes of oxygen plasma cleaning, leaving GaSb mesas and proving the pattern is transferring. The recipe used here was similar to the earlier ones, the key difference being a decrease in oxygen flow rate relative to the rest of the gas. However, the low oxygen flow rate would lead to a very rough, "grassy" GaSb surface once etching was completed, shown in figure 44.

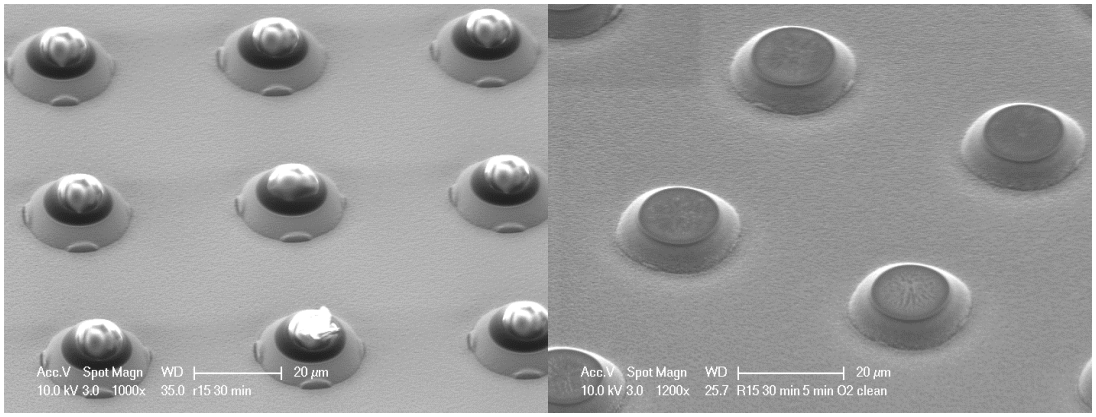

Figure 43 Pattern transfer after 30 minutes of etching using the same recipe as figures 42 and 43, except with a gas chemistry of $Ar/Cl_2/O_2$ 30/12/3. The bottom half of each lens on the left shows the lens shape transferring into the GaSb, the top half shows remaining photoresist still intact. On the right, the photoresist is removed with a 5 minute oxygen plasma clean. Only the gas chemistry (reduction of oxygen) was changed to create these results.

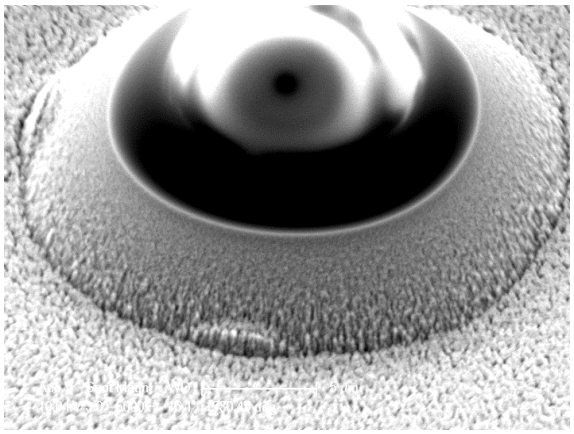

Figure 44 Rough grassy surface resulting from the gas chemistry used in figure 44.

While searching for a reason for the pattern transfer failure at higher oxygen flow rates, it was discovered that too high of a reflow temperature could lead to a "burning" of the photoresist, that may result in very difficult removal. After changing to the lower temperature reflow step (180° C to 145° C), the same etch recipe that destroyed the photoresist lens shape now maintained the pattern, despite its high oxygen content. As shown in figure 45, the photoresist remains intact after 30 minutes of etching although the GaSb etch rate is low and there is ring shape around the lens. It is suspected that the ring around the outside comes from either an angle dependency of the etch not allowing for quick removal of the edges of photoresist, or some kind of chemical interaction slowing down the GaSb etch near the edge.

It was concluded that the higher temperature reflow recipe was causing the problem shown in figure 41. Because of this concern, to be safe with not overheating the photoresist, the 145° C temperature was kept for the recipe, as it was advised to remain under 150° C [78].

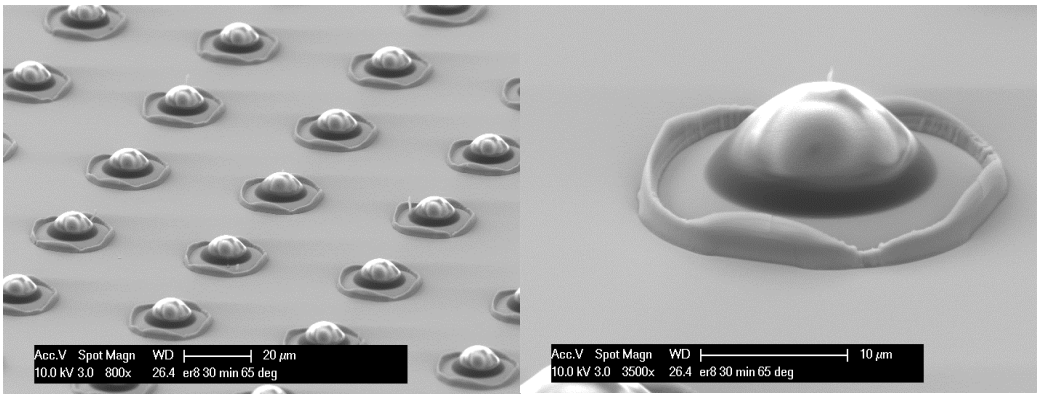

Figure 45 Resulting shape of the same recipe used in figure 41 for only 30 minutes with the lower photoresist melting temperature, showing that the pattern transfer failure was caused by the high temperature reflow step.

Inductively Coupled Plasma Etching

There are two main ways to etch semiconductor material: wet etching and plasma etching (also known as dry etching). Because wet etching is usually more isotropic (etching both deep into the substrate and laterally) as shown in figure 46, it would not be ideal for transferring a lens pattern. Plasma etching, on the other hand, is more anisotropic, and it is less selective, meaning the mask material is etched more quickly. While this lower selectivity would be problematic for an etch trying to reach maximum depth, it is helpful to an etch that is trying to achieve pattern transfer, because the mask must be removed at the same time as the underlying material.

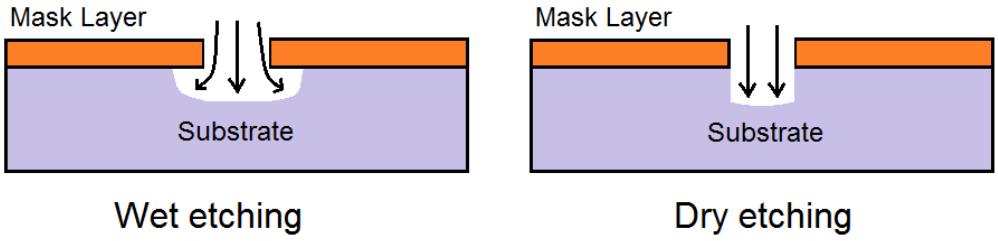

Figure 46 Wet etching vs dry etching. With a wet etch liquid etches laterally, while with a dry etch gases are bombarded vertically creating a more anisotropic etch.

Inductively coupled plasma (ICP) etching was chosen for the lens pattern transfer. ICP systems direct gas into a chamber at a steady flow rate while simultaneously modulating the throttle valve to a vacuum pump to maintain a constant pressure. To ignite the plasma, a coil is electrified at radio frequencies. To direct the plasma ions, the top and bottom of the chamber are biased and a magnetic field helps draw the plasma ions down toward the sample being etched. There are two mechanisms that contribute to ICP etching: physical and chemical. Physical etching comes from the transfer of momentum from the plasma ions to the material's atoms, knocking them loose and allowing them to evaporate. That is, the plasma atoms simply bombard the surface of the material. Chemical etching uses the chemical reaction of the ion atoms with the material forming new bonded molecules that are removed from the surface. The combination of the two etch mechanisms help speed up and aid each other, creating faster etch rates.

A Samco RIE-200iP chlorine ICP etching system was used for these experiments. A basic diagram is shown in figure 47 [80]. This system uses flow

controllers to pump gas into a chamber, where a sample can sit on a 6” wafer (usually silicon) attached by vacuum grease. This wafer sits on a temperature controlled helium vacuum chuck, and the attachment of the sample allows for a good thermal connection, keeping the sample temperature close to its setting (50° C in each etch discussed here) while otherwise the plasma bombardment would normally cause its temperature to rise. A roughing pump backing a turbo pump controls the chamber pressure.

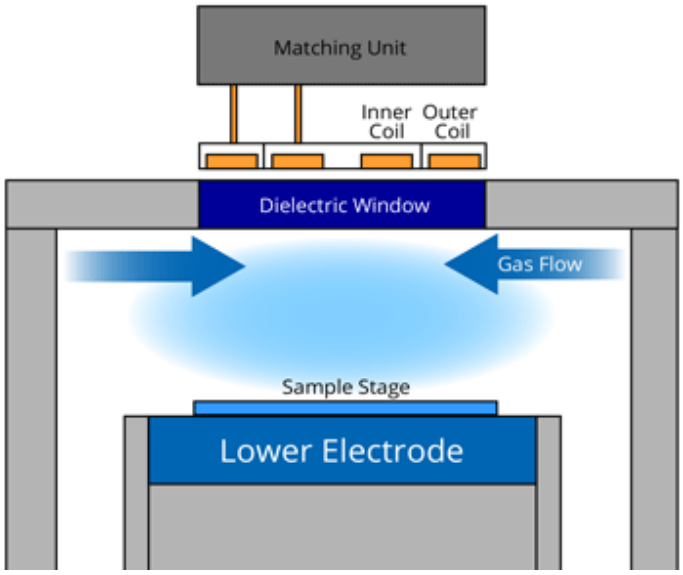

Figure 47 Diagram showing ICP chamber with incoming gas flow, the unit for matching impedance for the RF coils, and the lower electrode for the bias [80].

Boron Trichloride and Argon for Gallium Antimonide Etching

The first gas chemistry chosen to test the etching ability of GaSb was boron trichloride (BCl_3) and argon (Ar). The argon was the primary physical component of the etch, being a noble gas and not chemically combining with other materials. The argon's job then was aiding the chlorine in the BCl_3 by loosening surface material and allowing easier chemical reactions. The initial plan was to test if the physical etch of the photoresist would have a similar rate to the physical and chemical etch of the GaSb. Although there was not a significant physical etch rate of the photoresist that could be measured, table 1 shows a small sample of GaSb etch rates for different chamber conditions that helped lead to a final recipe for pattern transfer. Pressure is chamber gas pressure, bias is strength of the bias moving the gas downward, ICP is the RF coil power igniting the plasma, gas flow rates are measured in standard cubic centimeters per minute (sccm), and the Gasb etch rate is shown in μm per minute.

Table 1 GaSb etch rates for varying ICP parameters using BCl_3 and Ar.

Run	Pressure (Pa)	Bias (W)	ICP (W)	BCl_3 (sccm)	Ar (sccm)	Etch (μm/min)	Notes
1	1.33	100	800	10	20	.14	
2	1.33	300	800	10	20	.43	Surface rough
3	1.33	150	800	10	20	.3	
4	1.33	100	800	10	20	.06	Surface Pitting
5	1.33	100	200	10	20	.1	
6	1.33	100	100	10	20	.04	
7	1.33	100	100	10	20	.043	
8	1.33	200	100	10	20	.065	

While the etch rates shown are not considerably fast, this was not considered a problem. Since the lens height is relatively short (<20 μm), and the desired lens could

be even smaller in GaSb, a slower, more easily controlled etch was desired. Moreover, while some surface roughening may be desirable for light extraction, a very rough surface that may result from a much faster etch rate would be undesirable.

Chlorine, Oxygen, and Argon ICP for Pattern Transfer

Adding Oxygen

The solution that would aid pattern transfer during the etch was to add oxygen to the gas chemistry, as it removes photoresist. However in the Samco ICP system, mixing BCl3 and oxygen is not permitted, possibly due to the reaction that occurs between the two gasses [65, 81]. Because of this limitation, chlorine gas was used instead of boron trichloride to etch the GaSb [65]. Thus chlorine along with argon and oxygen would be the chosen gas chemistry for further experimentation.

Table 2 Initial runs for chlorine, oxygen and argon gas chemistry etches. Etch shows GaSb etch rate.

Run	Pressure (Pa)	Bias (W)	ICP (W)	Ar (sccm)	Cl_2 (sccm)	O_2 (sccm)	Etch (µm/min)	Notes
1	1.33	120	300	30	20	10	.013	Rough surface
2	1.33	120	150	30	20	10	.015	
3	0.5	150	150	30	20	10	.037	
4	0.5	150	150	15	35	5	.35	Very rough
5	0.5	150	150	25	25	8	.06	

Under this gas chemistry, the argon provides a physical bombardment to the substrate and the chlorine and oxygen act as chemical etchants. Figure 48 shows the basic principle of the process. The first experimental etches were to test the varying

rates of etching of the GaSb substrate and the AZ 4620 photoresist. After attempting a few basic etches, it was apparent that adding too much chlorine percentage in the gas chemistry would create a very rough surface, consistent with literature [82]. After a handful of experimental runs shown in table 2, it became apparent that the gas chemistry was simultaneously etching the GaSb and photoresist, though the photoresist was etching faster. This difference in etch rates was seen as acceptable, as a shallow lens would be a good starting point and the oxygen flow rate could be adjusted to etch the photoresist more slowly.

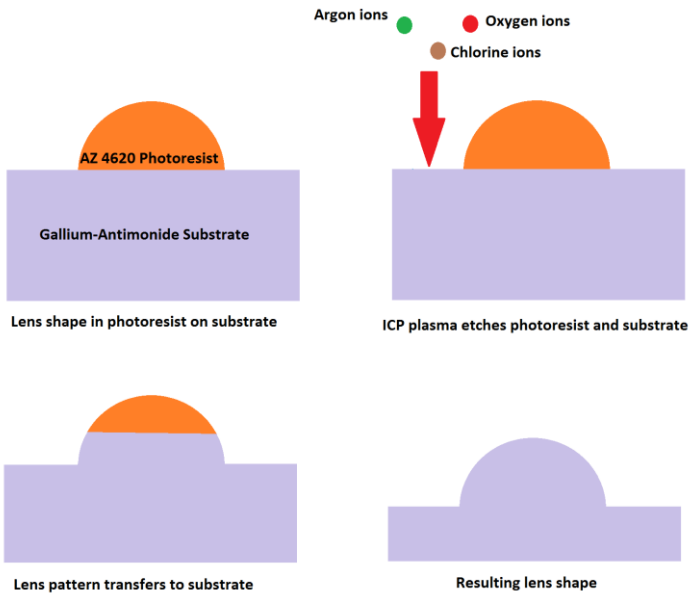

Figure 48 Diagram of the process for pattern transfer.

Results

After showing simultaneous etching of GaSb and photoresist, all parameters were varied to try to derive the significance of each ICP parameter. Table 3 shows the

results of an attempted design of experiment. ESC is the voltage on the electrostatic chuck holding the carrier wafer that the samples were mounted on. The most noticeable observation is that decreasing oxygen flow rate increase GaSb etch rate significantly. Drawing results from these experiments was problematic, as the photoresist was showing the pattern transfer problems discussed earlier. While the experiments seemed to yield non-effective results with the higher oxygen flow rates, the lower oxygen flow rate etch recipes were creating very rough surfaces. The surface roughness is suspected to be caused by micro-masking, where small clusters of molecules are formed at the surface that do not easily etch away. These molecules are a result of the chemical etching by-products. Whatever the cause, it appears that high oxygen content is necessary for leaving a smooth surface after etching, but at the same time, too high of oxygen content ruins initial pattern transfer, as shown by the ring in figure 46. Because of this trade-off, etch experiments were done with intermediate oxygen flow rates, based around the first successful pattern transfer recipe.

Table 3 GaSb etch rates while varying all parameters.

Run	Pressure (Pa)	Bias (W)	ICP (W)	Ar (sccm)	Cl_2 (sccm)	O_2 (sccm)	ESC (V)	Etch (μm/min)	Notes
1	1	175	175	30	25	9	600	.05	
2	0.5	125	125	30	25	6	600	.1	Very rough
3	1	125	125	30	20	9	500	.023	
4	0.5	175	175	30	20	6	500	.12	Very rough
5	0.5	125	175	25	25	9	500	.04	
6	1	175	125	25	25	6	500	.2	Very rough
7	0.5	175	125	25	20	9	600	.056	

Once it was discovered that lowering the gas flow rates to 30/12/3 $Ar/Cl_2/O_2$ produced a healthy pattern transfer, this gas chemistry with the parameters of run 7 in table 3 was used as the basis for the rest of the lenslet etching experiments.

Lenslet Results

Varying Oxygen Flow Rate

Etch times were finally increased to complete pattern transfer and create full GaSb lenslets. Given the tradeoffs, three data points for full pattern transfer were chosen using different oxygen flow rates. Four selected recipes from full lenslet etching are displayed in table 4, and each will have accompanying SEM images.

Table 4 Lenslet recipes with varying oxygen levels.

Run	Time (mins)	Pressure (Pa)	Bias (W)	ICP(W)	Ar (sccm)	Cl_2 (sccm)	O_2 (sccm)
1	45	0.5	175	125	30	12	1
2	60	0.5	175	125	30	12	3
3	60	0.5	175	125	30	12	4
4	60	0.5	175	125	30	12	5

Run 1 is a 45 minute etch with only 1 sccm of oxygen, to test the lower extreme of oxygen flow rate. This oxygen flow rate caused a very slow etch of the photoresist and a much more volatile and rough etch of the GaSb. The result is seen in figure 49, where it is also apparent that if the surface roughness can be cleared, a very tall lens shape can be achieved.

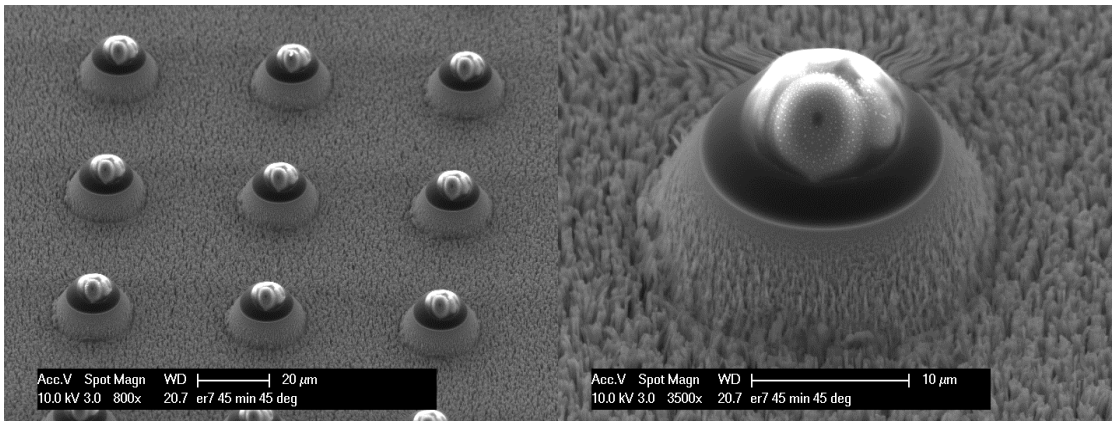

Figure 49 Lowest oxygen flow rate attempted at 1 sccm for 45 minutes. The surface becomes very rough with time.

In runs 2-4, enough time is given to etch through the vast majority of the photoresist, only sometimes leaving small tip of it at the top of the lens. Run 2 uses 3 sccm of oxygen, and is shown in figure 50, where the height of the lenslets was later measured to be at about 7.8 μm. In figure 51, run 3 increments the oxygen to 4 sccm. The measured height of these lenslets was about 6.5 μm. Lastly, figure 52 shows the result of 5 sccm of oxygen. The measured height of these lenslets was shown to be about 6 μm. The decrease in lenslet height with the increase of oxygen flow rate was expected.

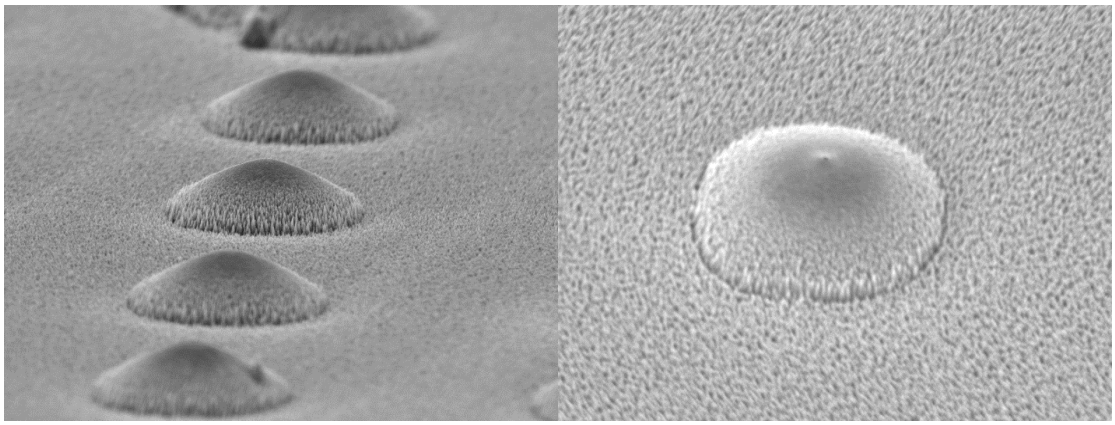

Figure 50 60 minute recipe using 3 sccm of oxygen.

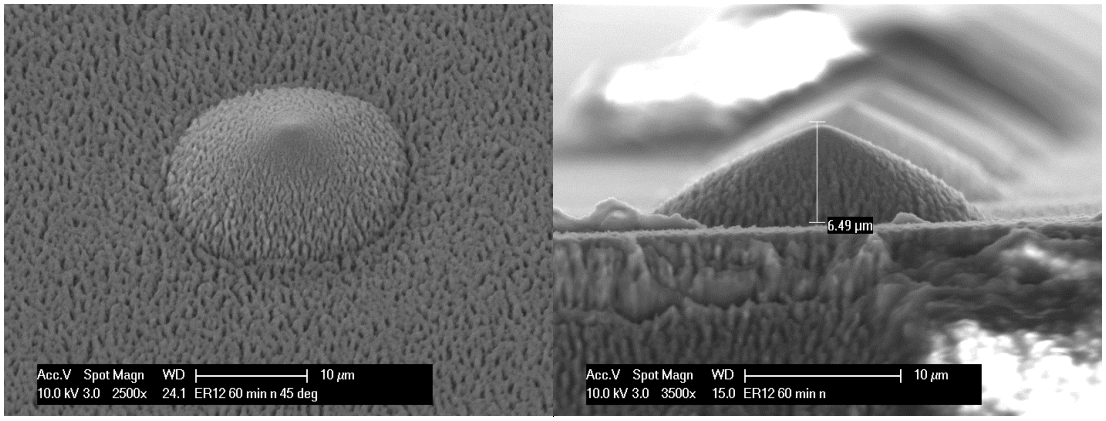

Figure 51 60 minute recipe using 4 sccm of oxygen.

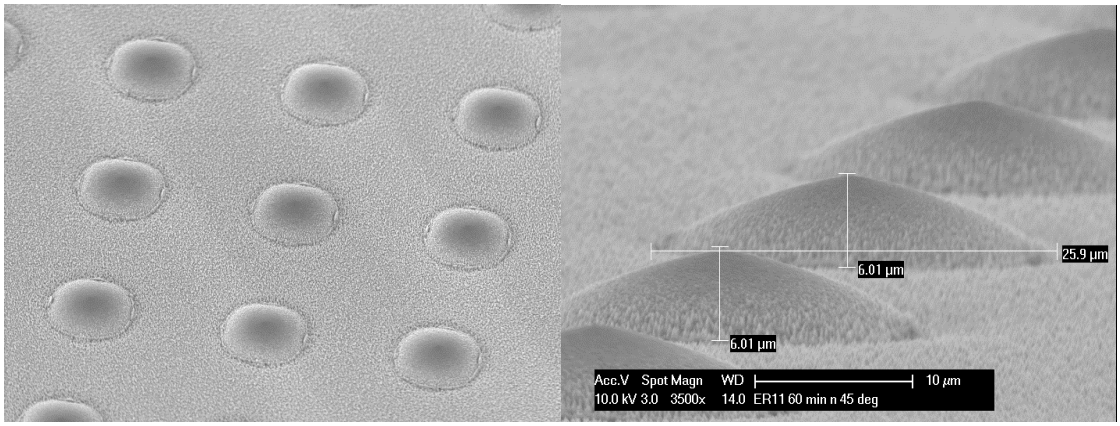

Figure 52 60 minute recipe using 5 sccm of oxygen.

Figure 53 shows the plots of the lens shape resulting from runs 2-4 with data obtained visually from the SEM images. Run 4 showed the least amount of surface roughness, along with the most curvature in the lens shape. At the lower lens shapes, the curvature is almost non-existent, making them more of shallow cones than lenses. The trade-off is the lens shape only being 6 µm tall. A taller shape may be achieved by starting with thicker photoresist lenses. While lots of "grass" on the surface of the GaSb may be generally undesirable, it may prove to be useful in the IRSP system. By scattering the oblique angled light, it reduces total internal reflection, but on the lens itself, where roughness is at a minimum, light passes through and focuses into the collimating optics. Overall, initial results indicate that effective lenslets should be achievable with varying shapes and sizes.

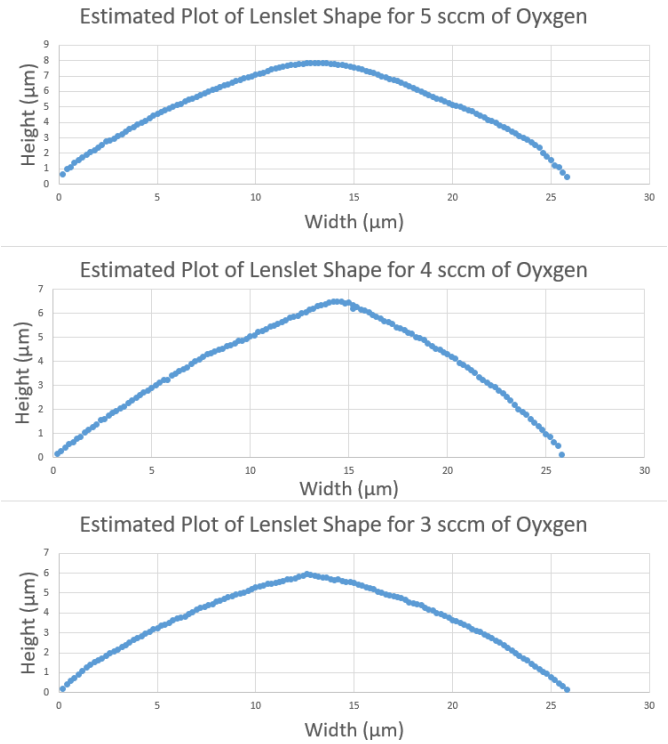

Figure 53 Lens shape data for varying oxygen flow rates. The data was taken visually from SEM images.

Changes to the Etch Recipe

Some etch parameters were slightly adjusted to see if more desirable results could be achieved. Initially it was thought that by increasing pressure from 0.5 to 1.33 Pa and ICP power from 125 to 200 W, the etch would become more isotropic and remove the grassy roughness. By increasing ICP power there would be more free chlorine ions to chemically etch the surface. By increasing the pressure, more gas would fill the space surrounding the uneven surface helping etch away features and clear away micro-masking. The result of 60 minutes of this recipe is shown in figure 54 where the result is disastrous and the micro-masking has worsened, although the etch rate has become much faster.

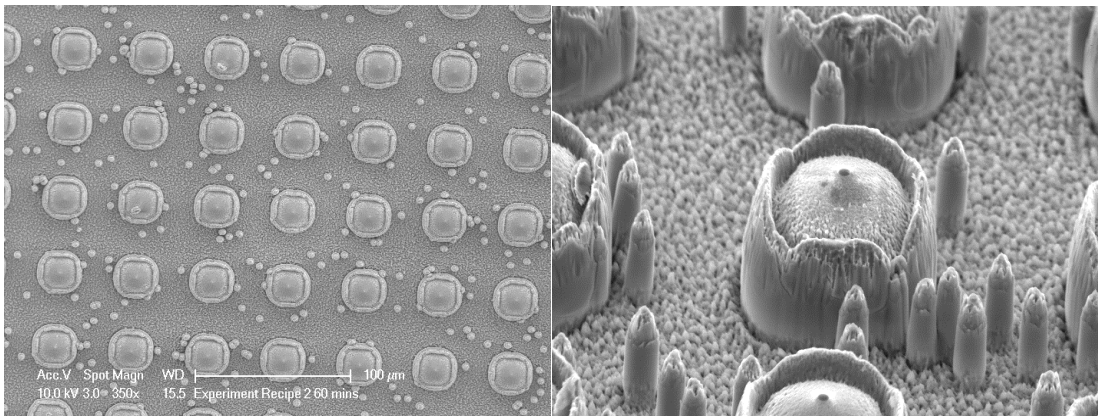

Figure 54 Results of increasing pressure and ICP power.

Next, a 30 minute etch was attempted with the bias power decreased from 175 to 100 W. The result is shown in figure 55, where the photoresist etch rate has decreased and the surface is rough but less grassy. Pattern transfer is not excellent, but this result may be a good start for future experimentation.

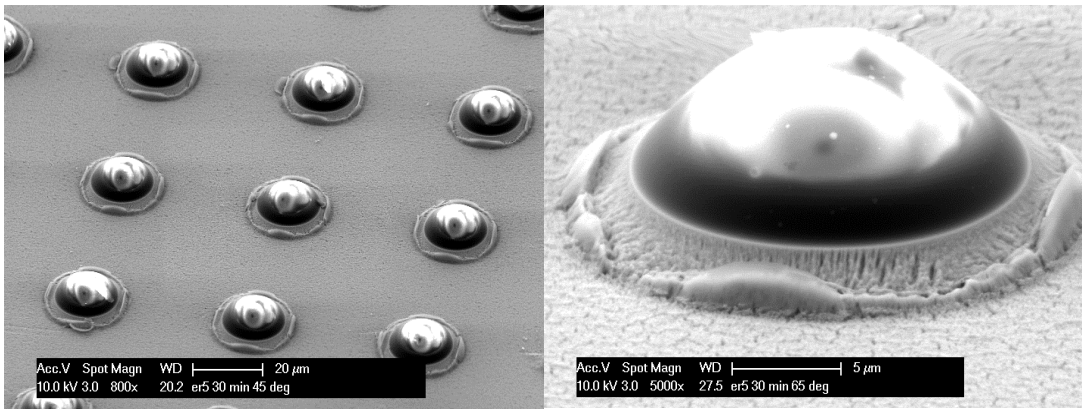

Figure 55 Result of decreasing bias power.

Building on this result, the bias power was set to 125 W and the ICP power at 150 W for 60 minutes. The hope was to increase the etch rate while maintaining the smooth surface. The results made the surface extremely rough, as shown in figure 56.

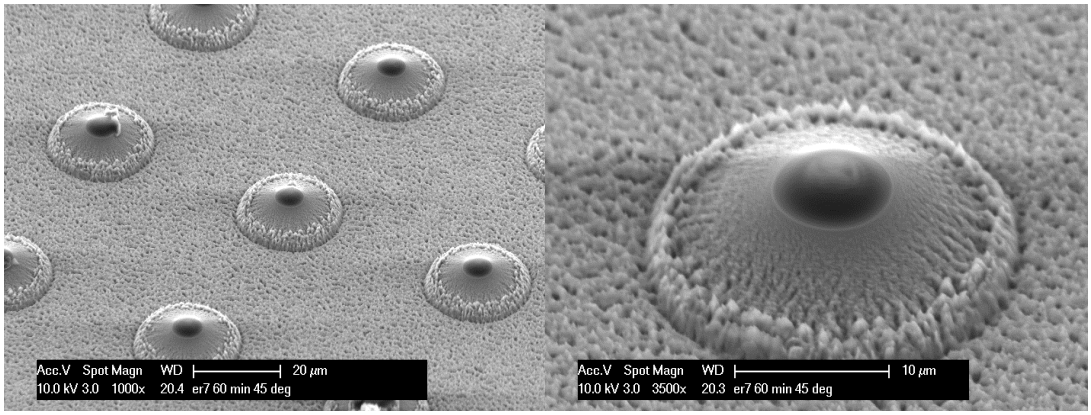

Figure 56 Result of 125 W bias power and 150 W ICP power.

A more promising result came from a recipe using 30/20/7.5 sccm of $Ar/Cl_2/O_2$ with a bias and ICP back to 175 and 125 respectively. The results are show in figure 58, where pattern transfer is still not ideal but the surface is left very smooth. The drawback is the shallow lens result and the inconsistency between lenslets across the sample as shown in the image.

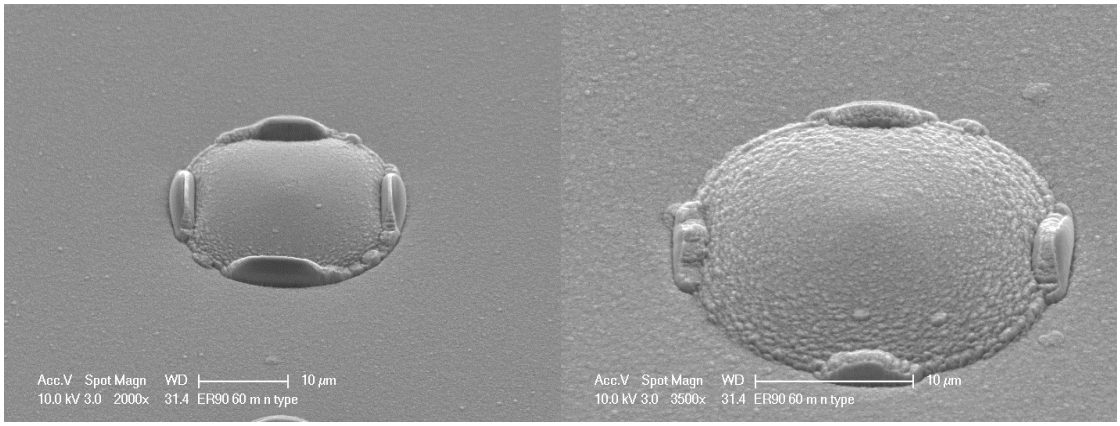

Figure 57 Result of 30/20/7.5 sccm of $Ar/Cl_2/O_2$. Pattern transfer is inconsistent across the sample.

Conclusion and Future Experimentation

In conclusion, it seems that generating variable height lenslets is a strong possibility for improving light extraction in the IRSP system. Not only that, but these recipes are able to include some surface roughening to scatter reflected light in combination with the lenslets to increase focus. The range of lens shapes that could be generated at this time is limited, however there are many possible paths to correct this limitation. While some work was done on looking into photoresist lens shaping, all kinds of initial lens shapes may be created by changing the photoresist, spin speed, mask shape, development parameters and melt parameters. Also, by changing gas chemistry, ICP power, bias power, and other ICP parameters the lens shapes will turn out differently.

There are also ways to decrease surface roughness. If the roughness is caused by high temperature, as indicated in some literature [83], it may be beneficially to reset the etch every 5 or 10 minutes to allow the sample to cool before continuing. Also, adding a more isotropic GaSb etch step at the end of the recipe may clear up and

reduce the grassy surface. Another option is to put the lenslets into a wet etch to smooth out the surface assuming no damage is done to the lens shape. Lastly, perhaps bathing the sample in a solution of silica beads and agitating with ultrasound could physically remove grass.

The next phase of lens research for these IRSP systems is to implement binary phase Fresnel lenses (BPFLs), as shown in figure 58 [84]. This solution could be ideal, because it focuses light on a target an exact distance away. By etching concentric rings around the center of the LED's back surface, one can create a "tuned" focus to the point of the collimating optics for a HWIL setup [85-86]. Further, once the mask is designed, the photolithography and etch step become much simpler, as a target etch depth must be reached but can tolerate some error.

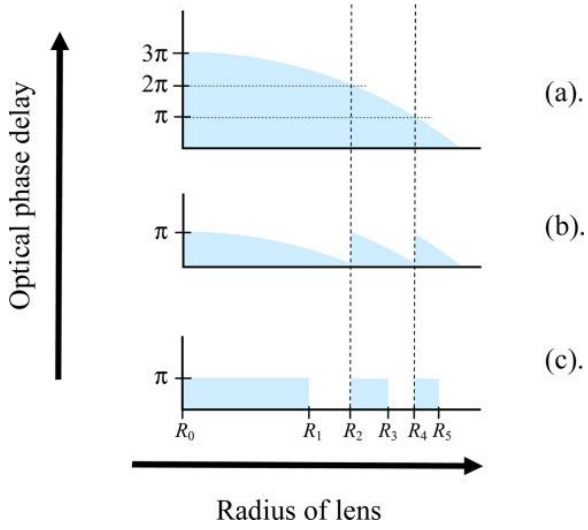

Figure 58 Diagram explaining the concept of a BPFL [84]. (a) shows a full lens shape. (b) shows the Fresnel lens equivalent. (c) shows the binary phase equivalent.

The hardest challenge with these solutions is performing the surface treatment on a finished SLEDs hybrid. While it is easy to test a bulk sample of GaSb, it is much more difficult on a full array. If done before hybridization, it must be certain that the features can survive flip-chip bonding, which is an area where BPFLs will also excel over lenslets. If done after hybridization, it must be certain that no damage is done to the hybrid, which may be difficult when considering how the ICP operates. If BPFLs are pursued, a simple oxygen plasma clean step after the etch in the ICP should make photoresist removal non-problematic.

Chapter 4

TWO WIRE TRANSMISSION LINE FOR CHIP TO CHIP OPTICAL COMMUNICATION

Introduction

As CMOS processes continue to improve and smaller circuitry increases the computational ability of modern computer processors, the connections, both intra-chip and inter-chip, become the bottleneck [87-88]. That is, as advanced VLSI creates smaller circuit components, increasing a processor's computational speed does not improve overall performance because their information cannot be transmitted within or outside the chip fast enough. Parallel processing can alleviate this problem by dividing the computation between processors, but there are still fundamental limits. Moreover, improving the interconnects in a parallel system then greatly improves processing speed, assuming the processors can be made faster as well.

The traditional metal wire carrying a digital signal has a fundamental bit rate limit based on its aspect ratio [87]. The longer and thinner a line is, the smaller the bit rate that it can transmit. The problem comes from the time required to change the voltage level on the wire, since digital signals require a rapid change between the "high" and "low" voltage. The larger a wire's time constant, the longer this transition takes. When a time constant gets too high, the signals blur, which would show as a closing of the "eye" in the eye diagrams in figure 59 [87]. With an increasing time constant, the slopes of the lines going up and down will get stretched horizontally, and eventually will not reach the voltage level required in the time given by the clock

period. This closing of the eye is caused by one of two factors, depending on frequency and conductor width [87]. The first cause is the skin effect making the conduction exist only close to the surface of the wire. This cause dominates more at higher frequencies, where the skin depth gets smaller and smaller. The second cause is bulk resistance, where the resistance of the metal increases the time constant. This cause is more of a problem as the cross sectional area of the wire gets smaller. In figure 60, Miller and Ozaktas show which mechanism will dominate [87]. There are ways to engineer better bit rates through metal interconnects, but there will still be a fundamental limit to data transmission over conventional wires.

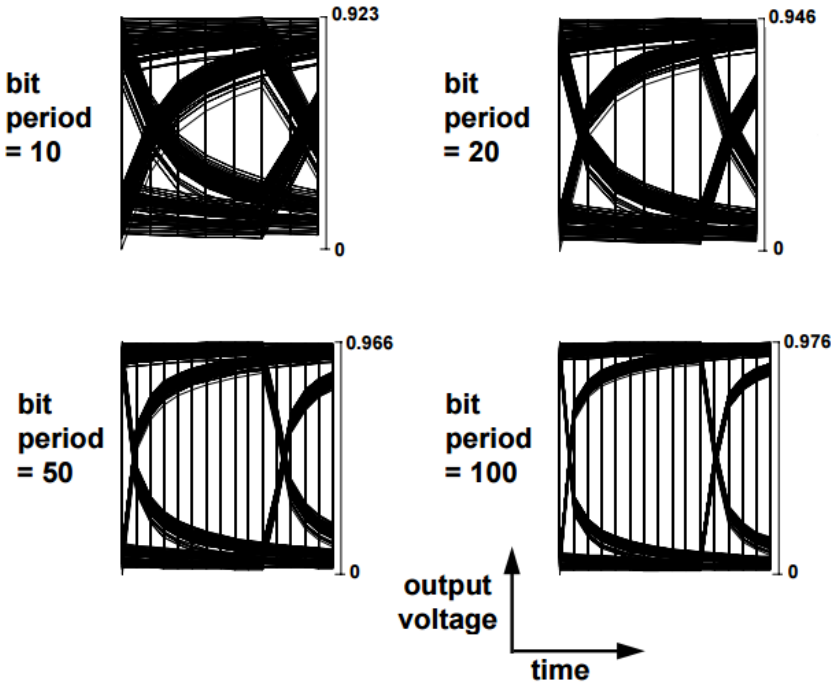

Figure 59 Eye diagram showing digital voltage level vs. time. Signals switch from a digital "high" to "low." As frequency increases (or period decreases), the signals begin to blur, closing the "eye" [87].

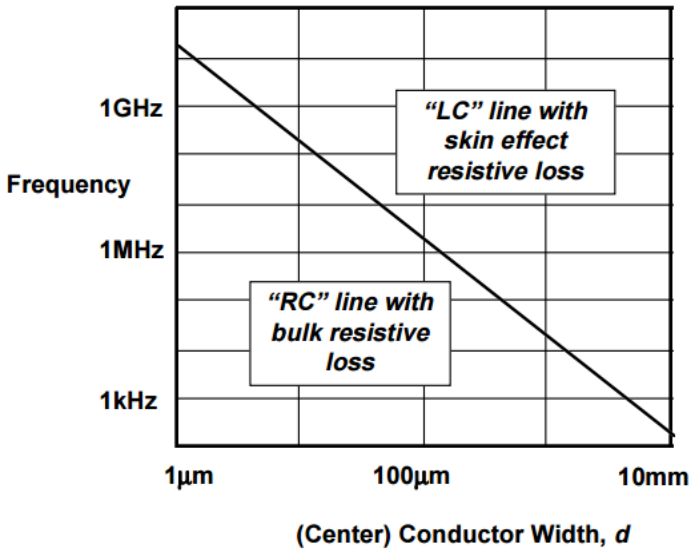

Figure 60 Miller and Ozaktas' plot showing which loss mechanism will dominate in a conductor based on frequency and conductor width [87].

Optical Interconnects

A solution to the bit rate problem that traditional metal wires face is to switch to an optical signal, because a photon travelling through space or a dielectric medium is not as hindered as an electron travelling through metal [89-90]. This advantage can already be seen on a larger scale, as almost all long distance transmission of data is done over optical fiber. These distances can be as long as oceans, where undersea fiber cables are laid, but have even become as short as the cables between racks in a data center. The greatest challenge here is integrating the optical components (light sources, receivers, and transmitting mediums) into already well developed silicon CMOS technology. IBM's Terabus for example, uses a polymer waveguide in PCB with transceivers for chip-to-chip communication [91]. On chip, optical components have been developed for CMOS silicon on insulator technologies [92-93]. Optical

interconnects have even been investigated using gold metal as the medium by exciting surface plasmon polaritons to carry signals from one end of a PCB to the other [94].

An entire area of research called silicon photonics has been working toward developing optical components on silicon for data transmission [95-97]. Light sources including silicon lasers have been developed and improved upon [98-101]. Silicon ring resonators have been shown as operational modulators for a light source [102-104]. With developments like these, optical interconnects are a possible source of hope for sustaining Moore's law into the future. However, while these designs require many new components, there may be a way to implement the wire-bonds already connecting a chip to its package. This chapter will discuss implementing this idea.

Transmission Lines

An electric current carried over a wire with electrons moving in one direction is direct current (DC). Alternating current (AC) has the electrons moving back and forth at some frequency, for example 60 Hz for the power in an American outlet. Once AC reaches a high enough frequency, it is begins to radiate too much power for efficient transmission over long distances. This power loss is why once frequencies increase into the microwave regime transmission lines are used. Figure 61 shows some transmission line geometries [105].

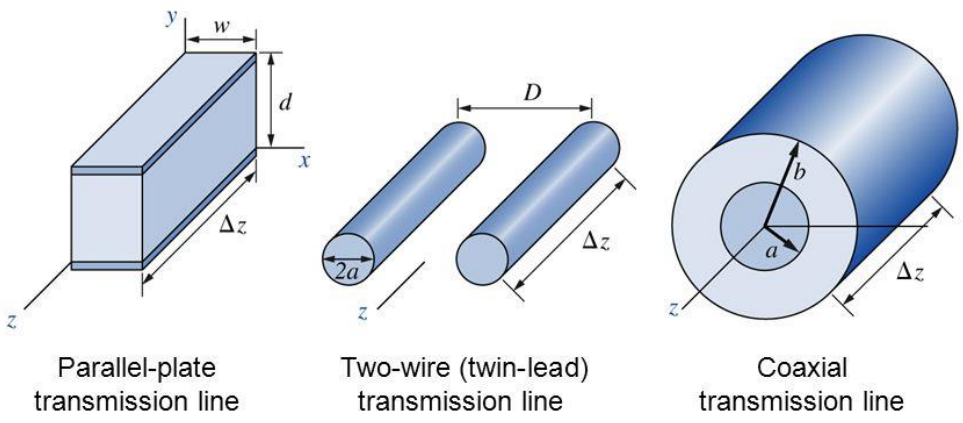

Figure 61 Parallel plate, two wire, and coaxial transmission lines [105].

Transmission lines propagate electromagnetic fields generated by the alternating current between conductors. There are many types, but a simple two parallel wire system will be discussed here. Figure 62 shows the fields generated between the two conducting wires [106]. These fields are in the transverse electromagnetic (TEM) mode, meaning their electric and magnetic fields are perpendicular to the direction of propagation. Once frequencies approach gigahertz and terahertz magnitudes, heavy losses start to become a concern. Because of these high-loss concerns, transmission lines for frequencies higher than the terahertz are not traditionally considered.

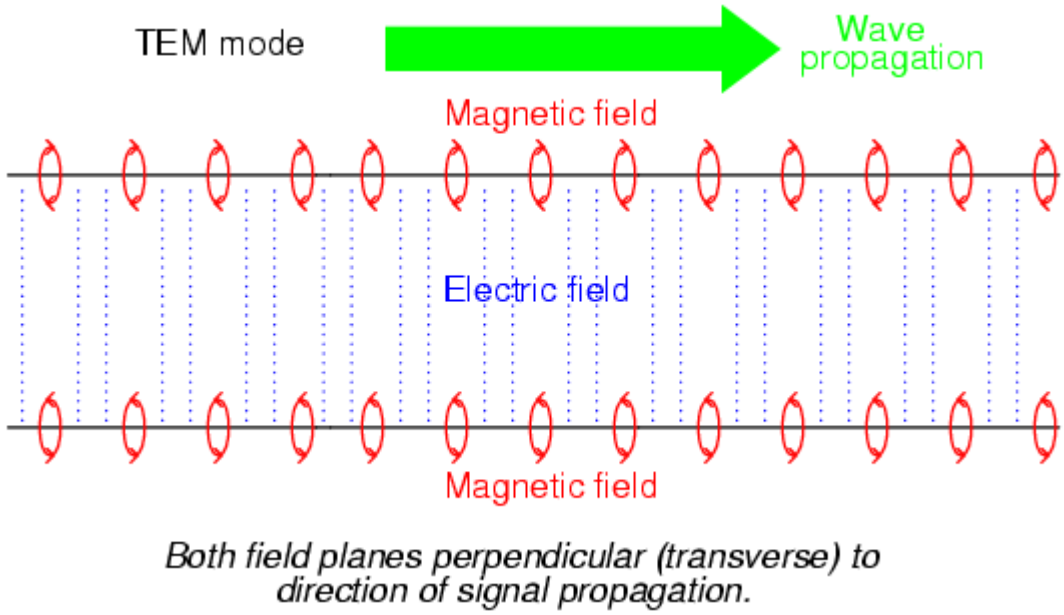

Figure 62 TEM mode in a two wire transmission line [106]. Electric fields go between wires while magnetic fields loop around them, both perpendicular to wave propagation.

Terahertz Two Wire Transmission Lines

Creating terahertz beams and transmitting them have become an area of interest [107-109]. While most terahertz transmission is done through other types of waveguides [110-114], single wire [115] and two wire transmission lines have been investigated. A two wire transmission line with low bending loss was shown to transmit the TEM mode [116]. Also, the theory of the operation of a two wire transmission line and its loss coefficient were calculated [117]. Since terahertz frequencies bridge the gap between the microwave and optical, it is then a question of whether transmission lines are applicable at optical frequencies, and if so what are the constraints.

Design

Design Using Bond Wire Technology

Taking into account previous research and the need for fast inter-chip communication, a novel use for a well-known connection is shown in figure 63. A waveguide that takes advantage of existing bond wire technology using infrared wavelengths would create an optical connection between two adjacent chips. Data signals carried by infrared light can couple into the transverse electromagnetic (TEM) mode between two gold conductors by placing a vertical cavity surface emitting laser (VCSEL) between two bond wires. These two wires then serve as optical transmission lines guiding the light to a photodetector on the other end. The mode has both electric and magnetic fields perpendicular to the direction of propagation and is concentrated near the inside of each wire. This design removes any extra optical elements from modern chip packaging.

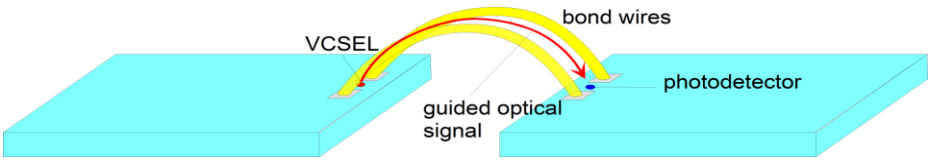

Figure 63 Bond wires bridge two adjacent chips to use IR light to communicate between a VCSEL and photodetector.

Challenges

There are several challenges with the proposed design that have to be addressed. Using optical signals guarantees fast communication given that enough power can go from the VCSEL to the photodetector. To calculate the loss of the two wire design there are several factors to consider. First is the transmission loss from

the conducting wires, which we can calculate with skin effect analysis. Coupling loss will be very significant as well, which may be mitigated by the source radiation pattern matching the mode shape of the waveguide. Minor wire misalignment as well as varying separation along the waveguide will cause loss via reflection. Lastly, curvature loss should be considered as well.

Transmission Line Loss

Skin Effect Analysis

Skin effect analysis is used to find the loss in terms of distance traveled on a conductive transmission line. The magnetic fields at the surface of the conductor will be equal to the magnetic fields just inside the conductor. The electric field then just inside the conductor can be found by solving Maxwell's equations, assuming that the spatial variation in the direction normal to the conductors is much greater than in the direction of propagation [118]. Another explanation of that assumption is that the skin depth is much smaller than the wavelength.

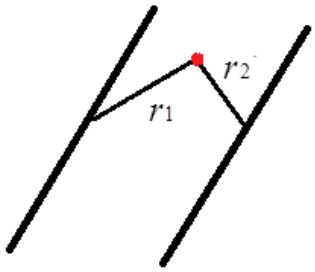

Figure 64 A point visualized between two parallel lines. The two distances r_1 and r_2 represent the shortest distance between the lines and the point.

Finding the power lost then starts with finding the magnetic fields on the surface of the conductors. Finding the field distribution for the TEM mode of a two wire system means solving for the fields in a two dimensional slice of the two wire waveguide, normal to the direction of propagation. To start, model the two wires as line charges with the lines at a position inside the wire [117]. The voltage between the line charges, visualized in figure 64, can be shown as

$$V(x,y) = A\ln\left(\frac{r_1}{r_2}\right). \tag{4.1}$$

Here, V is the voltage at the point (x, y), and is a function of the constant A, and r_1 and r_2, which are the distance between the point and the opposite first and second line charges.

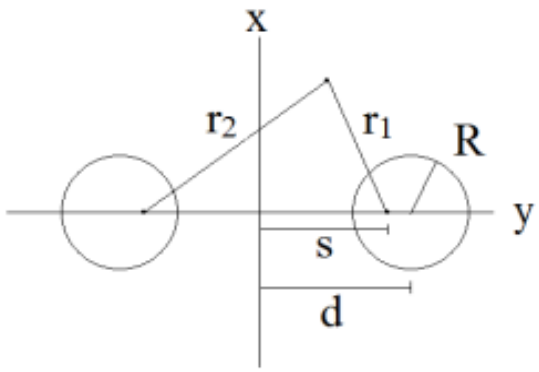

Figure 65 A slice of the two wire system. The wires have radius R, are spaced a distance d from the center. The distance s from the center to the wire represents the location of line charges to map the potential at any point using equation 4.1.

This geometry is illustrated in figure 65, which also shows the relationship between the two wires of radius R, and the location of the corresponding

representative line charges. Both line charges are a distance *s* away from the midpoint of the spacing between the two wires. The last variable *d* is the distance of the center of each wire from the midpoint of the spacing between them. The equation that gives a value for *s* such that the voltage in equation 4.1 is equal along the outside of the conductor is

$$s = \sqrt{d^2 - R^2}. \tag{4.2}$$

The electric fields can then be found as the derivative of the voltage:

$$E_x = \frac{dV(x,y)}{dx} = A\frac{4s(x^2 - s^2y^2)}{(s^2 - 2sx + x^2 + y^2)(s^2 + 2sx + x^2 + y^2)}, \tag{4.3}$$

$$E_y = \frac{dV(x,y)}{dy} = A\frac{8sxy}{(s^2 - 2sx + x^2 + y^2)(s^2 + 2sx + x^2 + y^2)}. \tag{4.4}$$

Using Maxwell's equations and the impedance of the medium (free space in this case), the magnetic fields are found from the electric fields. Figure 66 shows mapping the intensity of these fields against the geometry of the two dimensional slice of the two wires, where red areas indicate highest intensity and blue areas indicate lowest.

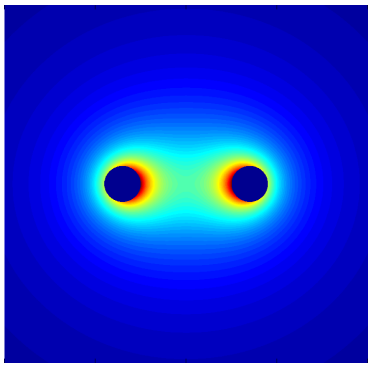

Figure 66 Field intensity of TEM mode between two wires. The blue and red represent the ends of the spectrum of low and high intensities, respectively.

The analysis and formulation for conductor loss found in Jackson uses static conductivity and is valid only for low frequencies. The complex conductivity, or complex refractive index, of the conductor must be used to find the lost power for higher frequencies [118]. To find the complex refractive indices for any given material and frequency, one can just use a source of empirically found values [119-120]. To find the formulation for loss using the complex conductivity, start with Maxwell's 4th equation:

$$\nabla \times \mathbf{H} = \mathbf{j} + \varepsilon \frac{\partial \mathbf{E}}{\partial t} = \sigma_{real}\mathbf{E} + \varepsilon_{real} \frac{\partial \mathbf{E}}{\partial t} = (\sigma_{real} - i\omega\varepsilon_{real})\mathbf{E}. \tag{4.5}$$

Both σ_{real} and ε_{real} are both only real values. To account for high frequency, substitute the complex permittivity

$$\varepsilon = \varepsilon_{rel} + i\frac{\sigma}{\omega} \tag{4.6}$$

in for the real permittivity and find that

$$\nabla \times \mathbf{H} = -i\omega\varepsilon_{rel}\varepsilon_0\mathbf{E} = \sigma\mathbf{E}. \tag{4.7}$$

In equations 4.6 and 4.7, σ or ε_{rel} are an approximation and are not yet accounting for the out of phase components of the equation. To continue the complex analysis, we start with the fields that go into the conductor:

$$E, H \propto e^{-\xi/\delta} e^{i\xi/\delta}, \tag{4.8}$$

where δ is the skin depth and ξ represents the normal coordinate into the conductor [118], given as

$$\frac{1}{\delta} = \sqrt{\frac{\omega\mu\sigma_0}{2}}. \tag{4.9}$$

At this point, the analysis deviates from the low frequency (DC) analysis. Taking equation 4.9 in the complex form, substituting for the low frequency conductivity with its equivalent shown in equation 4.7, and allowing ε_{rel} to become complex, the result is:

$$\frac{1}{\delta} = \sqrt{\frac{\omega\mu[-i\omega\varepsilon_0(\varepsilon_r + i\varepsilon_i)]}{2}} = \frac{\omega n}{2c}(1-i). \tag{4.10}$$

Here n represents the complex refractive index and the speed of light c is used to simplify the equation. Using this formulation for the inverse skin depth and substituting into equation 4.8, the fields

$$E, H \propto e^{-\frac{\xi\omega(n_r+in_i)}{2c}(1-i)} e^{i\frac{\xi\omega(n_r+in_i)}{2c}(1-i)} = e^{-\frac{\xi\omega n_i}{c}} e^{i\frac{\xi\omega n_r}{c}} = e^{-\frac{\xi 2\pi n_i}{\lambda}} e^{i\frac{\xi 2\pi n_r}{\lambda}} \tag{4.11}$$

can be found where the end of this equation changes the form of the radial frequency divided by the speed of light to the equivalent inverse free space wavelength, λ. Equation 4.11 implies that using the complex analysis the fields inside the conductor can be modelled as a wave propagating into it normal to the surface.

Linking equation 4.8 to equation 4.11, the high frequency (AC) skin depth is shown to be

$$\delta_{AC} = \frac{\lambda}{2\pi n_i}. \tag{4.12}$$

Now using the AC skin depth and remembering that the tangential magnetic fields in the conductor are equal to the tangential magnetic fields just outside the conductor, equation 4.11 can be extrapolated to find the magnetic field in the conductor as

$$H_c = H_{\|} e^{-\frac{\xi 2\pi n_i}{\lambda}} e^{i\frac{\xi 2\pi n_r}{\lambda}}. \tag{4.13}$$

To find power lost into the conductor, the electric field must also be solved. Assuming that the gradient of the field in normal direction is much greater than in the direction of propagation, the field gradient is simplified to

$$\nabla \cong -\mathbf{n}\frac{\partial}{\partial \xi}, \tag{4.14}$$

where **n** is the unit direction normal to the surface outward, and ξ is again the coordinate inward to the conductor [118]. In the proposed waveguide operating in the near infrared, the skin depth into the conductor is much smaller than the wavelength of the propagated light wave, allowing for the assumption giving equation 4.14 even expanding into visible wavelengths.

Taking the magnetic field in the conductor shown in equation 4.13, the electric field in the conductor is

$$E_c = (1-i)\sqrt{\frac{\mu\omega}{2\sigma}} H_{\|} e^{-\frac{\xi 2\pi n_i}{\lambda}} e^{i\frac{\xi 2\pi n_r}{\lambda}} = (1-i)\sqrt{-\frac{\mu}{2i\varepsilon_0 n^2}} H_{\|} e^{-\frac{\xi 2\pi n_i}{\lambda}} e^{i\frac{\xi 2\pi n_r}{\lambda}} = \frac{\eta_0}{n} H_{\|} e^{-\frac{\xi 2\pi n_i}{\lambda}} e^{i\frac{\xi 2\pi n_r}{\lambda}}. \tag{4.15}$$

Knowing the magnetic and electric field components, Poynting's theorem provides enough information to calculate the time-averaged power per area:

$$\frac{P}{A} = \frac{1}{2}\mathrm{Re}\{E_c H_c^{*}\}. \tag{4.16}$$

Resulting Formulas

To find the total power lost per length travelled due to the conductors' skin effect then we simply sum the losses along the outside of each wire. That is, for an individual wire, plug in the two dimensional surface integral of the conductor's electric and magnetic fields into equation 4.16. Because of the relationship between the electric and magnetic fields, doing this substitution will simplify to

$$\frac{P_{loss}}{length}|_{AC} = \frac{\eta_0 n_r}{2(n_r^{\,2} + n_i^{\,2})}\oint |H_{\parallel}|^2 dl, \tag{4.17}$$

where η_0 is the free space impedance.

It is worth noting that a simple DC analysis of the feasibility of the proposed waveguide would result in a different equation for power lost per length travelled [117]:

$$\frac{P_{loss}}{length}|_{DC} = \sqrt{\frac{\mu_0 \omega}{8\sigma_0}}\oint |H_{\parallel}|^2 dl. \tag{4.18}$$

The only difference is the factor outside the integral, which now accounts for the complex refractive index. Depending on the material properties of the conductor, the AC analysis may prove to show lower loss coefficients (power lost per unit length), making the waveguide a more attractive option than originally thought.

The attenuation coefficient α, is simply

$$\alpha = \frac{P_{loss}\,/\,length}{P_0}. \tag{4.19}$$

The time-averaged power flow then uses Poynting's formula

$$P_0 = \frac{1}{2}\mathrm{Re}\{\int_s (E \times H^*) ds\}. \quad (4.20)$$

Results

All results found from this loss analysis were calculated in MATLAB. The electric and magnetic field magnitudes can be mapped out using equations 4.3 and 4.4 for a given wire radius and wire spacing. The result of these equations will be a two dimensional drawing of fields between two line charges that exist between the wires. Then, overlaying the geometry of the two conductor waveguide (in this case two circles), the total power flow is calculated from equation 4.20 and for the entire two wire geometry outside of the wires. It is easy to sum the fields along the outside of the wires after that to provide the surface integral of the power lost per length given in equation 4.17. To finish calculating the power lost, the numerical data for the complex index of refraction for a given conductor at a given frequency can be looked up [119-120]. These values complete the information required for equation 4.19, giving the attenuation constant.

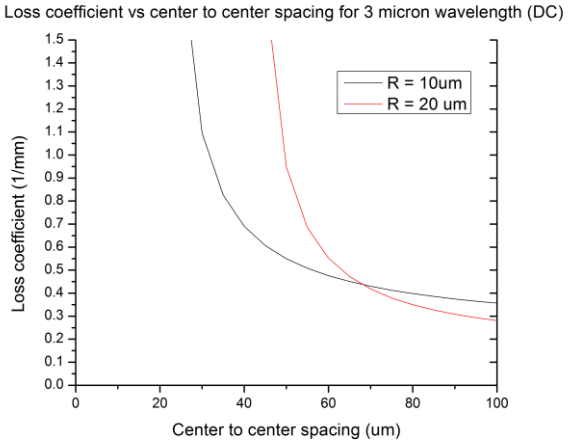

Figure 67 Loss coefficient vs center to center spacing for 3 μm wavelength using DC analysis. Wire radii of 10 and 20 μm are plotted.

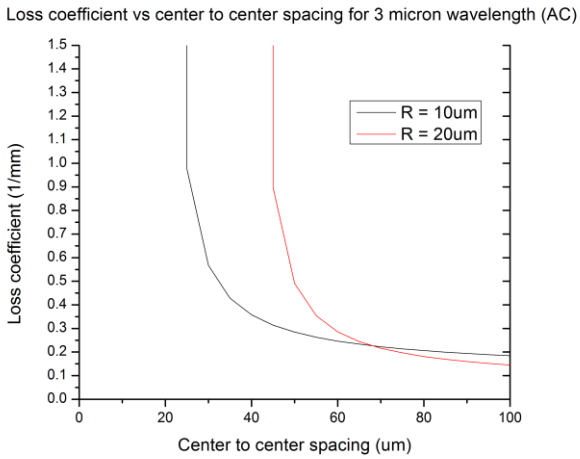

Figure 68 Loss coefficient vs center to center spacing for 3 μm wavelength using AC analysis. Wire radii of 10 and 20 μm are plotted. Using AC analysis losses are well below those shown from the DC analysis in figure 67.

Figure 67 shows the loss coefficient given by the low frequency analysis of the proposed two-wire waveguide using gold wires. It plots the attenuation coefficient in

inverse millimeters as a function of the center to center spacing between the wires. The two lines represent different wire radii of 10 and 20 μm. This analysis is done at a 3 μm wavelength using Palik's values for complex index of refraction of gold [119]. As can be seen in figure 68, the same plot as figure 67 except using the high frequency analysis show before, the attenuation is not as high when accounting for the high frequency. The AC loss coefficients show as about 60% of the DC loss coefficients. As the spacing becomes great enough the attenuation goes below 0.2 mm^{-1} [121]. Based on the graphs, it would be favorable to operate the two wire waveguide around the knee of the curve to keep a low level of attenuation while keeping the spacing close enough to help coupling into the TEM mode.

Figure 69 shows the results of the gold wire analysis extending down into common VCSEL wavelengths, using a center to center spacing of 60 μm and gold wires of 15 μm radii. The AC analysis shows an increase in attenuation as the wavelength gets shorter, but still shows even stronger performance than would be thought from the DC analysis. Due to the complex index of refraction of gold, there is also a decrease in attenuation at 1.2 μm, resulting in a loss coefficient of about 0.3 mm^{-1}. However, this "dip" in attenuation is result of measurement, as shown by a comparison to the Johnson and Christy's values in figure 70 [120]. In figure 70, the attenuation graph is smooth and slightly increasing, although both sets of values are similarly low.

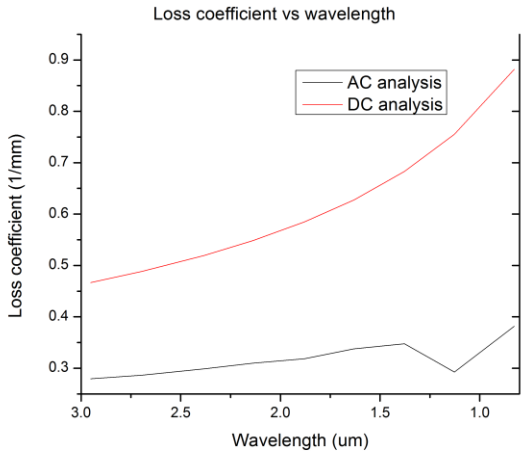

Figure 69 Loss coefficient vs. wavelength for a wire radius of 15 μm and center to center spacing of 60 μm.

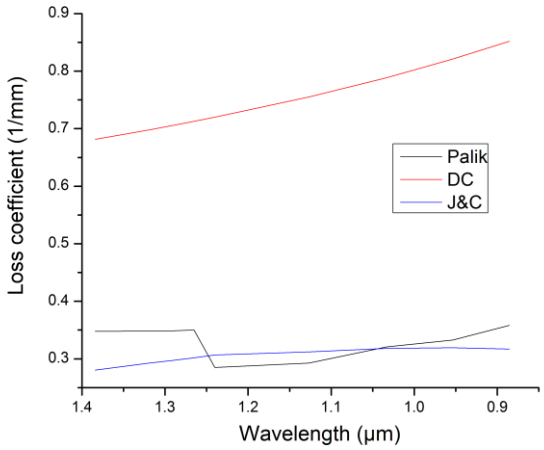

Figure 70 Loss coefficients for DC analysis and AC analysis (using both Palik's and Johnson and Christy's values).

The final result of the loss analysis then shows that two chips several millimeters apart could use a gold wire transmission line with tolerable transmission

losses. Gold wires with radii of 15 μm and 60 μm center to center spacing could carry signals of VCSEL wavelengths only losing 0.4 mm^{-1} (-1.7 dB/mm). Looking at a 1.2 μm wavelength, the losses will be 0.3 mm^{-1} (-1.3 dB/mm) and the light could travel 7 mm with less than a 10 dB transmission loss. Overall these results are promising for facilitating chip to chip communication in the proposed two wire waveguide for VCSEL to photodetector communication [121].

Other Losses and Coupling

The next step in the analysis of the two wire waveguide for chip to chip communication is looking into other possible sources of power loss. Because bond wires are placed in an arc, the curvature will cause some losses. To calculate the curvature loss, it is understood that the radius of curvature that corresponds to a bending loss scales directly with wavelength [122]. In a calculation for a two wire terahertz waveguide, a 50 cm radius of curvature only provided ~1 dB of loss for a 1500 μm wavelength [116]. Scaling that result to 1 μm wavelength, a 300 μm radius of curvature will provide a similar tolerable loss. For the two wire waveguide at optical wavelengths, two chips 2 mm apart will have a radius of curvature of 1 mm, an even lower curvature loss [121].

The next problem using bond wires then is the possible non-uniform spacing of the two wires from one end to the other. As the spacing of the two wires changes, geometry changes will create a gradient of impedance mismatch that may cause reflections of power. However, looking at the relationship for transmission line impedance in free space:

$$Z_0 = 276 \log\left(\frac{d}{r}\right), \tag{4.21}$$

where Z_0 is the characteristic impedance, d is the center to center wire separation and r is the radii of the wires, the impedance of the line will scale logarithmically with the separation. This scaling will significantly dampen any power reflection compared to the causal change in wire separation. To give an example using equation 4.21, the calculated impedance of a 25 μm diameter wire spaced 100 μm apart is about 166 Ω. Assuming an abrupt misalignment of 20 μm at some point along the wires (making the wire spacing 120 μm), the impedance with the same geometry is calculated to be about 188 Ω. Plugging these impedances into the equation for the reflection coefficient,

$$\Gamma = \left| \frac{Z_2 - Z_1}{Z_2 + Z_1} \right|, \tag{4.22}$$

Γ, the reflection coefficient, is found to be about 0.062. Assuming the wires are aligned somewhat accurately, this reflection should not be a significant source of loss for the two wire system [121].

The last remaining source of loss will come from coupling a VCSEL's light output into the TEM mode. The first thing to consider when calculating coupling loss is the overlap integral of the waveguide's TEM mode shape and the incoming light source's mode shape, defined as

$$\eta = \frac{\left| \int E_1^* E_2 dA \right|^2}{\int |E_1|^2 dA \int |E_2|^2 dA}, \tag{4.23}$$

where η is the coupling efficiency and E_1 and E_2 are the electric fields in the two overlapping modes. Looking back at figure 66, the power is concentrated near the wires. This mode shape means the waveguide would best be supported by two sources placed near the footprint of the wires, or one source split into two ends that are close to the inside of the wires. The electric fields in this mode point from one conductor to

the other, so it will also be critical that the incoming light is polarized in that same direction. If it is not correctly polarized, any excess power not aligned to the mode's direction will be wasted. Considering that a polarized light source placed between the wires and concentrated near them is feasible, the overlap integral of the TEM mode and the incoming mode should yield a strong result, implying that coupling into the mode could be possible.

Experiments

Wire-Bonds on Glass

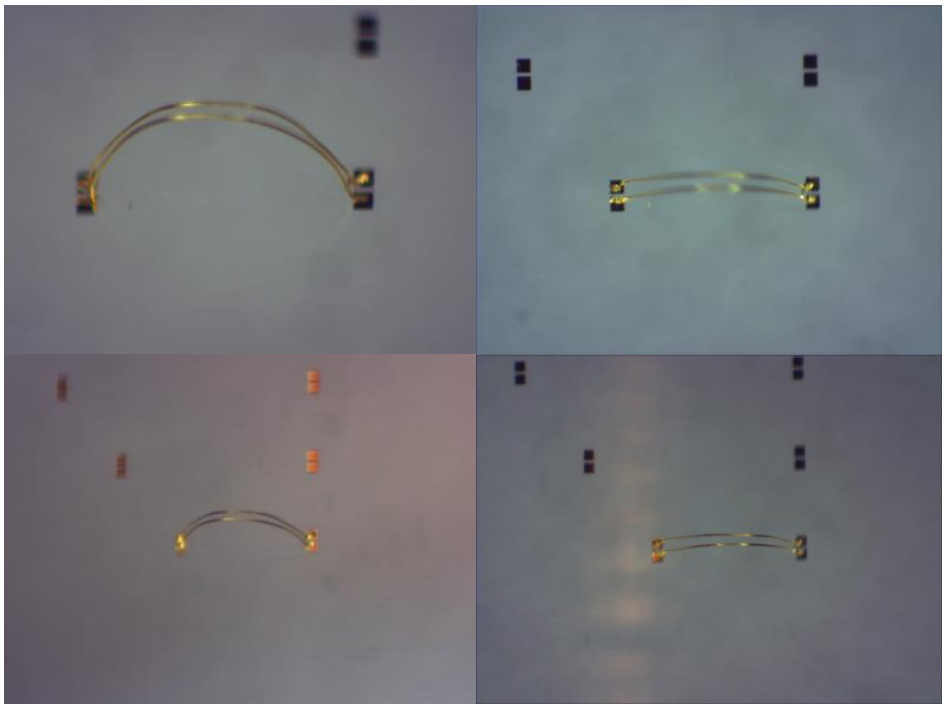

Figure 71 Wire-bonds hand bonded onto gold pads on glass.

The first attempt at a real two wire waveguide was to place the wires onto glass. A small, thin piece of circular glass was processed with photolithography to have wire-bond pads made of titanium and gold. These pads would be in sets of two, with varying spacing between them. Opposite each pair of pads was a copy of those pads for the two wire-bond ends. The source for this experiment was visible red laser light shined through the glass into the opening between the two bond pads. A camera was mounted and zoomed in on the opposite set of pads where the wire-bonds ended. The wires were hand bonded as close to the inside of the pads as possible, to ensure the correct spacing. Figure 71 shows images of the wire-bonds on glass.

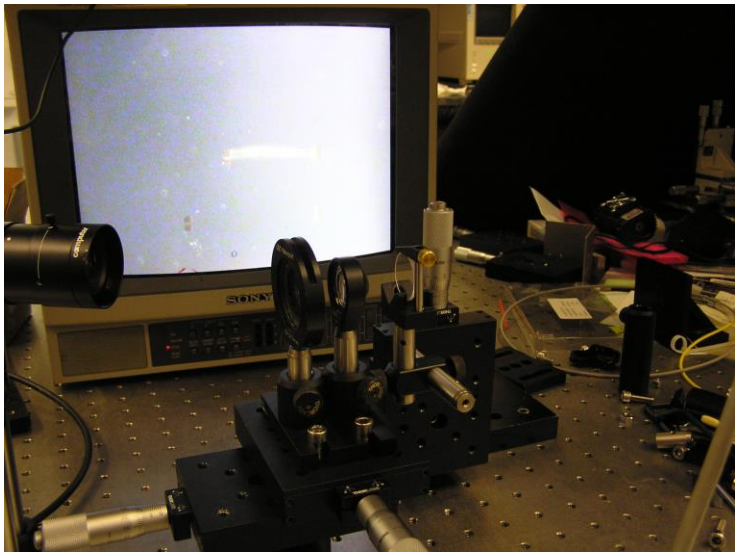

Figure 72 Experimental setup. Light is focused onto circular glass window between two wires. A camera is zoomed onto the wires and displayed on the screen behind the setup. On the screen, the gold horizontal line is the wire pair.

Figure 72 shows the experimental setup, with the red light coming from a laser pointer, through an iris and lens onto the sideways mounted glass. No visible light was detected on the other side of the wires. The first speculation was that the wire-bonds were not precise enough or perhaps the intensity of light transmitted was not strong enough to be seen on camera.

Optical fiber that could provide a light source much closer to the waveguide system was implemented to simplify the alignment. By bringing the fiber to the top of the wires' arc, infrared light could be immediately coupled into the two wire system. Figures 73 and 74 show the real experimental setup, both visually and with a screen showing the output of a zoomed in camera. This experiment did not end up showing any result either, despite efforts to try varying alignments of the fiber to the wires.

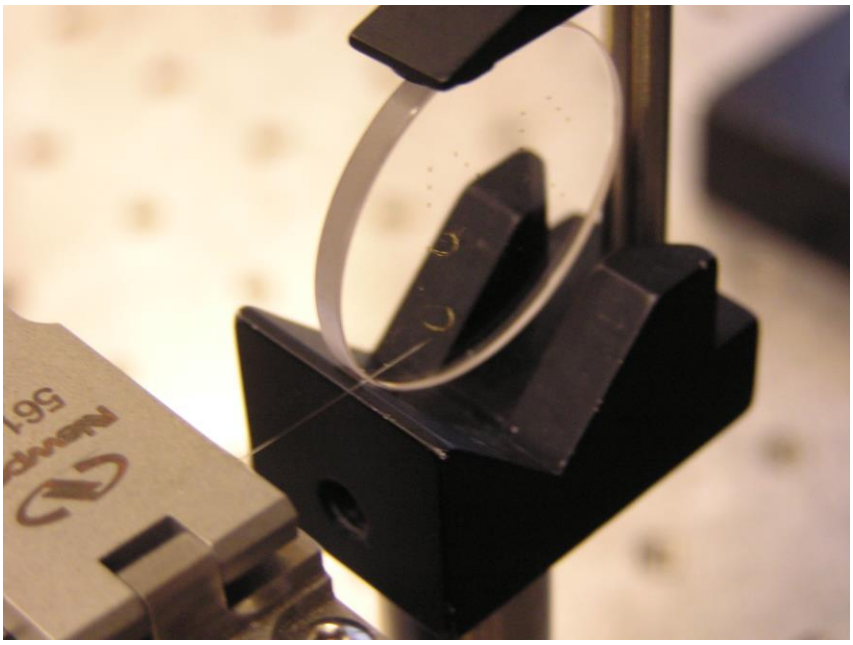

Figure 73 Optical fiber approaching between wires on glass.

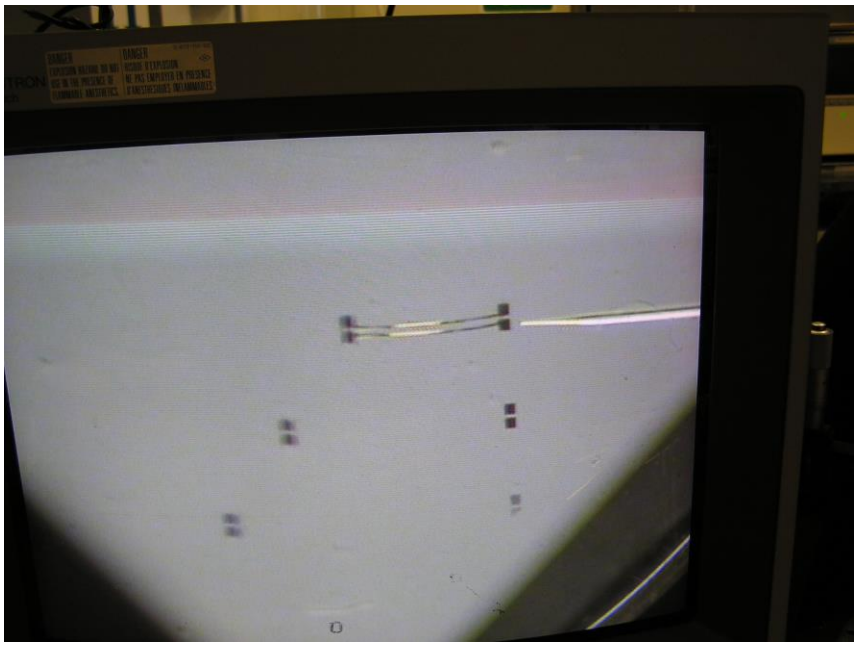

Figure 74 Camera view of two wire waveguide on glass, with optical fiber approaching the center.

Wire-Bonds on Chip

After other attempts to hand place gold wires failed, a more precise and ambitious method was pursued. On a manufactured silicon photonics chip, a small area was reserved for our experiment. Along the edge of this area were grating couplers to allow laser output to couple into waveguides that travelled just under the surface of the chip. Then, the light passed into a 3 dB splitter and two grating couplers launched those light signals up between two wire-bond pads. On the other end the same setup was mirrored so light could couple back into the waveguide and travel out of the chip. A rendering of the setup is shown in figure 75.

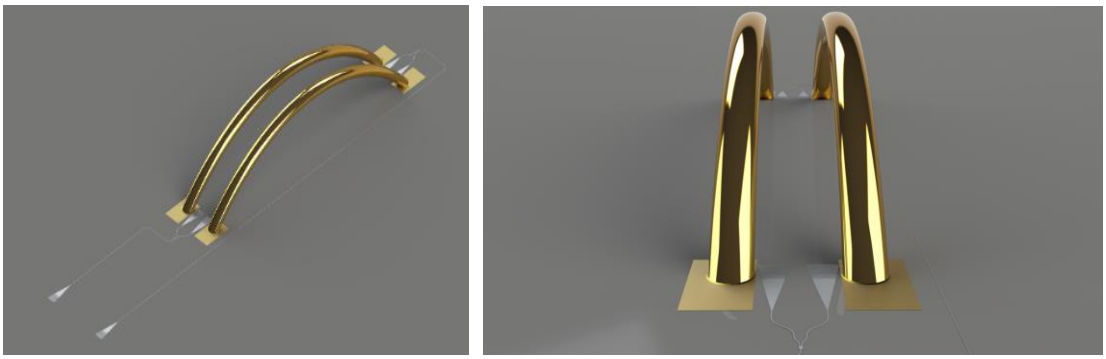

Figure 75 Rendering of two wire waveguide. Light comes in via the left grating coupler, splits into to grating couplers to send light between the wires. Light is then collected at the other end of the waveguide and sent to the right grating coupler.

The wires were machine bonded by Pantronix Corporation, which yielded a few bond pairs placed accurately enough to be used. Nearby to the bond pads, there were couplers for light that were simple loops for testing of the light coupling before testing the two wire waveguide. The chips top down diagram is shown in figure 76**,** as well as a top and side view of the wire-bonds shown in figure 77.

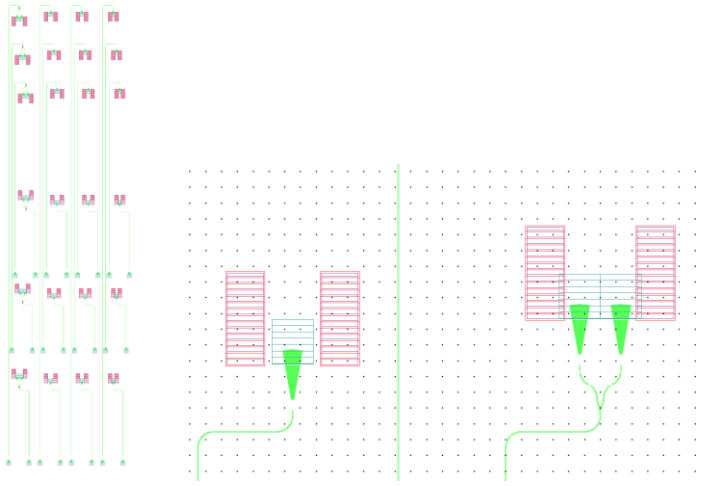

Figure 76 Layout of chip on left, blown up features on right. Red areas are bond pads, green lines are in-chip waveguides, and green cones are grating couplers.

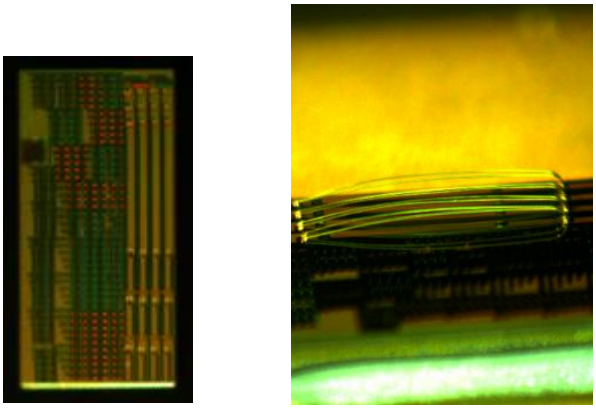

Figure 77 Top down view of the chip on left, side view of the chip on right. Wire-bonds can be seen in each image.

An Agilent laser which had a 1550 nm source and a detection input was connected to two optical fibers. These fibers were plugged into the input and output and both ended on a fiber array designed. That is, the end of both fibers travelled through a glass block that could be placed on the surface of the chip right above the

grating couplers. A diagram of a fiber array and how it is made is shown in figure 78 [123]. The spacing was matched to the chip to allow one fiber to input light into one coupler and the other to receive light from the chip's output coupler.

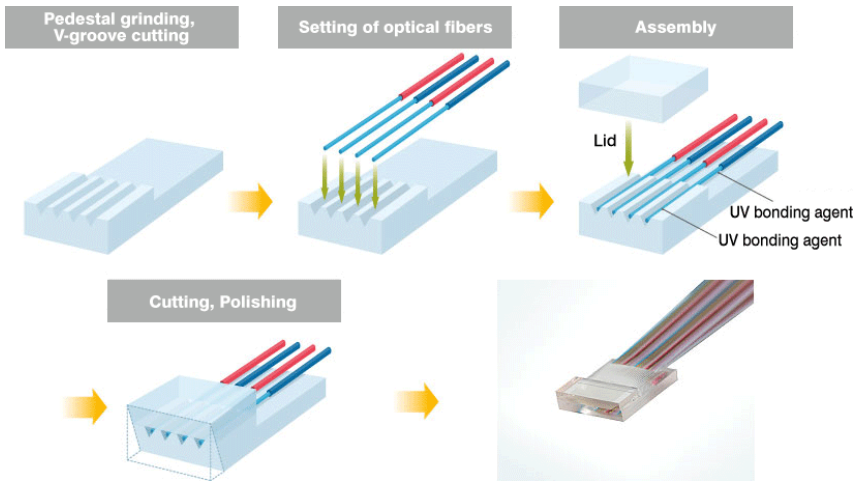

Figure 78 Making a fiber array [123].

The chip was mounted on a stage that was adjustable in three dimensions. The fiber array was adjustable in three dimensions as well as the tilt angle. Using this setup and the laser light, one of the loops off to the side was used to determine that the setup worked without the two wire waveguide. Laser light could be coupled from fiber to the waveguides on chip and a signal would be detected through the other fiber. However, when this experiment was attempted with the two wire waveguides, despite meticulous adjustment of the array to the chip, no light could be coupled out of the system.

Radio Frequency Signals in PCB

The primarily suspected problem with the waveguide was that the TEM mode could not be sustained beyond some certain spacing. This suspicion was based on the fact that the conductors were not perfect and the TEM mode would not exist perfectly perpendicular to the direction of propagation. Because of the difficulty coupling into the TEM mode, light would either pass through or couple into higher order modes with much higher losses.

To investigate, copper planes were put into PCB to test whether the TEM mode could be sustained in copper with a radio frequency (~20 GHz) coming from a network analyzer. Two copper tracks would run side by side and gradually increase their spacing. These tracks would act as transmission lines carrying a signal up to several wavelengths of spacing (~1.5 cm per wavelength). At some distance down the PCB transmission line, the two lines were shorted using a metal rod, and the effect on the reflected signal read by the network analyzer was measured. A diagram of the PCB layout is shown in figure 79, along with the experimental setup. Up to three wavelengths of spacing, the reflection increased when the lines were shorted, showing that the TEM mode was strongly transmitted to that point of shorting. Beyond three wavelengths of spacing, the reflected signal did not show any increase beyond the noise levels read by the network analyzer. While not disproving the theory that the two wire waveguide could support a TEM mode at large spacing, this experiment did not show any promise. Thus, the PCB transmission line with RF frequencies was the last experimental attempt related to the two wire transmission line waveguide for optical or infrared frequencies.

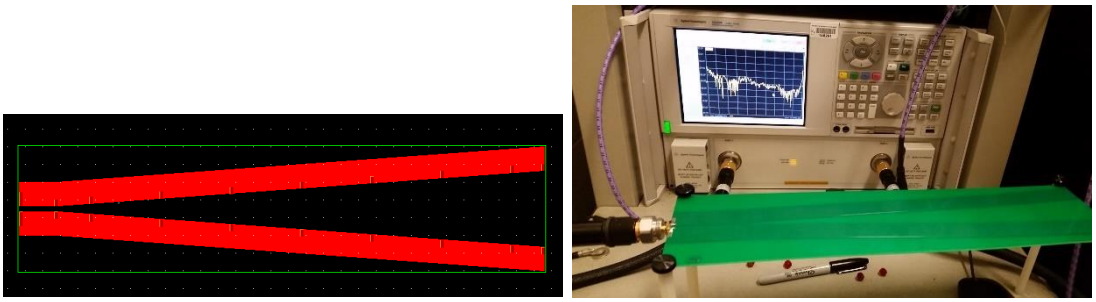

Figure 79 PCB layout on left, experimental setup on right. The red represents copper in the PCB. The experimental setup includes the network analyzer measuring reflection vs frequency.

Conclusion

Due to the lack of an unambiguous experimental result it is impossible to say that the two wire transmission line waveguide transmits optical frequencies at this time. There are a number of possible problems with the experimental setups used. A challenge with transmitting light into the wire-bond waveguide is ensuring that the angle of the TEM mode propagation lines up with the incoming source. Another challenge is the possibility that the light is being attenuated or lost so much throughout its path that it is not strong enough to distinguish from noise. It is also possible that given the large geometry of the system it is impossible for light to couple into the TEM mode due to the quasi-TEM nature of the mode. Because the conductors are not perfect, there is some variation in the mode outside of the transverse plane, which may cause problems coupling into the TEM mode with large separation.

As for the loss analysis, a quick and easy way to calculate the attenuation for any two conductor waveguide has been determined. Given a large enough geometry, one can simply follow the steps shown to calculate a transmission line's attenuation coefficient. All that is required is the geometry of the system and the complex index of refraction for the conductor at a given wavelength.

Chapter 5

CONCLUSION

This thesis has presented a wide range of research topics related to the development of IR systems. The early work started with a discussion of the challenges and adaptations to the problems presented early in the development of the world's first 512 x 512 LED IRSP system. Specific to the processing of the LED array, improvements to the recipe to help device performance and yield were shown in detail. For being the first full microdisplay system built by the team involved, the results were impressive, and showed promise for future IRSP systems.

Continuing the engineering efforts and research into the next generations of systems, enhancements were applied to every part of the system including the drive circuitry, and specifically the RIIC. VLSI circuit characterization laid the groundwork for future designs by establishing the RIIC's performance at both room temperature and 77 K. By measuring performance, a more advanced NUC can be applied to step toward a more finished IRSP product.

In solving the most critical problems, investigations into improving light extraction to reduce heat revealed the feasibility of lenslets. Lenslets patterned on the emitting backside of the LED array help reduce total internal reflection while possibly focusing pixel light to improve efficacy to the collimating optics of the HWIL setup.

Lastly, an investigation into an aggressive optical interconnect solution was unable to find any conclusive results. The losses for a two wire IR transmission line were analyzed, showing the skin effect losses to be low enough when travelling over

short distances. While this analysis is promising, the problem of coupling into the TEM mode is a challenge not yet overcome. However, the analysis was still able to demonstrate a simple way of analyzing transmission losses in two wire transmission line systems.

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Appendix A

LIST OF ACRONYMS

IRLED – infrared light emitting diode

IR – infrared

LED – light emitting diode

IRSP – infrared scene projector

GaSb – gallium antimonide

CMOS – complementary metal oxide semiconductor

RIIC – read-in integrated circuit

MWIR – mid-wave infrared

FPA – focal plane array

UUT – unit under test

HWIL – hardware in the loop

TPA – thermal pixel array

SLED – superlattice light emitting diode

MBE – molecular beam epitaxy

BCS – balanced composite substrate

CTE – coefficient of thermal expansion

PCB – printed circuit board

CuW – copper-tungsten

IDE – integrated drive electronics

DAC – digital to analog converter

AMI – acetone, methanol, isopropanol

RIE – reactive ion etching

SEM – scanning electron microscopy

DVI – digital video interface

FPGA – field programmable gate array

CSE – custom support electronics

NUC- non-uniformity correction

TCSA – two color SLEDs array

NSLED – nightglow SLED

SWIR – short wave infrared

ROIC – read-out integrated circuit

PMOS – p-channel metal oxide semiconductor

NMOS – n-channel metal oxide semiconductor

ESD – electrostatic discharge

ICP – inductively coupled plasma

ESC – electrostatic chuck

BPFL – binary phase Fresnel lens

VLSI – very large scale integration

DC – direct current

AC – alternating current

TEM – transverse electromagnetic

VCSEL – vertical cavity surface emitting laser