THE FABRICATION AND CHARACTERIZATION OF ION-IMPLANTED GERMANIUM-INCORPORATED SILICON-CARBIDE DIODES AND TRANSISTORS

by

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A thesis submitted to the Faculty of the University of Delaware in partial fulfillment of the requirements for the degree of Master of Science with the major in Electrical and Computer Engineering.

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ABSTRACT

The unique material properties of Silicon-Carbide (SiC) make it a superior choice over Silicon or Gallium-Arsenide for applications in power electronics. Unfortunately, SiC semiconductor technology was only developed in recent years and its processes are still immature. Additionally, proper lattice matched compatible elements and alloy materials are rare, which gives other wide-bandgap materials, such as Gallium-Nitride, dominance. Furthermore, the well-established standard CMOS processes can not be applied to SiC in all cases. Finding proper complementary elements and alloys could bring SiC into competition with other wide-bandgap materials again. This thesis describes the incorporation of Germanium (Ge) in SiC as a way of bandgap engineering. Alloying with Germanium is believed to lower the bandgap of SiC, therefore using it to create heterojunction devices. I will introduce Ge-alloyed SiC heterojunction diodes, transistors and Schottky-barrier diodes, and address its advantages over their isomaterial devices. The design of the above mentioned devices will be reported, as well as all fabrication steps. Finally, a thorough analysis and evaluation will be concluded based on device measurements.

Chapter 1

INTRODUCTION AND MOTIVATION

For decades, Silicon (Si) has been the material dominating the semiconductor industry. Silicon-Carbide, a wide-bandgap semiconductor, however, has many superior properties when compared to Silicon, i.e. a higher thermal conductivity [1], a wider bandgap [2], and a higher reverse breakdown voltage [3, 4]. SiC could revolutionize the semiconductor industry in applications of high frequency [5], high power [6], and high temperature electronics [7]. Since research on SiC-based semiconductor devices started only in recent years, its process technology is still immature. Yet, promising developments for novel applications have been made already. These include high power Schottky-barrier diodes, which are commercially available for several years, as well as blue light emitting diodes (LED) made from SiC, i.e. at CREE® [8]. Recently, terahertz emitters fabricated from doped SiC were reported by our group [9]. Additionally, some other fundamental semiconductor devices were fabricated by different groups, including diodes [10], Field Effect Transistors (FET) [11], Bipolar Junction Transistors (BJT) [12], and Heterojunction Bipolar Transistors (HBT) [13].

1.1. Silicon-Carbide heterostructure research and motivation

Despite its superior properties, complementary elements and alloy materials, which are the backbones of novel devices, are hard to find for SiC. Finding complementary elements to create heterostructures could bring SiC-based devices back into competition with other wide-bandgap materials, i.e. Gallium-Nitride (GaN).

C. Guedj and J. Kolodzey studied Ge incorporation in 3C-SiC with a theoretical model [14]. In addition, G. Katulka et al. reported electrical and optical properties of 4H-SiC alloyed with Ge (4H-SiC:Ge) [15, 16]. Further on, K. Roe et al. fabricated a pnp heterojunction bipolar transistor (SiC:Ge-HBT) [13]. Adding these results of our group, Ge is promising to form SiC:Ge heterostructures, therefore changing its intrinsic properties.

Following my predecessor's footsteps, the motivation of this study and resulting thesis was to design diodes and npn HBT's. This would complement the Ge-alloyed device arsenal further, and prove the effectiveness of Ge introduction as a way of heterostructure formation and bandgap engineering. In collaboration with scientists from Northrop-Grumman these devices were designed, fabricated, and analyzed.

1.2. Outline of the thesis

In chapter 2, some important physical properties of both SiC and Ge will be introduced. Then, a brief review of the physical properties of the fabricated devices will be presented. Knowing the physical behavior of these devices, a careful derivation of the device design considerations will be given in chapter 3. Furthermore, chapter 3 contains the complete device fabrication process. Using several analytical tools, chapter 4 will cover all measurements performed on the diodes and transistors. Additionally, each result will be analyzed and evaluated. The conclusion of my Master's thesis will be presented in chapter 5, which will also include a prospect on future work.

Chapter 2

BACKGROUND INFORMATION ON THE HETEROJUNCTIONS AND DESCRIPTION OF SILICON-CARBIDE-BASED MATERIALS

In this chapter, the physical properties of 4H-Silicon-Carbide, Germanium, and Ge-incorporated SiC [15, 17] will be introduced. To serve this purpose best, the following three heterostructure devices will be presented. These devices have also been fabricated and analyzed (see chapter 3, 4). They are Germanium-incorporated SiC Schottky-barrier diodes (designated: SiC:Ge-SBD's), SiC heterojunction diodes (designated: SiC:Ge-JD's), and SiC heterojunction bipolar transistors (designated: SiC:Ge-HBT's). For the purpose of comparison, additional devices have been fabricated without Ge incorporation. The Ge-free counterparts of the above mentioned devices are SiC Schottky-barrier diodes (designated: SiC-SBD's), SiC homojunction diodes (designated: SiC-JD's), and SiC homojunction bipolar transistors (designated: SiC-BJT's), respectively. In the end this research could give one a direct comparison on the influence of Ge in SiC.

2.1. Physical properties of Germanium and 4H-Silicon-Carbide

In this section the physical properties of Ge, 4H-SiC, and a 4H-SiC:Ge alloy will be introduced.

2.1.1. Germanium as a material for bandgap engineering in Silicon-Carbide

An effective way to improve device performance is to lower the bandgap in the base of a transistor [18-20]. In the case of heterojunction diodes, a bandgap lowering in the p-type region was chosen to lower the barrier for electron flow [20]. SiC:Ge will alter the barrier height compared to plain SiC when forming a metal-semiconductor barrier. To lower the bandgap in the appropriate region of the above declared devices, a SiC:Ge alloy was formed. A linear interpolation was used to calculate the supposed change in bandgap, which yields a lowering of the bandgap of 4H-SiC by ΔE_G=27meV/at.% of Ge [13].

Previous work from our group shows the effectiveness of Germanium in Silicon-Carbide [i.e. 13-17]. K. Roe et al. fabricated a p-type 4H-SiC:Ge-HBT with an improvement of gain by more than 30% over a comparable homojunction transistor [13].

Table 2.1 Physical properties of 4H-Silicon Carbide and Germanium at 300K. The values for Ge are taken from Muller & Kamins (otherwise indicated) [20].

Physical properties:	**4H-Silicon-Carbide:**	**Germanium (diamond):**
Bandgap	3.23eV (indirect) [2]	0.67eV (indirect)
Density	$3.211 gcm^{-3}$ [21]	$5.32 gcm^{-3}$
Atomic density	$N_0=9.702*10^{22}cm^{-3}$ [22]	$N_0=4.42*10^{22}cm^{-3}$
Melting point	3103K ±40K at 35atm [23]	1210K
Lattice parameter	a=3.0730Å, c=10.053Å [24]	a=5.658Å
Atomic radius of Silicon	r=0.41Å* [25]	
Atomic radius of Carbon	r=0.91Å* [25]	
Atomic radius of Ge		r=0.53Å* [25]
Intrinsic carrier concentration	$n_i \sim =2.5*10^{-9}cm^{-3}$ [1]	$n_i=2.4*10^{13}cm^{-3}$
Electron mobility	$\mu_n \leq 900 cm^2(Vs)^{-1}$ [24]	$\mu_n=3900 cm^2(Vs)^{-1}$
Hole mobility	$\mu_p \leq 120 cm^2(Vs)^{-1}$ [24]	$\mu_p=1900 cm^2(Vs)^{-1}$
Electron affinity	qX=4.05eV [26]	qX=4.0eV
Diffusion length (n-type)	$L_p \sim =12 \mu m$ [24]	
Diffusion length (p-type)	$L_n \sim =1.5 \mu m$ [24]	

* Standard radii for ions in inert gas configuration.

2.2. The effect of Germanium on the device behavior of diodes and transistors

This section will carefully derive and explain the theoretical effects of Ge introduction on the 3 different devices, introduced at the beginning of chapter 2. These effects are based on theoretical considerations and actual data from experiments. But more research is needed to understand it better.

When introducing about 1 at.% of Ge into 4H-SiC, a linear interpolation of both bandgaps results in a theoretical lowering of the 4H-SiC bandgap of ΔE_G=27meV/at.% of Ge [13]. But it is not known how the conduction and valence bands are altered.

2.2.1. Schottky-barrier diode on a 4H-Silicon-Carbide:Germanium substrate

A metal-semiconductor barrier made with SiC is an excellent device for high voltage and high power applications (see introduction in chapter 1 and its references). Its wide bandgap exhibits a reverse breakdown field of about 3MVcm^{-1} and its thermal conductivity is about one order of magnitude higher than that of Gallium-Arsenide (GaAs) [27].

A Schottky-barrier diode is one of the most fundamental semiconductor devices. Therefore, the effect of Ge can be seen at the most fundamental level, without getting lost in too many device mechanisms.

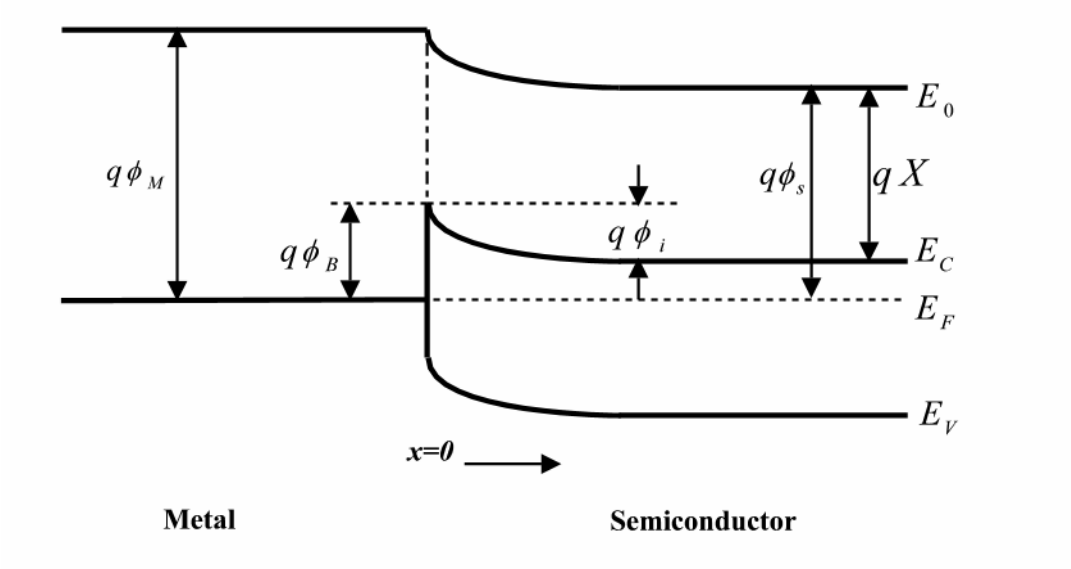

Figure 2.1 **The band-diagram of an n-type Schottky-barrier versus distance is shown. Important characteristics of this Schottky-barrier are the metal work function $q\varphi_M$, the electron affinity qX of the semiconductor, the barrier height φ_B, and the built-in potential φ_i [20].**

The difference in the work function of the metal and the electron affinity of the semiconductor leads to the barrier height. If subtracting the Fermi-level of the semiconductor with respect to the conduction band edge, one gets the built-in potential. The built-in potential provides the turn-on voltage for the Schottky-barrier diode (SBD). Titanium (Ti) was used to form the Schottky-barrier on the fabricated devices. The work function of Ti is 4.33eV [28], but to form a SBD, the contact needs to be annealed at 400°C [29]. Thus it forms an alloy at the surface to the 4H-SiC and its work function changes. In the case of 4H-SiC:Ge, the alloy and corresponding work function might be different compared to 4H-SiC. Hence, a theoretical evaluation is not so easily possible. Since this thesis is not about contacts, a more detailed analysis will not be assessed. Instead, the diode characteristics will be measured and the effect of Ge in 4H-SiC determined directly. The turn-on voltage may be in the range between 0.5V and 1V, as measured for Ti/n-type 4H-SiC [29]. Assuming that 1% Ge results in about 13meV change in the conduction band and valence band respectively, the change in the turn-on voltage can certainly be measured. Unfortunately, it is not yet clear where the band-offset occurs, nor the distinct mechanism for bandgap lowering. Strain induced by the Ge, could also be a mechanism of bandgap lowering [30]. The knowledge gained from these SBD's is crucial to understand the behaviors of the junction diodes and transistors too.

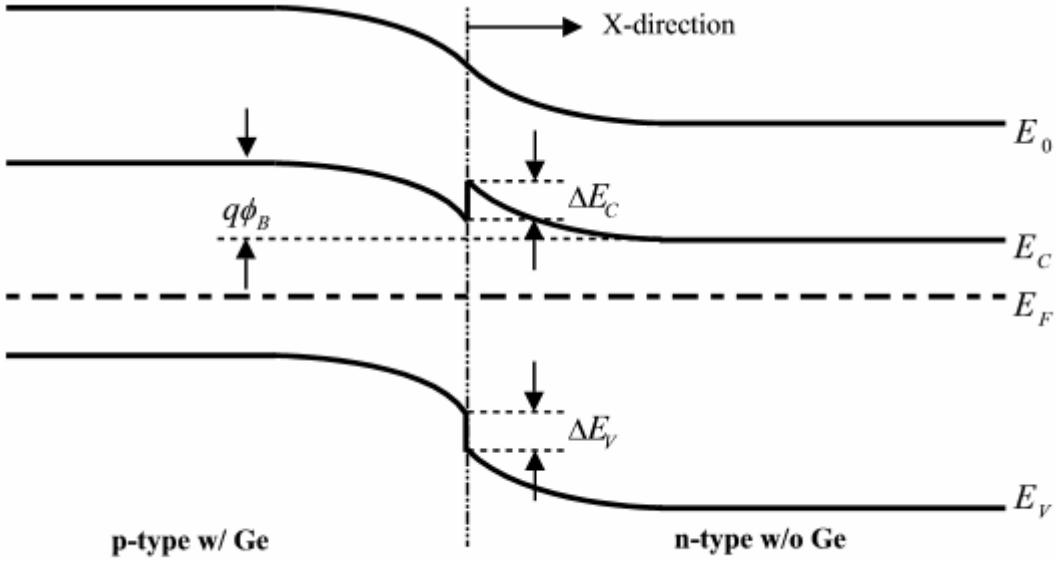

Figure 2.2 **Shown is the band-diagram of a pn-heterojunction diode. The band discontinuities ΔE_C and ΔE_V are assumed to be equal. The advantages of a heterojunction are that the barrier φ_B for electron injection is smaller than that for hole injection. It results in an improvement of many device parameters, including a lower turn-on voltage [20].**

2.2.2. Heterojunction diode on a 4H-Silicon-Carbide:Germanium substrate

Another fundamental device is the Junction Diode (JD). For high voltage applications, SiC junction diodes could have a great impact on current technology for their high break-down voltages and other advantages [3, 4].

The difference of a heterojunction diode compared to a homojunction diode is the band discontinuity. For the case shown, the electron injection into the p-type region must overcome a lower barrier compared to the injected holes into the n-type region (see Fig. 2.2). Thus, it results in a lower turn-on voltage and higher frequency response [20].

To obtain the ideal diode equation for a junction diode, the electron current and the hole current must be summed, since $J_{total} = J_n + J_p$ (2.1) [20]. For a heterojunction, J_n contains an additional factor, and the electron current is then $J_{n\_hetero} = J_n * \exp\left(\frac{\Delta E_G}{kT}\right)$ (2.2), where ΔE_G is the bandgap difference of the two materials and kT the temperature voltage [20]. The total current of the diode under bias can be written as $J_{total} = J_0 * \exp\left(\frac{\Delta E_G}{kT}\right)\left[\exp\left(\frac{qV_A}{kT}\right) - 1\right]$ (2.3) [20], where J_0 is the saturation current, of the diode, q the electron charge, and V_A the applied voltage. Equation 2.3 represents the ideal diode equation, whereas the actual diodes might deviate from that in several parameters.

In the following, one will find a comparison of the ideal diode equation and the real diode equation for homojunction diodes and heterojunction diodes as well [20]. The non-idealities of the junction can be expressed in the ideality factor n. Therefore, the equations containing the ideality factor n, are the real diode equations. Equation 2.4 and 2.5 can also be applied to Schottky-barrier diodes as described in section 2.2.1 [20].

Total current of a homojunction diode:

$$J_{total} = J_0 \left[e^{\frac{qV_A}{kT}} - 1 \right] \quad (2.4)$$

$$J_{total} = J_0 \left[e^{\frac{qV_A}{nkT}} - 1 \right] \quad (2.5)$$

Total current of a heterojunction diode:

$$J_{total} = J_0' \left[e^{\frac{qV_A}{kT}} - 1 \right] \quad (2.6) \text{ where } J_0' = J_0 * e^{\frac{\Delta E_G}{kT}} \quad (2.6a)$$

$$J_{total} = J_0' \left[e^{\frac{qV_A}{nkT}} - 1 \right] \quad (2.7)$$

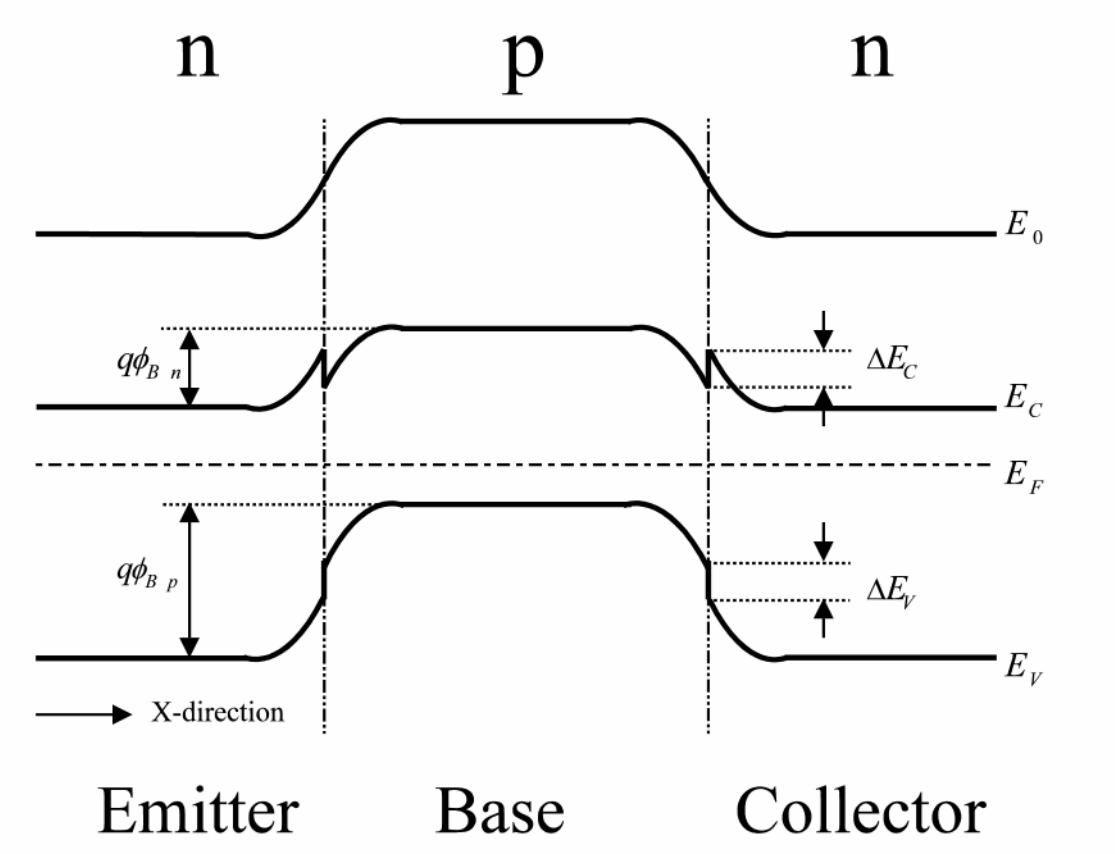

Figure 2.3 **The band-diagram of a double heterojunction bipolar transistor is shown [20]. The base is p-type with a smaller bandgap, while the emitter and collector are n-type with a wider bandgap. The bandgap lowering is achieved through Ge incorporation into the base. The bandgap difference ΔE_G of the heterojunction transistor is the sum of ΔE_C and ΔE_V.**

2.2.3. Double heterojunction bipolar transistor on a 4H-Silicon-Carbide:Germanium substrate

It is remarkable how little Ge in SiC is necessary to improve the gain of a transistor. The maximum gain of a single heterojunction bipolar transistor is exponentially dependent on its bandgap difference [19]. This makes the ion-implantation, despite its limitations to create large compositions, an adequate choice of fabrication tool.

In Fig. 2.3 one can see the main advantage of a heterojunction transistor, which is an advanced control of carrier flow. The main factor is the bandgap difference of the wide bandgap emitter to the narrow bandgap base. This bandgap difference determines the gain improvement over a homojunction device [19]. As believed, either the induced strain of Ge in SiC or the alloy composition of Ge and SiC may contribute to the bandgap lowering effect [13, 31]. The reason of choosing a double heterostructure over a single heterostructure lies in its easy process handling and the symmetry of electrical characteristics. Additionally, a double heterostructure has some dominant advantages in device performance compared to a single heterostructure [19].

$$\frac{I_n}{I_p} = \beta_{\max} = \frac{N_{n\_emitter}}{N_{p\_base}} * \frac{v_{dn\_base}}{v_{dp\_emitter}} \exp\left(\frac{\Delta E_G}{kT}\right) \quad (2.8)$$

In equation 2.8 the gain β_{max} of a heterojunction transistor is given by the ratio of I_n/I_p, approximately the ratio of electron to hole current [19]. N_{p_base} is the base doping concentration and $N_{n\_emitter}$ the doping concentration in the emitter. $v_{dn\_base}/v_{dp\_emitter}$ represents the ratio of the drift velocities of the minority carriers. In the case of a BJT the exponential term is one. Unfortunately, $v_{dn\_base}/v_{dp\_emitter}$, the ratio of the drift velocities of the minority carriers is not exactly known for the transistors that were fabricated. But it is still possible to make an estimation of the improvement of an HBT compared to a BJT, by focusing on the exponential term in equ. 2.8.

$$\beta_{\max\_HBT} = \beta_{\max\_BJT} * \exp\left(\frac{\Delta E_G}{kT}\right) \quad (2.9)$$

Assuming that the bandgap lowering in the base is ΔE_G=27meV [13], the resulting gain improvement (see equ. 2.9) is $\beta_{max\_HBT}=2.84*\beta_{max\_BJT}$. These calculations are based on the ideal diode equation whereas a real diode behavior will probably show a different gain improvement. But the essence of these calculations is obvious; a small amount of Ge in SiC may improve the gain considerably, which is the motivation of this research.

Chapter 3

DESIGN AND FABRICATION OF THE DIODES AND TRANSISTORS

After describing the general physical properties of the diodes and transistors already, the device design and the fabrication steps will be presented in this chapter.

3.1. General device design considerations and limitations

To design the devices appropriately, not only the exact SiC substrate parameters (i.e. doping concentration, epitaxial layers, etc.) had to be known, but also the capabilities of the ion-implanter, available target material sources, manufacturing procedures, and practical design rules. In this section, the SiC:Ge alloy formation technique and the available 4H-SiC wafers will be introduced.

3.1.1. Silicon-Carbide:Germanium alloy formation

The alloy formation was planned to be done through ion-implantation of Ge into the 4H-SiC substrate. Scientists from Northrop-Grumman offered to do the ion-implantation of Germanium as an alloy material and Aluminum (Al) as a p-type dopant. The ion-implanter used, is limited to a maximum energy of 195keV. Since Ge has a smaller implantation depth compared to Al for a given energy, Ge was the limiting depth parameter for the design [22]. It was decided to implant ~1 at.% Ge into SiC. The amount was derived from pervious research in our group [31]. 1 at.% Ge is believed to correspond to a bandgap lowering of 27meV [13]. Having a bandgap difference on the order of the thermal voltage kT, it should be sufficient to see the change in device behavior.

3.1.2. 4H-Silicon-Carbide wafer substrates

Two 3" 4H-SiC (n-type) wafers were generously provided by Northrop-Grumman for this purpose. Their donor concentration is about $2*10^{18}cm^{-3}$. On each wafer, two epitaxial layers were grown prior to my device fabrication. These layers correspond to the design of a Static Induction Transistor (SIT), for which the wafers were originally designed. The bottom layer is called a drift layer and the upper layer a channel layer. Table 3.1 shows the properties of the epitaxial layers.

Table 3.1 **Listed are the doping concentration and thickness of the preprocessed epitaxial layers.**

Wafer ID:	Channel doping:	Channel layer thickness:	Drift doping:	Drift layer thickness:
BX0178-04	$1.04*10^{16}cm^{-3}$	1.21µm	$3.85*10^{15}cm^{-3}$	2.64µm
FW0065-08	$2.83*10^{16}cm^{-3}$	1.00µm	$4.71*10^{15}cm^{-3}$	2.11µm

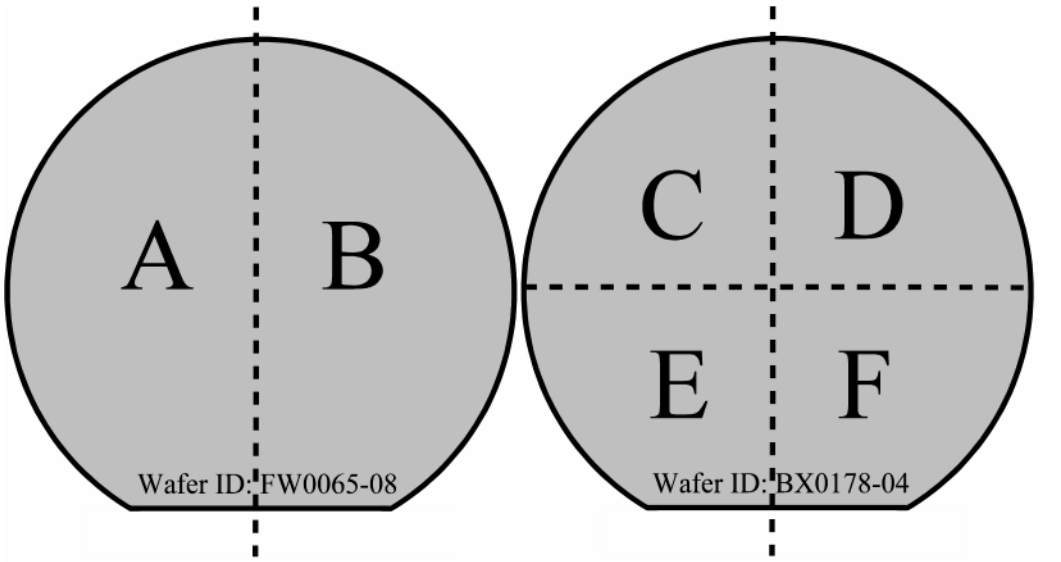

Figure 3.1 **Shown are the designated areas for each device category that was designed and fabricated. Table 3.2 shows the corresponding device category on the wafer parts A to F.**

Table 3.2 Implanted areas and device allocation of Fig. 3.1 are shown.

Wafer part in Fig. 3.1:	Implantation:	Corresponding devices:
A	Aluminum	SiC-BJT's
B	Al and Ge	SiC:Ge-HBT's
C	unimplanted	SiC-SBD's
D	Ge	SiC:Ge-SBD's
E	Al	SiC-JD's
F	Al and Ge	SiC:Ge-JD's

3.2. Design of the diodes and transistors

Following a chronological guideline, this section will focus on the practical development of my choice of design for the transistors and diodes respectively. This section will begin with the design of the bipolar transistors, whose design was the guideline for the diodes too. To optimize the cost-efficiency, all implantations were simulated and processed with the same energy and dose for all devices. Careful considerations and calculations will be described that made it possible without sacrificing device performance.

3.2.1. Design of the heterojunction bipolar transistors

Ion-implantation, a well-established processing tool, was considered to serve my purpose best for Ge incorporation. The most crucial parameter in the transistor design is the implantation depth of Ge in SiC. Several approaches are possible to achieve a heterostructure design. Ge implantation only into the base region of the transistor was chosen, therefore creating a double heterojunction with respect to the emitter and collector regions.

To estimate the implantation depth and profile of Ge and Al, an implantation simulation software was used. "The Stopping and Range of Ions in Matter", SRIM, is capable to simulate a 3-dimensional implantation profile, using Monte-Carlo calculations [22]. Two implantations with different energies for each element exhibited good results and a nearly uniform impurity concentration. A high Ge concentration at the surface was necessary to reach the maximum bandgap difference. Hence, a 500Å thick sacrificial SiO_2 layer was deposited on the surface of the substrate prior to the implantation and also included in the simulations. The sacrificial layer, as indicated in Figs. 3.2 and 3.3, diminishes lattice damage and channeling due to the highly energetic ions, and when removed, the wafer surface is left with a very high impurity concentration. In the same way, Al as a p-type dopant was simulated and implanted to the same depth as Ge to form the base region of the transistor. The simulated impurity profiles are seen in Figs. 3.2 and 3.3.

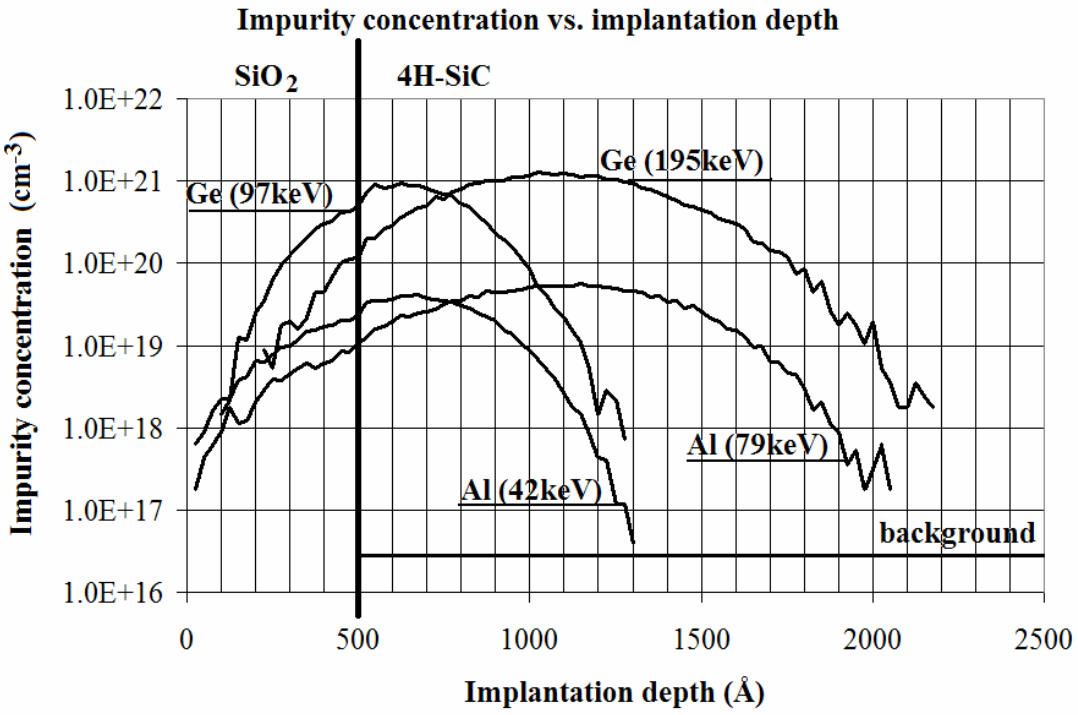

Figure 3.2 **Individually implanted impurity concentration profiles versus implantation depth as simulated with SRIM. Shown are the separated implantation profiles of all four implantations. The 1st 500Å is a sacrificial SiO_2 layer. These profiles apply to the junction diodes too.**

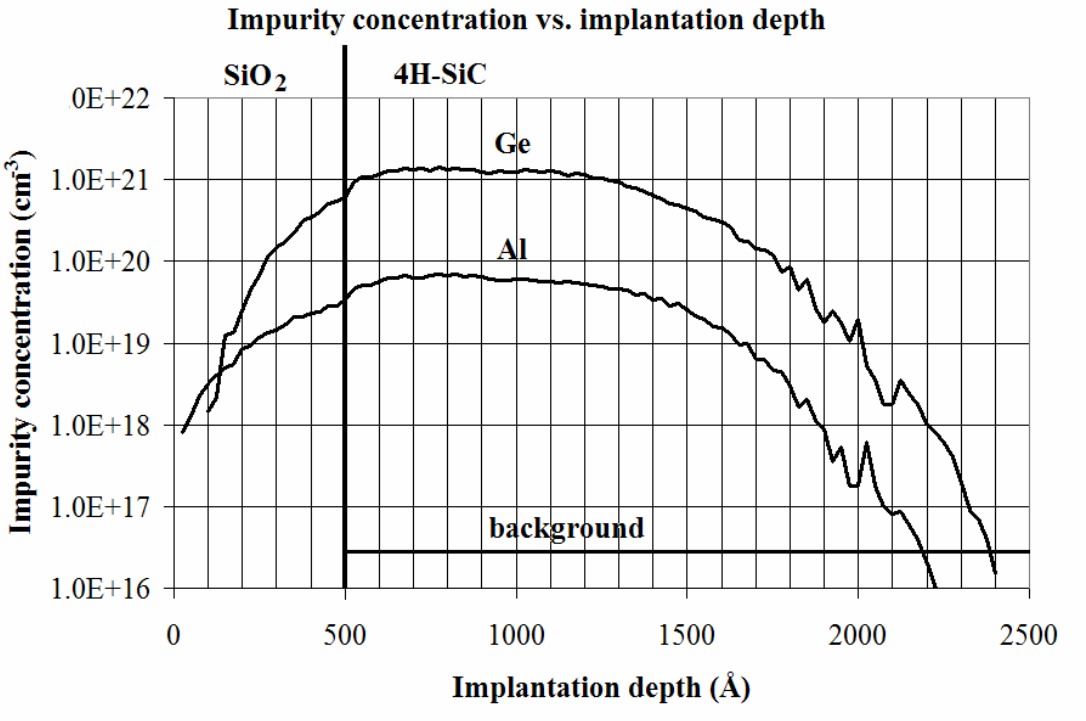

Figure 3.3 **Overall impurity concentration profile versus implantation depth as simulated with SRIM. Shown are the actual impurity profiles of Ge and Al. The 1st 500Å is a sacrificial SiO_2 layer. These profiles apply to the junction diodes too.**

Table 3.3 **Shown are the values of energy and dose for each element, determined by SRIM simulations, and also used for the ion-implantation. These results were also used for the junction diodes respectively.**

Impurity:	**Implantation energy:**	**Implantation dose:**	**Max. implantation concentration per element:**
Ge	195 keV	$9.0*10^{15}cm^{-2}$	$1.1*10^{21}cm^{-3}$
Ge	97 keV	$3.6*10^{15}cm^{-2}$	--
Al	79 keV	$4.4*10^{14}cm^{-2}$	$7.0*10^{21}cm^{-3}$
Al	42 keV	$2.0*10^{14}cm^{-2}$	--

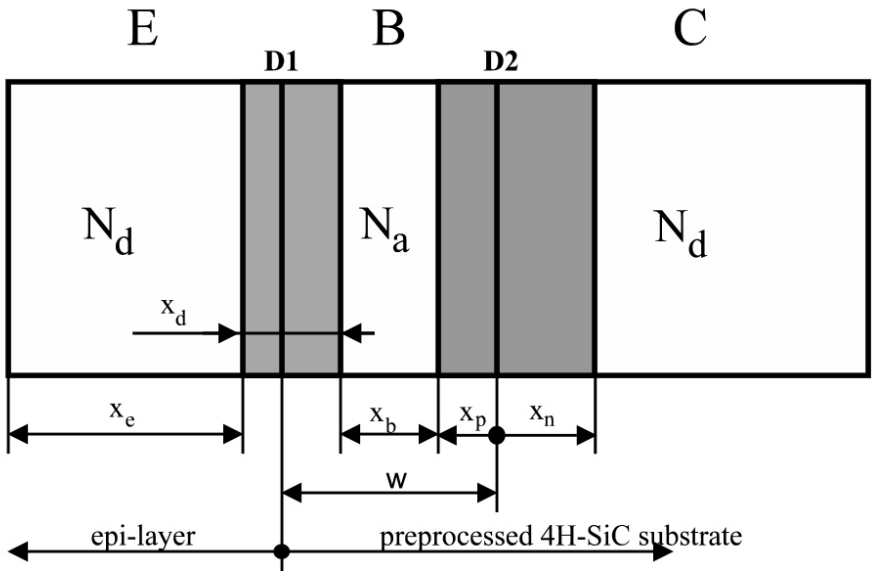

Figure 3.4 **Shown is a simplified transistor sketch where the grey regions are the depletion regions of the base-emitter diode (D1) and collector-base diode (D2) respectively. W is the physical base width as simulated with SRIM and x_b the quasi-neutral base region. X_e is the quasi-neutral emitter region.**

After the base width and profile was known, the dopant concentrations of the emitter and base could be calculated. On the left-hand side of Fig. 3.4 the n-type emitter layer is shown. It was designed to be an epitaxial layer deposited after implantation. On the right-hand side the collector is shown with its fixed doping concentration and therefore determined the doping concentration of the base and emitter. For transistor layer thickness design, the most crucial parameters are the depletion region of the base-emitter diode and collector-base diode extending into the base region. The depletion extensions have to be less than the physical base width, even under bias. The remaining quasi-neutral region (x_b) should be small, resulting in high gain.

Assuming a step-junction doping profile of D1 and D2 in Fig. 3.4, the following equations apply to calculate the depletion regions and doping concentrations. This approximation is valid since the diffusion length of the minority carriers is much larger than the base and emitter regions and the implantation profile is nearly rectangular [20].

The depletion width of a step-junction:

$$N_a x_p = N_d x_n \quad (3.1)$$

$$x_d = x_n + x_p = \left[2\frac{\varepsilon_s}{q}\phi_i \left(\frac{1}{N_a} + \frac{1}{N_d} \right) \right]^{1/2} \quad \text{[no bias applied]} \quad (3.2)$$

$$x_d = x_n + x_p = \left[2\frac{\varepsilon_s}{q} \left(\frac{1}{N_a} + \frac{1}{N_d} \right) (\phi_i - V_A) \right]^{1/2} \quad \text{[bias applied]} \quad (3.3)$$

$$\phi_i = \frac{kT}{q}\ln\frac{N_d}{n_i} + \frac{kT}{q}\ln\frac{N_a}{n_i} = \frac{kT}{q}\ln\frac{N_a N_d}{n_i^2} \qquad (3.4)$$

In equations 3.1 to 3.4 [20], N_a is the accepter concentration in the base, N_d the donor concentration in its designated region, x_n the depletion width extending into the n-type region, x_p the depletion width extending into the p-type region, and ε_s is the dielectric constant of 4H-SiC.

Applying equations 3.1 and 3.4 with its physical parameters described in chapter 2, the impurity concentrations in table 3.4 were found to satisfy my application best. These values were carefully developed by considering the depletion regions and the general design rules of a BJT. Since this implantation process and post-annealing was known to yield about 1% activated Al dopants, an actual Al impurity concentration of $7.0*10^{19}cm^{-3}$ was implanted. The minimum quasi-neutral base width under 10V collector to emitter voltage was calculated to be about 1000Å. The physical base width was determined to be 1600Å through SRIM simulations. This means, the physical base width gets reduced by about half its size when under normal working condition. The quasi-neutral region is relatively small and the weak spot of the device, but if processing carefully, a high gain should be reached. The epitaxial emitter layer was chosen to be 2500Å thick and therefore much wider than the depletion width extending into the emitter region.

Table 3.4 **Simulated and incorporated impurity concentrations in each layer of the transistor.**

Transistor layer:	**Impurity concentration:**
Collector: (values fixed)	$N_{d\_coll}=2.8*10^{16}cm^{-3}$
Base: (Aluminum)	$N_{a\_base}=7.0*10^{17}cm^{-3}$
(Germanium)	$N=1.1*10^{22}cm^{-3}$
Emitter (Nitrogen)	$N_{d\_emit}=2.0*10^{19}cm^{-3}$

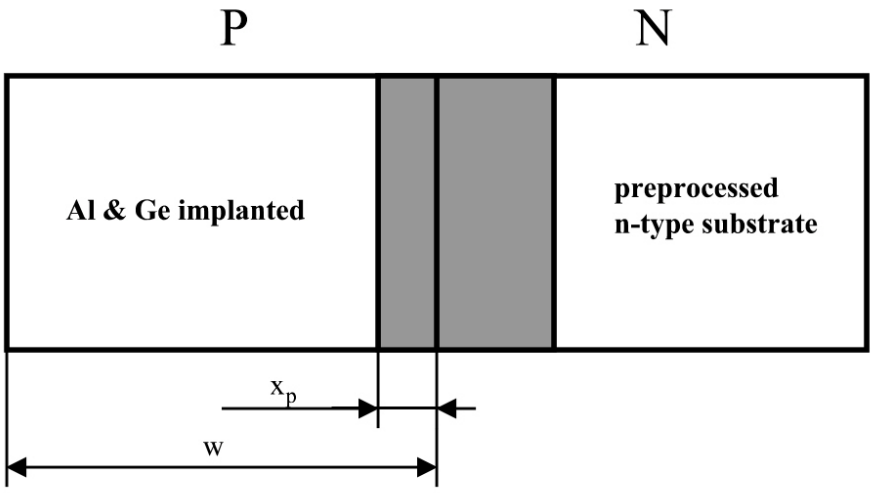

Figure 3.5 **The design of the 4H-SiC:Ge-JD is shown in this figure. The grey shaded area is the depletion region of the pn-junction. The preprocessed 4H-SiC substrate was implanted with Ge ($N_{Ge}=1.1*10^{21}cm^{-3}$) and Al ($N_{Al}=7.0*10^{19}cm^{-3}$) as shown in Fig. 3.3. The physical junction depth w is at approximately 1600Å. The extension x_p of the depletion region into the p-type material was calculated to be about ~300Å.**

3.2.2. Design of the heterojunction diodes

The p-type region of the 4H-SiC:Ge-JD was formed by ion-implantation of Ge and Al respectively, as described in section 3.2.1 for the transistors. Therefore their simulation results were used too. Using equation 3.4, the calculated built-in voltage φ_i is 3.07eV. It should result in a turn-on voltage of approximately 2.5…3 Volts.

As in the case of the transistors a complete theoretical analyses was not possible because some of the material properties were not exactly known. Therefore, homojunction diodes were designed too. Their purpose was to evaluate the differences and advantages of the Ge-containing devices. Additionally, the comparison of the measured devices with the ideal diode equation (equ. 2.6), will give one another perspective of the real junction behavior.

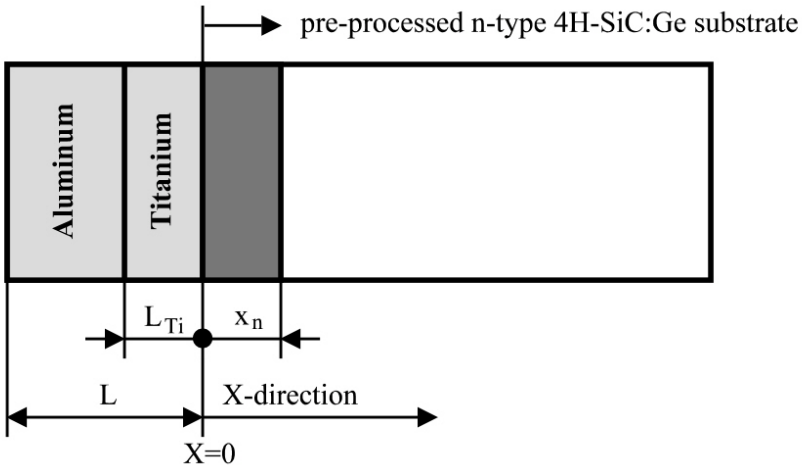

Figure 3.6 **Layer diagram of a Schottky-barrier diode [20]. Titanium with a thickness L_{Ti} of 600Å was chosen to form the Schottky-barrier. To achieve a high quality ohmic contact to exterior measurement probes, Al was deposited on Ti. The whole metal thickness L is 3100Å. The depletion region x_n formed at the semiconductor–metal barrier extends virtually only into the 4H-SiC:Ge substrate.**

3.2.3. Design of the Schottky-barrier diodes

The barrier formation is due to the difference in the work function of the metal and the electron affinity of the semiconductor as indicated in Fig. 2.1. Hence, their should be a measurable difference between the SiC:Ge-SBD's and SiC-SBD's.

Good results were obtained by using Ti/Al contacts for Schottky-barrier formation on n-type SiC, whereas Ti/Al contacts on p-type SiC substrates are known to be ohmic [32]. Certainly, a theoretical prediction of the contact properties is not so easily obtained, since the work function of the annealed metal-semiconductor alloy is different compared to the intrinsic Ti work function.

3.3. Device fabrication

In this section the device processing will be described. After device design, Dr. G. DeSalvo, Dr. J. Oliver, Dr. J. Gigante, Dr. G. Storaska and M. McCoy performed the ion-implantation, wafer annealing, and epitaxial growth. Then, the wafers were shipped to me for further processing.

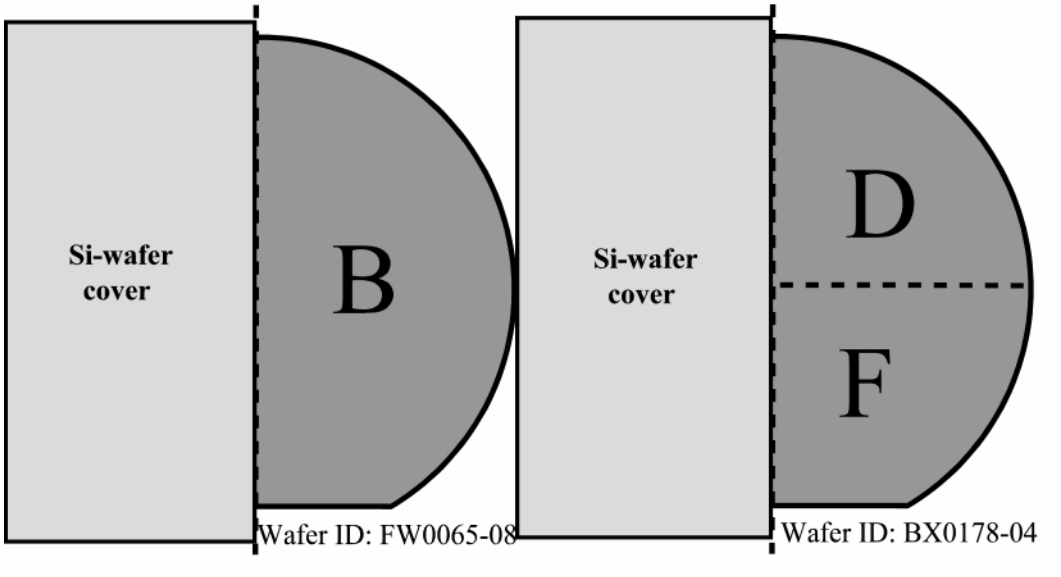

Figure 3.7 ***Ge implantation*: Shown is the top-view of both wafers. FW0065-08 was implanted with Ge only on its right half for the SiC:Ge-HBT's (B), whereas the left part was covered with a sacrificial Si wafer mask to avoid Ge implantation for the SiC-BJT's. BX0178-04 was implanted the same way, forming the alloy for SiC:Ge-SBD's (D) and SiC:Ge-JD's (F).**

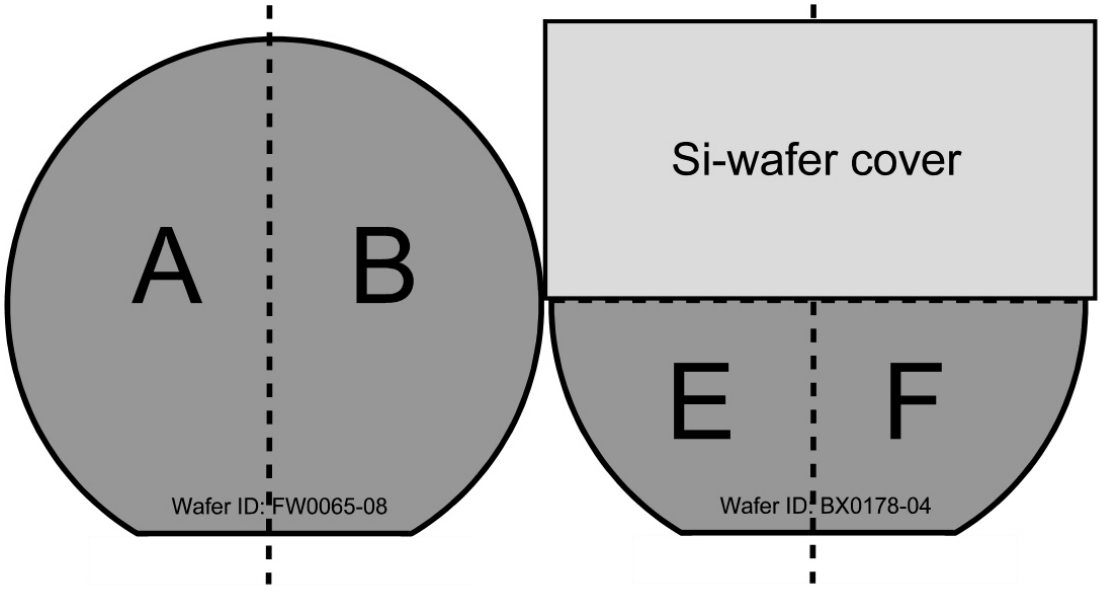

Figure 3.8 ***Al implantation*: Shown is the top-view of both wafers. FW0065-08 was implanted with Al on its whole surface to form the base layer for the SiC-BJT's (A) and SiC:Ge-HBT's (B). The lower part of BX0178-04 was implanted with Al, forming the p-type region for SiC-JD's (E) and SiC:Ge-JD's (F).**

3.3.1. Wafer implantation and post-annealing

As described in section 3.1.2, the wafers FW0065-08 and BX0178-04 were preprocessed with 2 epitaxial layers. After wafer wet cleaning, a 550Å thick tetraethoxysilane (TEOS) layer was deposited with Plasma Enhanced Chemical Vapor Deposition (PECVD) on both wafers. The TEOS layer was densified at 950ºC for 30min in dry oxygen, resulting in a 500Å SiO_2 layer. The SiO_2 layer was used to form an implantation sacrificial surface region. Its basic functions are diminishing lattice damage, channeling inhibition, and when stripped in Buffered Hydrofluoric Acid (BHF), a high impurity concentration at the surface of the wafer substrate is left. As shown in Figs. 3.7 and 3.8, the wafers were then partly covered with a Silicon wafer mask to prepare the 6 different devices for ion-implantation. The implantation process took several hours. First, the desired ion source needed to be outgased and stabilized at 1000ºC. During that time the wafers were being loaded. The wafer heat-up cycle took only a couple of minutes. The first element to be implanted was Ge.

Table 3.5 Shown are the implantation parameters for each implantation process.

Implantation parameters:	**1st Ge implantation:**	**2nd Ge implantation:**	**1st Al implantation:**	**2nd Al implantation:**
Ion energy	195keV	97keV	79keV	42keV
Dose	$6.7*10^{15}cm^{-2}$	$3.0*10^{15}cm^{-2}$	$4.0*10^{14}cm^{-2}$	$1.92*10^{14}cm^{-2}$
Ion beam current	~10μA	~10μA	~200μA	~100μA
Impl. duration	~3hrs	~1hr	~30sec	~30sec

After Ge implantation, the wafers were cooled down over several hrs and the Si wafer covers were changed as shown in Fig. 3.8 for the Al implantation. The time scheduled to change the ion source was about 4hrs. Using the same wafer heat-up process, Al was implanted in two steps.

With the intention to activate the Al impurities and cause Ge to become substitutional, both wafers were scheduled for post-annealing. After SiO_2 removal, a graphite sheet was deposited on the wafer surface to avoid out-diffusion during post-annealing. Annealing was then done in an Argon ambient at 51kPa and at 1675ºC for 30min.

3.3.2. Emitter epitaxial layer growth

After implantation and post-annealing, I received BX0178-04 for further processing, whereas on FW0065-08 Dr. Oliver performed an epitaxial layer growth of the transistor emitter region. This Chemical Vapor Deposition (CVD) growth was done in a Planetary Reactor® [33]. It is configured for 5 three inch wafers, each rotating individually on a platen. The atmosphere was hydrogen and argon was used to purge the chamber. The heat-up process of the chamber including samples took about one hour, as well as the cooling-down cycle. Prior to the growth initiation, a hydrochloric acid (HCl) surface etch was done at 1400ºC. The actual growth data are listed in Table 3.6.

The substrate etchback in the hydrogen ambient was the most crucial parameter prior to growth initiation. A careful heat-up procedure prevented an etchback of more than 10nm. This was important to avoid base width reduction.

The variation in doping concentration over the whole wafer surface was less than 7% and the variation in layer thickness less than 3%. After processing, the wafer was shipped to me for further processing.

Table 3.6 **Shown are the CVD growth parameters of the epitaxial emitter layer growth.**

Growth parameters:	**Values:**
Growth temperature	1600ºC
Growth pressure	50kPa
Gases	Silane, Propane
Dopant	Nitrogen
C/Si ratio	0.8...1.3
Growth rate	2µm/hr
Thickness	240nm
Growth time	~7min
Actual doping concentration	$1*10^{19}cm^{-3}$

Table 3.7 **Shown is the positive mask-set used in photolithography to fabricate the diodes and transistors. The inner diameter of the annuli is designated d_{in} and the outer diameter d_{out}.**

Mask #:	Purpose:	Features:	Feature size: (d_{in} / d_{out})	Surface area: (cm^2)
mask # 1	base etch		240µm / 480µm	base: $1.01*10^{-3}$ emitter: $4.52*10^{-4}$
mask # 2	collector etch		440µm / 680µm	collector: $1.82*10^{-3}$
mask # 3	emitter contact		--- / 200µm	$3.14*10^{-4}$
mask # 4	base contact		280µm / 400µm	$6.41*10^{-4}$
mask # 5	collector contact		520µm / 640µm	$1.83*10^{-4}$

3.3.3. Photolithography and pattern transfer

3.3.3.1. Junction diode and Schottky-barrier diode fabrication process

First, from all four parts of BX0178-04 (see Fig.3.1) small pieces (~2X2cm) were produced for further processing. Two masks for etching and metal contact deposition were used. Mask# 2 (see table 3.7) was used to etch annular trenches into the substrate to isolate each individual device. Mask# 4 was used to deposit one set of metal contacts. On the backside of the substrates, a continuous metal layer was deposited in a further process step to contact the two-terminal devices. Fig. 3.9 shows a side-view of the completed devices.

Reactive Ion Etching (RIE) was performed on a Plasmatherm 790 [34]. The following recipes were used to clean and etch the SiC devices.

RIE process # 1 (chamber cleaning) is composed of:

1. Evacuation of the chamber to $1*10^{-5}$Torr
2. Purge chamber with Nitrogen to 200mTorr
3. Evacuate to $5*10^{-5}$Torr

4. Plasma etching between 1 to 5min
    a. chamber pressure = 150mTorr
    b. process gas = 20sccm oxygen
    c. plasma power = 100W
5. To increase the cleaning time, loop to point 3.

RIE process # 2 (etching) is composed of:

1. Evacuation of the chamber to $1*10^{-5}$Torr
2. Purge chamber with Nitrogen to 200mTorr
3. Evacuate to $5*10^{-5}$Torr
4. Plasma etching between 1 to 5min
    a. chamber pressure = 30mTorr
    b. plasma power = 30W
    c. Hydrogen = 16sccm
    d. Sulfur Hexafluoride (SF6) = 8sccm
5. To increase the etch time, loop to point 3.

The etch rate was ~12nm/min. This recipe was designed to perform mainly ion-milling.

The following listing describes the processing steps performed on the diodes for pattern transfer:

1. Wafer wet cleaning of all 4 diode substrates
    a. H_2SO_4:H_2O_2 = 4:1 for 10min
    b. HCl:H_2O_2:H_2O = 1:1:1 for 10min
    c. BHF for 1min
2. Oxygen plasma chamber cleaning (process # 1)
    - duration = 90min
3. RIE etching of substrates front to roughen surface (process # 2)
    - duration = 3min
    - etch depth = ~120Å
4. RIE etching of substrates backside to roughen surface (process # 2)
    - duration = 3min
    - etch depth = ~120Å
5. Wafer wet cleaning of all 4 diode substrates
6. Transferring Mask # 2 patterns onto all 4 substrates
    - using AZ5214 positive photoresist

7. RIE etching of trenches (process # 2)
    - duration = 60min
    - etch depth = 6000Å
8. Resist removal by Acetone

3.3.3.2. Transistor fabrication process

The transistors were fabricated similarly to the diodes. The mask-set of table 3.7 and the RIE processes explained in section 3.3.3.1 were used on small parts of FW0065-08. I will now list the photolithography and etching procedure. The description of the procedures described in section 3.3.3.1 will be shortened in the following steps:

1. Wafer wet cleaning of substrates
2. Oxygen plasma chamber cleaning (process # 1)
3. RIE etching of substrates backside to roughen surface (process # 2)
4. Transferring Mask # 1 patterns onto both substrates
5. Oxygen plasma chamber cleaning (process # 1)

6. RIE etching of transistor base (process # 2)
    - duration = 27min
    - etch depth = 3000Å
7. Resist removal by Acetone
8. Transferring Mask # 2 patterns onto both substrates
9. Oxygen plasma chamber cleaning (process # 1)
10. RIE etching of transistor collector / device isolation (process # 2)
    - duration = 62min
    - etch depth = 7200Å
11. Resist removal by Acetone.
12. Transferring Mask # 3 patterns onto both substrates
13. Oxygen plasma chamber cleaning (process # 1)
14. RIE etching of substrate emitter to roughen surface (process # 2)
15. Resist removal by Acetone.

Fig. 3.10 shows the transistors after fabrication.

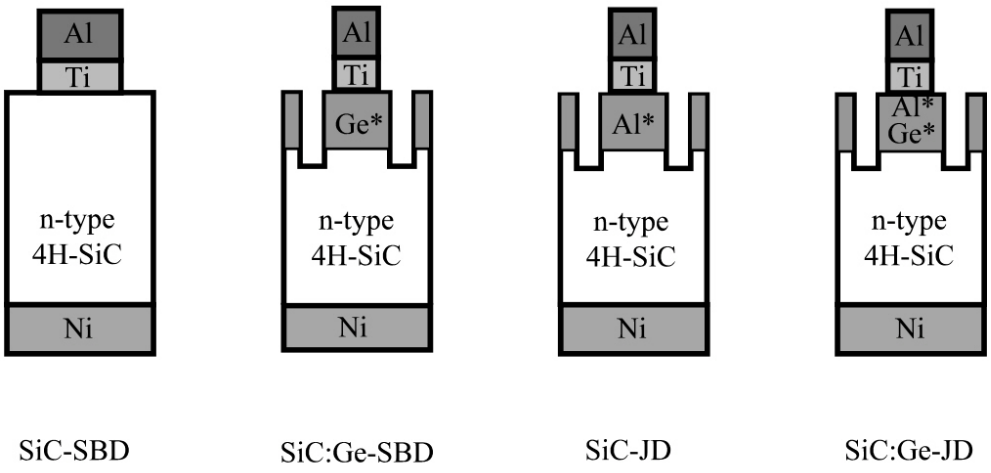

Figure 3.9 **Side-view of all manufactured diodes. SiC-SBD = Schottky barrier diode w/o Ge – part C in Fig. 3.1. SiC:Ge-SBD = Schottky barrier diode w/ Ge – part D in Fig. 3.1. SiC-JD = homojunction diode – part E in Fig.3.1. SiC:Ge-JD = heterojunction diode w/ Ge – part F in Fig. 3.1. The backside Nickel (Ni) ohmic contact is 1500Å thick. Etched trenches are 6000Å deep. Titanium is 600Å thick and Al is 2500Å thick. *The upper grey shaded area of the 4H-SiC substrate indicates impurity incorporation through ion-implantation. Its depth is about 1600Å.**

3.3.4. Metallization and contact annealing

3.3.4.1. Metal deposition and contact annealing of the diodes

After etching, metal contacts had to be deposited to access the two-terminal devices. As mentioned in chapter 2, Ni was used to form the backside ohmic contact. And on the front a two step Ti/Al contact metal deposition was made to form Schottky-barrier contacts on n-type SiC and Schottky ohmic contacts on p-type SiC.

The processing steps for the metal contacts and annealing procedure are listed below:

1. Organic solvent cleaning of all samples
    a) Acetone for 10min + mechanical impurity removal
    b) Methanol dip
    c) Isopropanol dip
2. Evaporation of Ni on wafer backside
    - evaporation technique = electron beam evaporation
    - chamber pressure = $1*10^{-6}$Torr
    - evaporated thickness = 1550Å
    - evaporation rate = 3Å/sec

3. Ni contact annealing [35] of SiC:Ge-SBD's and SiC-SBD's

    - annealing technique = Heatpulse® 610 [36]; rapid thermal annealing
    - inert gas = compressed Nitrogen, grade 4.8

    a) outgas oxygen and H_2O at 150ºC for 10min

    b) heat-up to 950ºC at 50ºC/sec

    c) anneal 120sec @ 950ºC

    d) cool down to <300ºC at 10ºC/sec

4. Organic solvent cleaning of all samples

5. Transferring Mask # 4 patterns onto all four substrates

    - using AZ5214 positive photoresist

6. Evaporation of Ti on wafer frontside of all samples

    - evaporation technique = electron beam evaporation
    - chamber pressure = $1*10^{-6}$Torr
    - evaporated thickness = 620Å
    - evaporation rate = 2Å/sec

7. In-situ evaporation of Al on wafer frontside of all samples

    - evaporation technique = electron beam evaporation
    - chamber pressure = $1*10^{-6}$Torr
    - evaporated thickness = 2450Å
    - evaporation rate = 2.5Å/sec
    - lift-off Ti/Al remnants by Acetone

8. Ni, Ti/Al contact annealing [32, 35] of SiC:Ge-JD's and SiC-JD's
    - see point 3
9. Ti, Al contact annealing [29] of SBD's
    - annealing technique = rapid thermal annealing
    - inert gas = compressed Nitrogen, grade 4.8

    a) outgas oxygen and H_2O at 150ºC for 10min

    b) heat-up to 450ºC at 20ºC/sec

    c) anneal 300 sec @ 450ºC

    d) cool down to <300ºC at 10º/sec

The deposited contacts adhered to the substrate quiet well during annealing. The nitrogen ambient caused oxidation on the deposited contacts, which was determined by visual inspection. This means that some oxygen must have been present during contact annealing. Further annealing will be done with forming gas (95% N / 5% H) to remove all oxygen from the chamber.

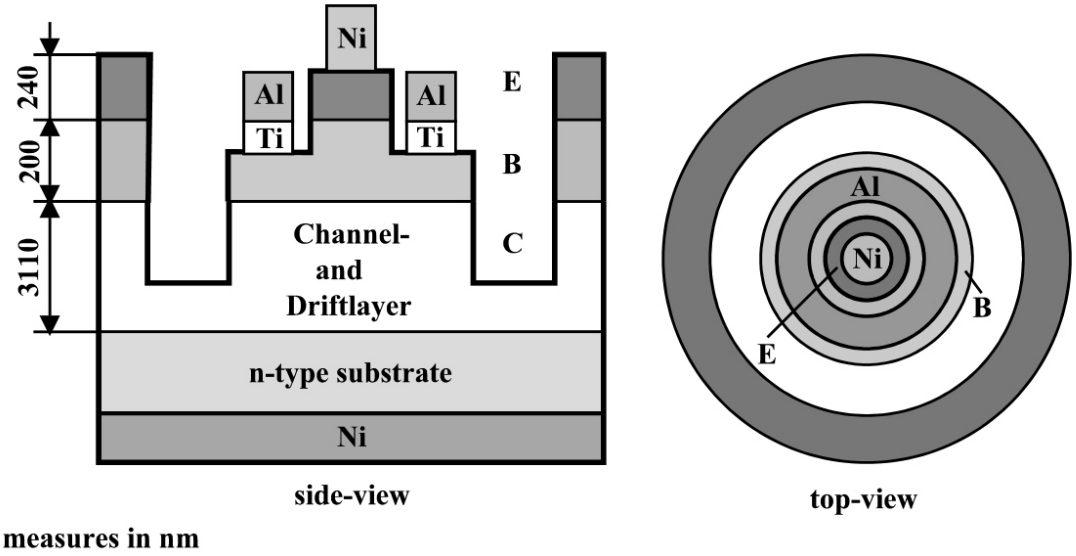

Figure 3.10 **Shown are the side-view and top-view of the transistors after fabrication. Ohmic Ni contacts were used for the emitter (top) contact and collector contact (bottom) respectively. Ti/Al formed the ohmic base contact. A 720nm deep trench was etched to isolate each device.**

3.3.4.2. Metal deposition and contact annealing of the transistors

Like in section 3.3.4.1, metal contacts had to be deposited and annealed. The n-type ohmic contacts were made by Ni deposition and the p-type ohmic contact with Ti/Al.

Following, I will list the deposition and annealing procedure for the SiC:Ge-HBT's and SiC-BJT's. Since its procedure is similar to the description in section 3.3.4.1, I will state it in a compressed form.

1. Organic solvent cleaning of all samples
2. Evaporation of 1600Å Ni on wafer backside
3. Organic solvent cleaning of transistor samples
4. Transferring Mask # 3 (emitter contacts) patterns onto substrates
5. Evaporation of 2200Å Ni on wafer front for emitter contacts
6. Lift-off Ni remnants by Acetone
7. Organic solvent cleaning of all samples
8. Transferring Mask # 4 (base contacts) patterns onto substrates
9. Evaporation of 600Å Ti on wafer front for base contacts
10. In-situ evaporation of 2500Å Al on wafer front for base contacts
11. Lift-off Ti/Al remnants by Acetone
12. Organic solvent cleaning of all samples

13. Ni, Ti/Al contact annealing [32, 35] of SiC:Ge-HBT's and SiC-BJT's

- annealing technique = rapid thermal annealing
- purge gas = forming gas (95%N/5%H)

a) outgas oxygen and H_2O at 150ºC for 10min

b) heat-up to 950ºC at 50ºC/sec

c) anneal 150 sec @ 950ºC

d) cool down to <300ºC at 10ºC/sec

Annealing was done in a forming gas atmosphere instead of 4.8 grade Nitrogen. Hence, the contacts showed much less oxidation. But the contacts had some microscopic cracks, which might be due to the long annealing time.

The deposited SiC-BJT contacts adhered well to the substrate during annealing. However, the deposited contacts on the SiC:Ge-HBT's peeled off very easily before annealing. The reason is yet unclear to me.

Chapter 4

DEVICE MEASUREMENTS AND EVALUATION

In this chapter measured current versus voltage (IV) characteristics will be shown. These characteristics were measured on a Cascade™ Microtech Probe Station [37], equipped with a HP (Agilent) 4156B Precision Semiconductor Parameter Analyzer. Semi-logarithmic plots and linear plots will be compared to analyze their results best. Additionally, capacitance versus voltage (CV) characteristics will be presented. CV measurements were obtained on the same probe station, equipped with a HP (Agilent) 4284A Precision LCR Meter. All measurements were performed at room temperature (~300K). The chapter will be concluded with Transmission Electron Microscopy (TEM) images, X-Ray Diffraction (XRD) spectra and an evaluation of measurements.

4.1. Diode measurements and results

To normalize the measurement results, current densities were used instead of the actual currents. By knowing the active contact area of $6.41*10^{-4}cm^2$ (SBD's) one can easily calculate the actual measured currents. In the case of the JD's the active device area will listed in the appropriate sections. Furthermore, the HP (Agilent) 4156B semiconductor parameter analyzer is limited to ≤100mA – hence the lateral current limiting of the IV curves.

4.1.1. Measurements of the Schottky-barrier diodes

IV and CV measurements on both Schottky-barrier diodes are shown and analyzed in this section.

4.1.1.1. Current versus voltage of the Schottky-barrier diodes without Germanium

IV measurements on the fabricated Schottky-barrier diodes, before and after contact annealing, show the effectiveness of contact annealing in SiC. There was a measurable difference in turn-on voltage of the Ge containing diodes compared to the SiC-SBD's.

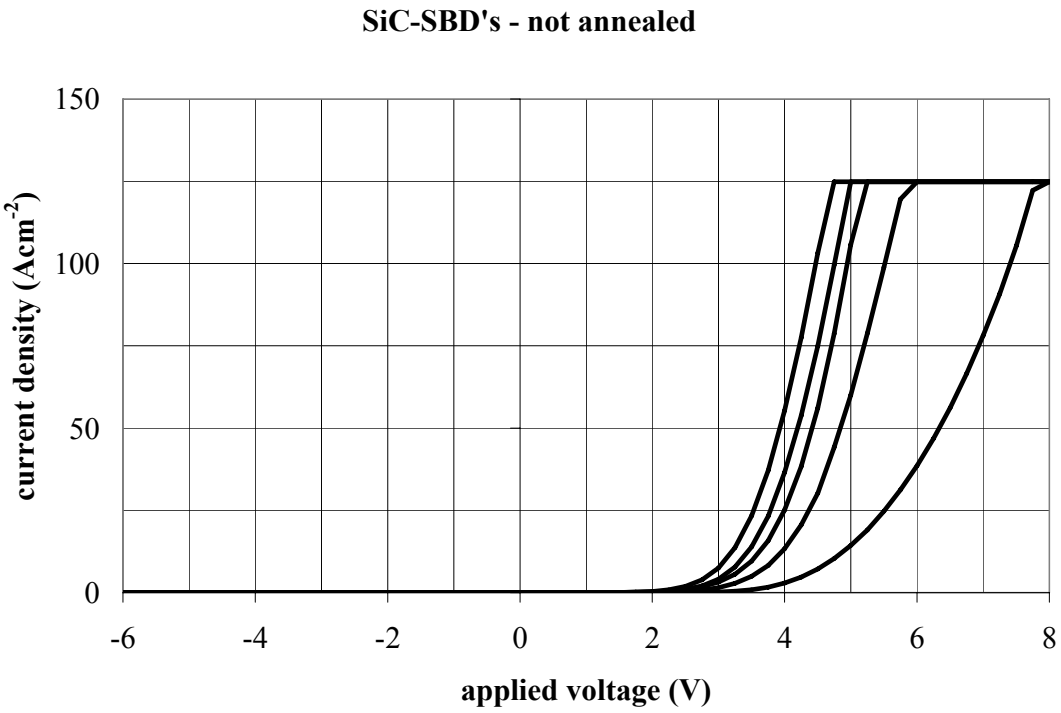

Figure 4.1 ***IV plots of SiC-SBD's – not annealed*: It is shown the IV curves of some sample metal-semiconductor barrier diodes, representing the variation observed among the processed diodes. The Ti/Al barrier metal was not annealed. The result is a high turn-on voltage, and a big variance in device behavior. Similarly processed SiC-SBD's with a Titanium/Gold (Ti/Au) contact did not show any considerable difference.**

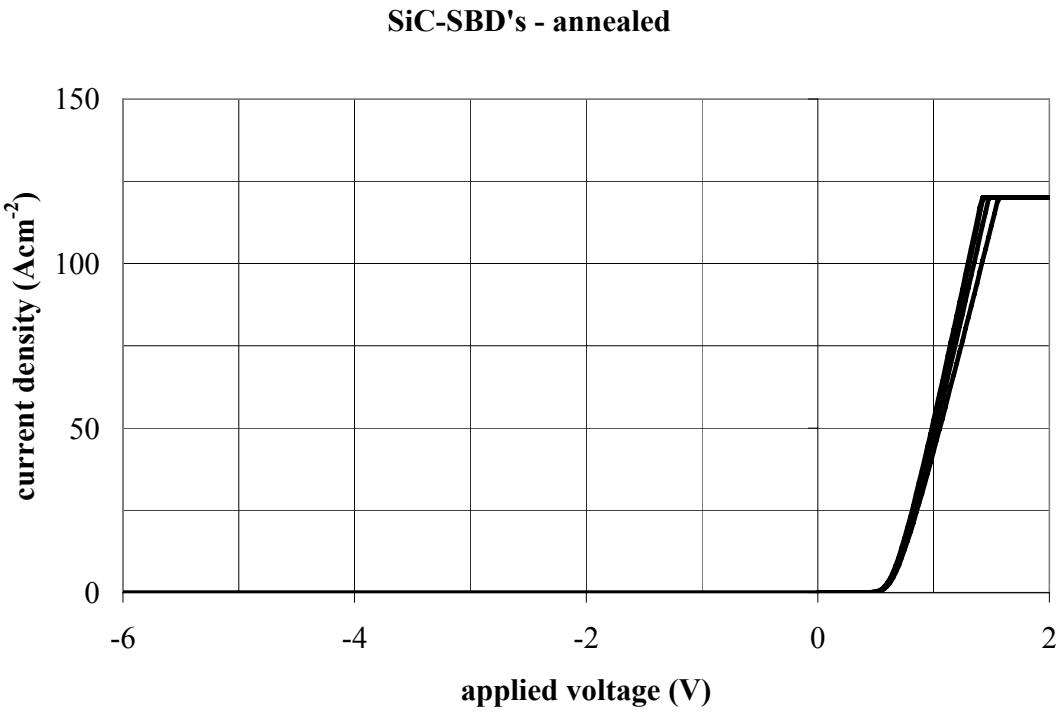

Figure 4.2 ***IV plots of SiC-SBD's – annealed*: In contrary to the first plot, after annealing the device behavior became more ideal, well predictable and much lower in turn-on voltage. Shown are different curves representing the diodes with the lowest turn-on voltage. Similarly processed SiC-SBD's with Ti/Au contacts exhibited no considerable difference.**

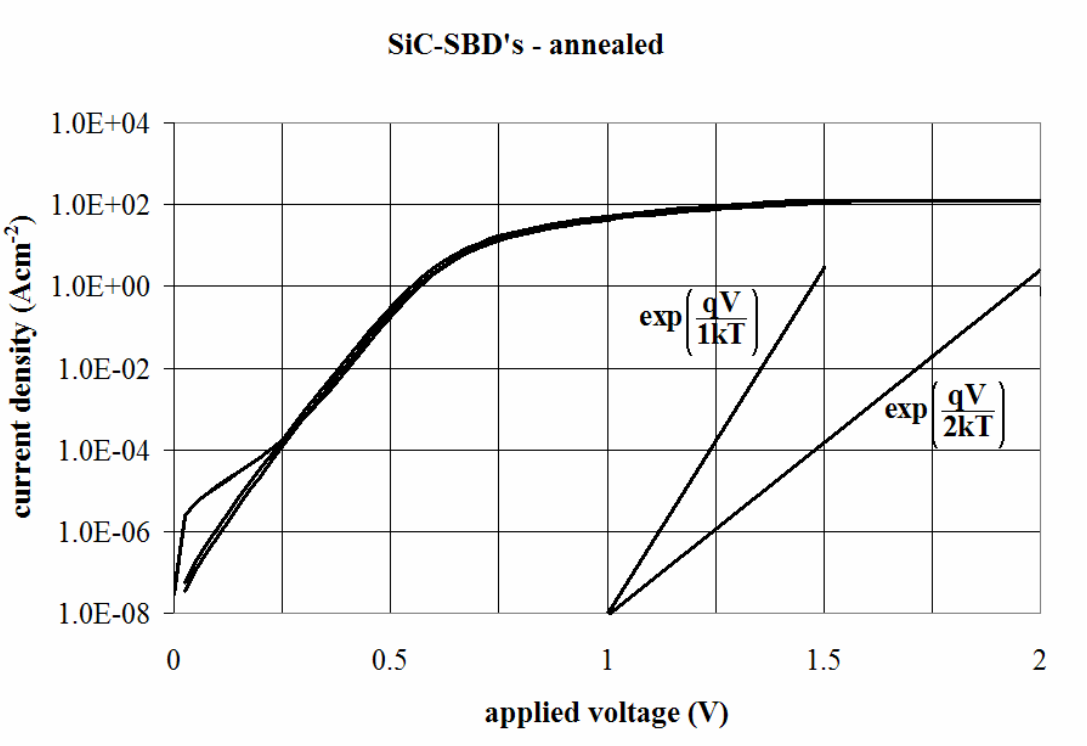

Figure 4.3 ***IV plots of SiC-SBD's – annealed (semi-log. plot)*: Beginning at very low currents, the device behavior is linear over many orders of magnitude of current density. Shown are different curves representing the diodes with the most linear behavior. On the right-hand side, the exponential terms of the diode equation, having an ideality factor of n=1 and n=2, are shown.**

Characteristic values of the annealed SiC-SBD's are listed below. The contact resistance was calculated from the slope of the IV-curve, where the exponential diode behavior becomes linear and the contact resistance is dominant.
Characteristic values of the annealed SiC-SBD's:

- Turn-on voltage: 0.8V @ 50Acm^{-2}
- Contact resistance: ~4.5mΩcm^2 (determined by IV measurements)
- Ideality factor: 1.1 – 1.64

With a turn-on voltage of about 0.8V and an ideality factor of 1.1, these devices are well functional and will the yardstick to determine the change of Ge-doped devices.

4.1.1.2. Current versus voltage of the Schottky-barrier diodes with Germanium

The diodes, annealed at 400ºC, exhibited not very useful data. They were in general highly resistive and their IV characteristics were inconsistent. Since I processed several batches of SiC:Ge-SBD's, I will provide the results of one that was annealed at 950ºC for 90sec. using shorter ramp times. The active contact area is 2.48*10^{-4}cm^2. Their device behavior is much more coherent and will be presented instead.

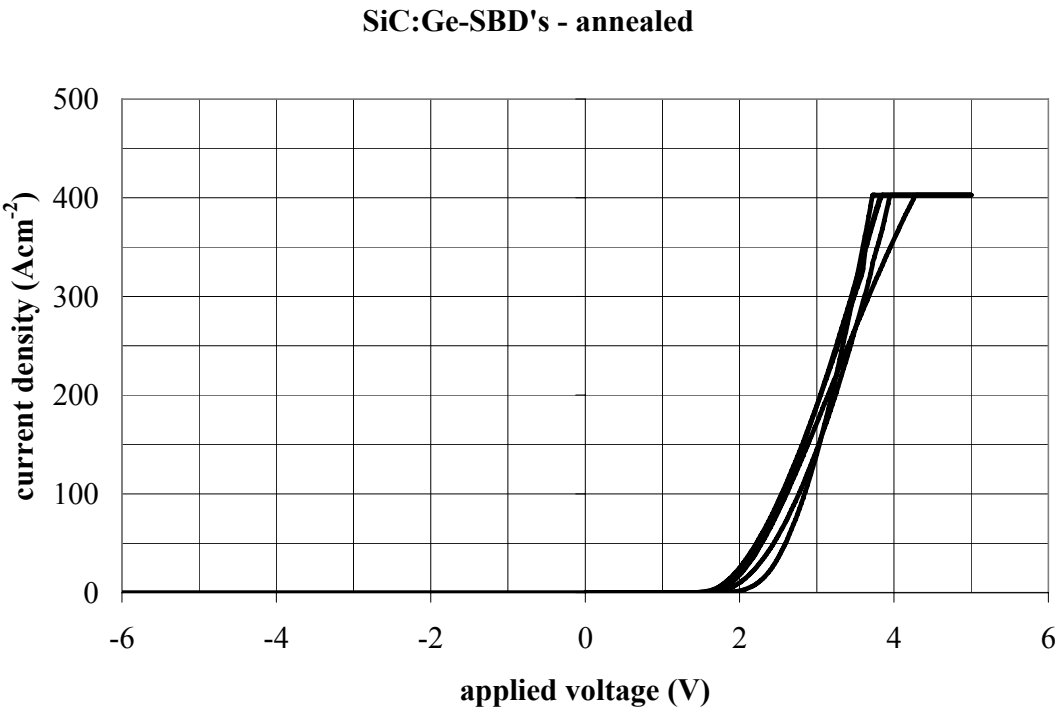

Figure 4.4 ***IV plots of SiC:Ge-SBD's - annealed*: Compared to Fig. 4.2 the turn-on voltage is approximately 1V higher at 50Acm^{-2}. Shown are different curves representing the diodes with the lowest turn-on voltage. The performance differs from device to device. Additionally, a higher contact resistance is generally seen than for the SiC-SBD's. Similarly processed SiC:Ge-SBD's with Ti/Au contacts exhibited comparable results.**

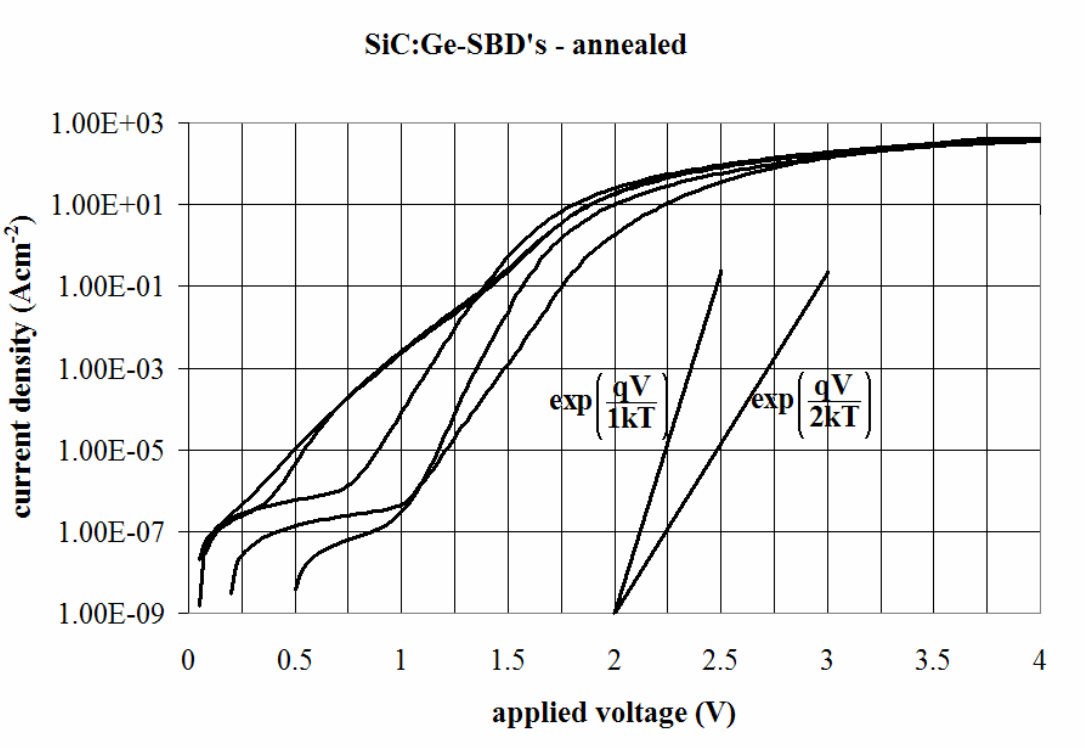

Figure 4.5 ***IV plots of SiC:Ge-SBD's – annealed (semi-log. plot)*: Despite the current step below 1V, the devices have a linear behavior over many orders of magnitude of current density. Shown are different curves representing the diodes with the most linear behavior. On the right-hand side, the exponential terms of the diode equation, having an ideality factor of n=1 and n=2, are shown.**

Characteristic values of the annealed SiC:Ge-SBD's:

- Turn-on voltage: 2.2-2.7V @ 50Acm^{-2}
- Contact resistance: ~20mΩcm^2 (determined by IV measurements)
- Ideality factor: 1.57 – 2.0

The Ge-containing Schottky-barrier diodes are similar to those without Ge if subtracting the current step occurring in most devices below 1V. Using this approach, the barrier of the 4H-SiC:Ge-SBD's is several 100meV higher compared to the SiC-SBD's. TEM images (section 4.3) revealed Ge precipitation during processing. This Ge-island formation may be related to the current steps, because it is not present in the diodes without Ge. The precipitated Ge may have formed an additional barrier.

4.1.1.3. Capacitance versus voltage of the Schottky-barrier diodes

CV measurements were performed with an overlaying AC signal of 1MHz and a peak-to-peak voltage V_{pp} of 25mV. Following, the CV-plots of a SiC:Ge-SBD and a SiC-SBD are shown. Each curve represents the approximate device behavior of all measured devices. Both diodes had a contact area of 6.41*10^{-4}cm^{-2} and CV was performed on the samples, whose process is described in chapter 3.

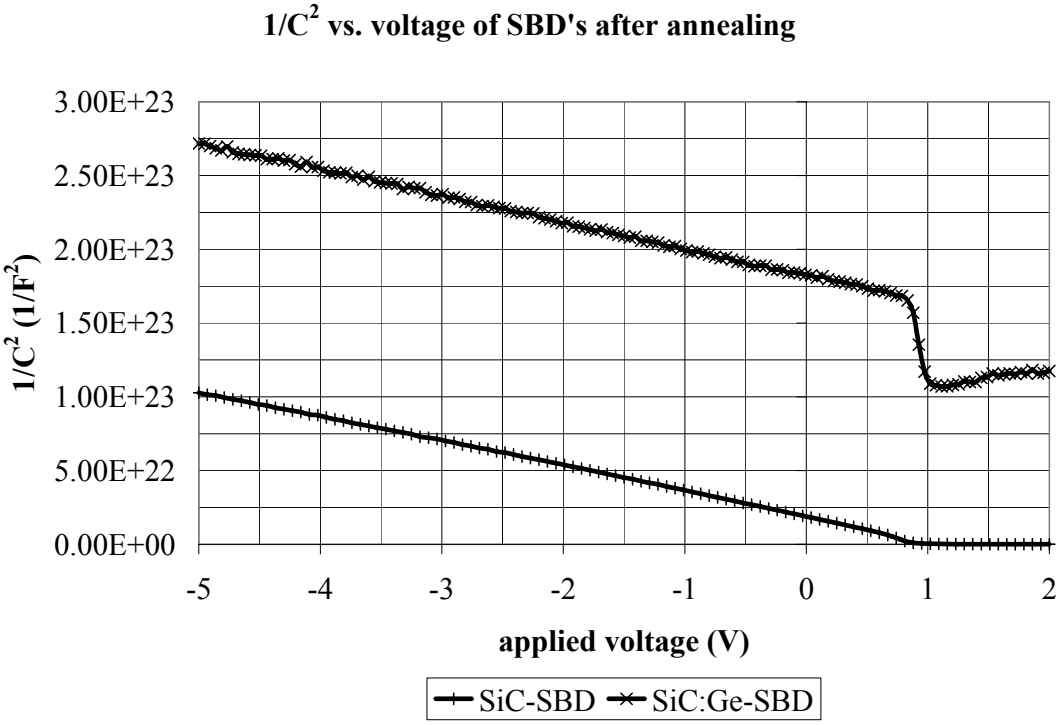

Figure 4.6 The lower curve shows $1/C^2$ vs. voltage of a SiC-SBD. Its nearly perfect linear behavior confirms its ideality. If extrapolating the line until intersecting the x-axis, one will find the built-in voltage to be about 1V and using equ. 4.1, N_d=~$2*10^{15}cm^{-3}$. The upper curve shows $1/C^2$ vs. voltage of a SiC:Ge-SBD. It has a rough curve and a downward kink at nearly 1V. For this curve I could not extrapolate the built-in voltage because of the downward kink, but N_d=~$2*10^{15}cm^{-3}$ in the linear region.

Using CV analysis, the carrier concentration versus depletion width for the SBD's is given equ. 4.1, where ε_s is the dielectric constant of 4H-SiC and A the active device area.

$$N(x_d) = \frac{-2}{q\varepsilon_s A^2 \left[d\left(1/C^2\right)/dV_A \right]} \qquad (4.1) \qquad [20]$$

CV measurements on SiC-SBD's showed consistent and nearly ideal device behavior. However, the CV measurements on the SiC:Ge-SBD's did not show a line as smooth as that of the SiC-SBD's. I speculate that the implantation has probably created more defects then expected, introducing an uneven carrier vs. distance profile. The downward kink at 1V may be explained by surface amorphization, because the depletion width extends to the surface for forward bias near 1V.

4.1.2. Measurements of the junction diodes

IV and CV measurements on both junction diodes are shown and analyzed in this section.

4.1.2.1. Current versus voltage of the junction diodes without Germanium

The anneal time of 120sec at 950ºC and the long cool-down time in a Nitrogen atmosphere might have affected the contacts more than intended. Therefore I will state the results from a different batch processed similarly. The p-type mesa area of these devices is $4.52*10^{-4}cm^2$. The anneal time was only 90sec, followed by a more rapid cool-down cycle. The plotted graphs represent the measured diodes with the lowest turn-on voltage. However, devices with a very high contact resistance were found too.

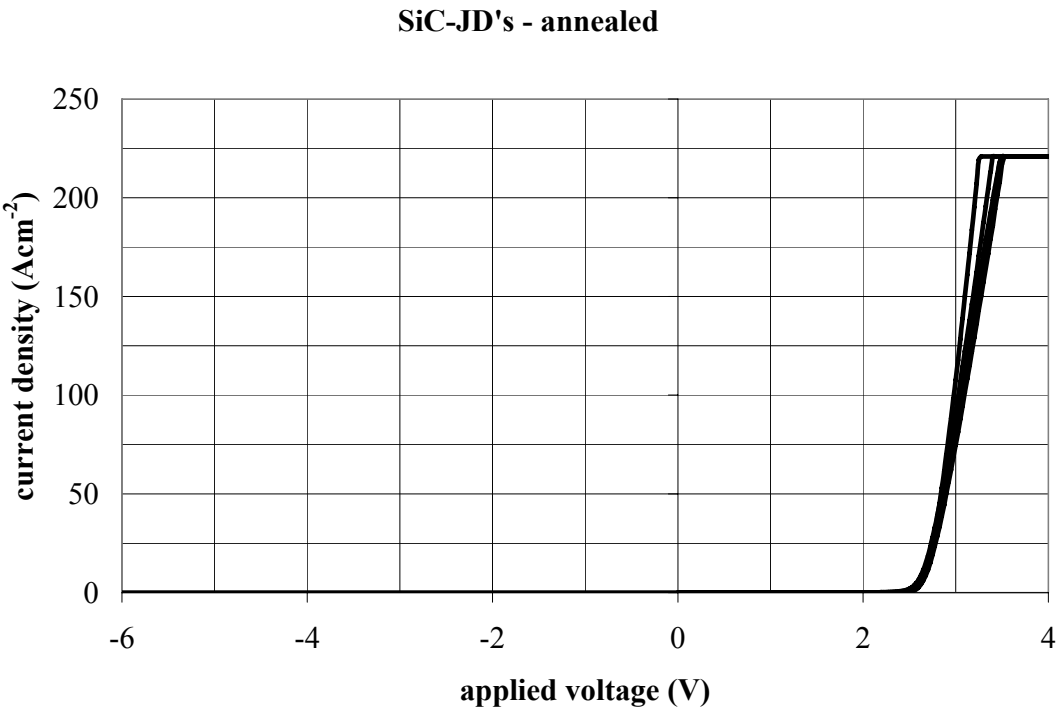

Figure 4.7 ***IV plots of SiC-JD's - annealed*: After contact annealing, the diodes exhibited comparability in device behavior.**

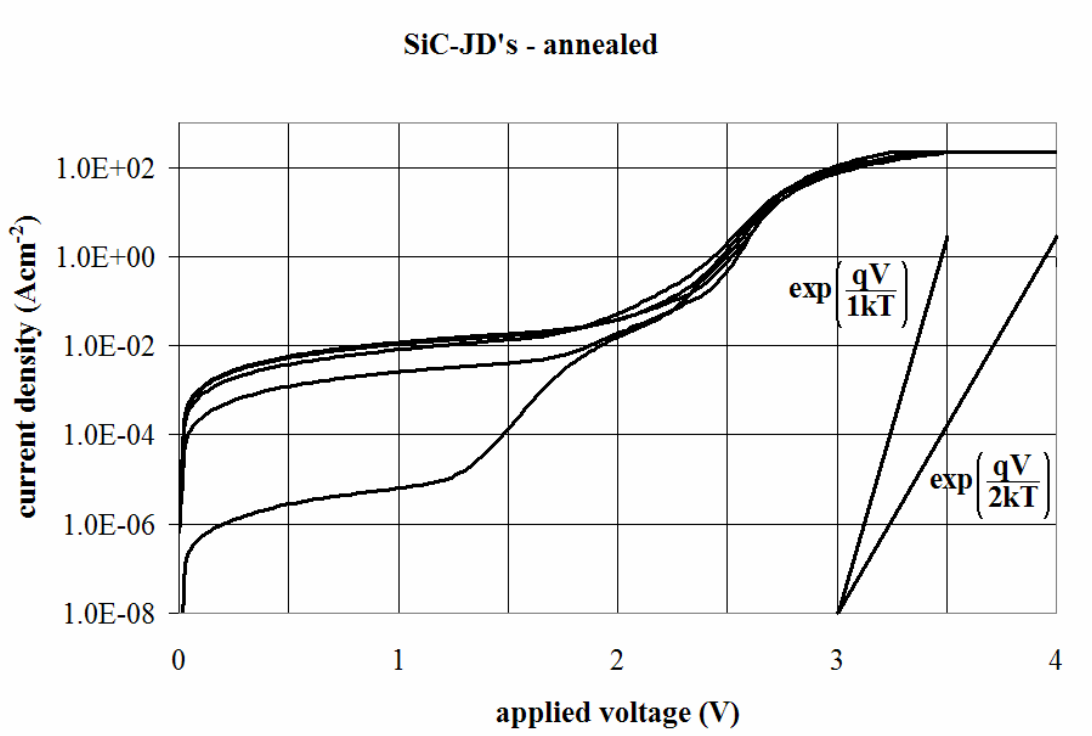

Figure 4.8 ***IV plots of SiC-JD's – annealed (semi-log. plot)*: Current steps and non-linearities are seen. The two steps, at 1V and 3V seem to indicate a parasitic junction or Schottky-barrier in series to the actual diode. On the right-hand side, the exponential terms of the diode equation, having an ideality factor of n=1 and n=2, are shown.**

Characteristic values of the annealed SiC-JD's are listed below:

- Turn-on voltage: 2.8V @ 50Acm^{-2}
- Contact resistance: ~33mΩcm^2 (determined by IV measurements)
- Ideality factor: 2.5 – 3.5

Despite their low turn-on voltage and low contact resistance, the devices showed a non-linear behavior in the semi-log. plot. It may be due to a parasitic junction or Schottky-barrier in series to the actual diode. Because of the differences in the shapes of the IV curves it will be challenging to compare them directly with the Ge-containing devices.

4.1.2.2. Current versus voltage of the junction diodes with Germanium

For the same reason mentioned at the beginning of section 4.1.2.1, I will show the graphs of slightly different processed diodes, which exhibited better device consistency. The p-type mesa area of these devices is 4.52*10^{-4}cm^2. The anneal time was only 90sec, followed by a more rapid cool-down cycle. The plotted graphs represent the measured diodes with the lowest turn-on voltage. However, devices with a very high contact resistance were found too.

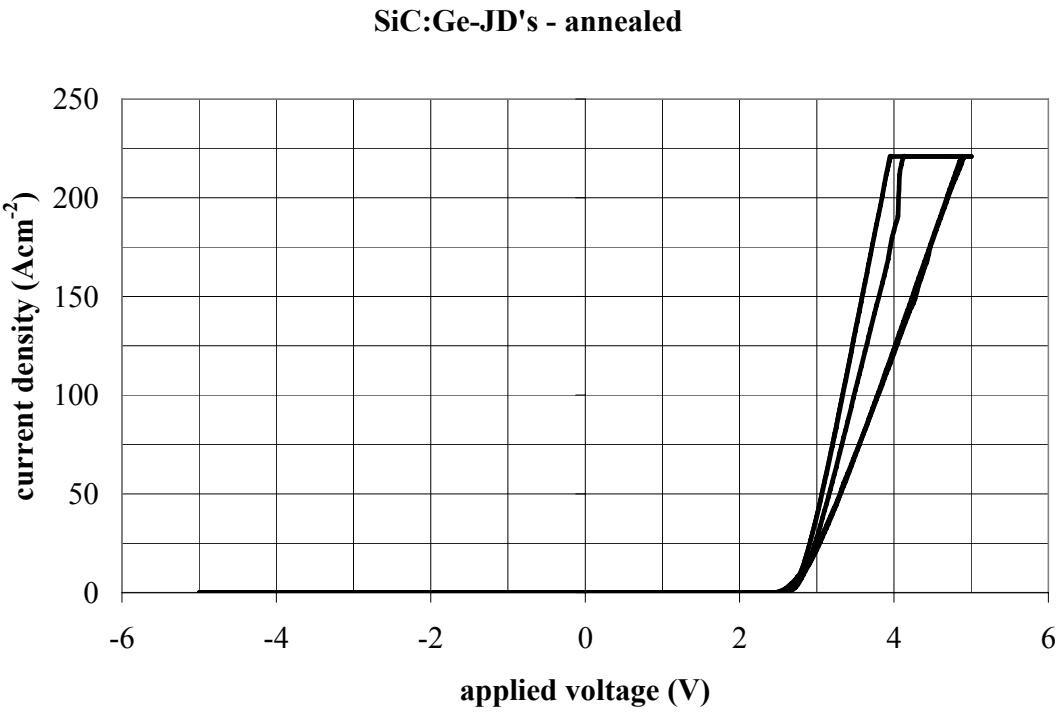

Figure 4.9 ***IV plots of SiC:Ge-JD's - annealed*: The turn-on voltage is several 100mV higher than that of the homojunction diodes. Yet, they show a nicely rectifying behavior.**

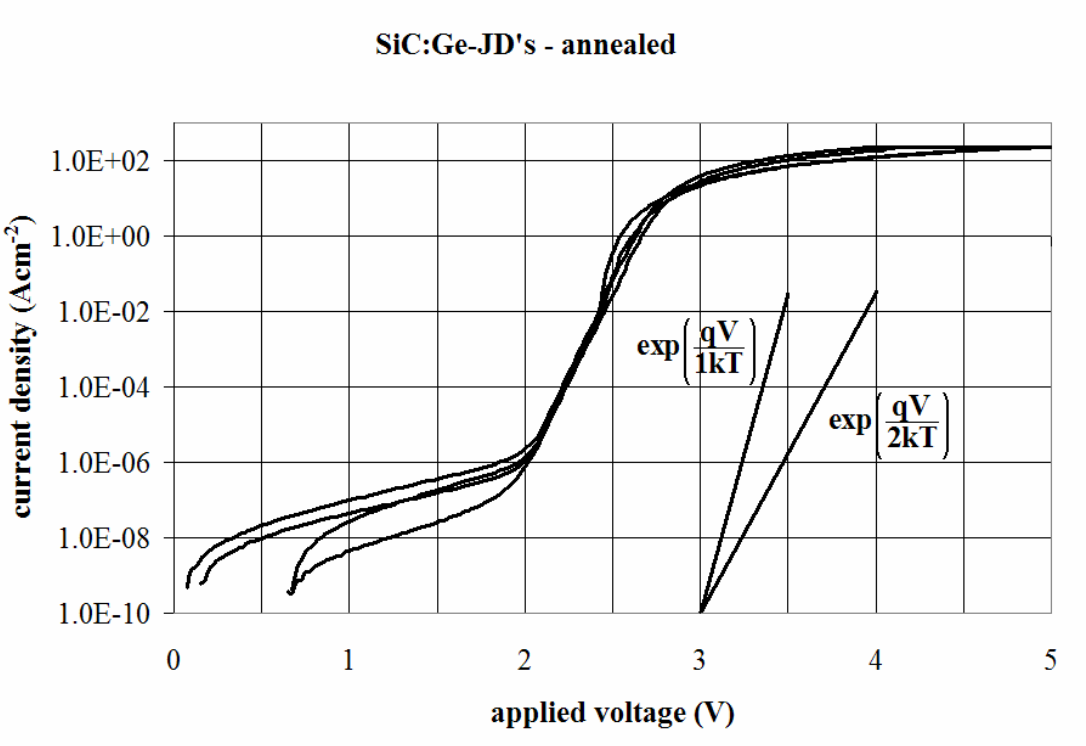

Figure 4.10 ***IV plots of SiC:Ge-JD's – annealed (semi-log. plot)*****: As in Fig. 4.8, current steps are seen. The two steps, at 1V and 3V seem to indicate a parasitic junction or Schottky-barrier in series to the actual diode. On the right-hand side, the exponential terms of the diode equation, having an ideality factor of n=1 and n=2, are shown.**

Characteristic values of the annealed devices are listed below:

- Turn-on voltage: 3.2V @ 50 Acm^{-2}
- Contact resistance: 160mΩcm^2 (determined by IV measurements)
- Ideality factor: 1.7 – 2

The effect of Ge in the processed junction diodes is not clearly seen. Both the homojunction diodes and the heterojunction diodes as well, have to overcome an additional barrier which appears as an extra step in the IV curves. The reason is not yet clear to me. Ge precipitation, surface amorphization, and a parasitic SBD may play a role in these device behaviors. But encouragingly, the SiC-JD's and SiC:Ge-JD's as well, have a turn-on voltage of about 3V, which was also expected by the calculated built-in voltage.

4.1.2.3. Capacitance versus voltage of the junction diodes

Following, the CV plots of a SiC:Ge-SBD and a SiC-SBD are shown. Each curve represents the approximate device behavior of all measured devices. The CV plots were obtained from the samples, whose process is explained in chapter 3.

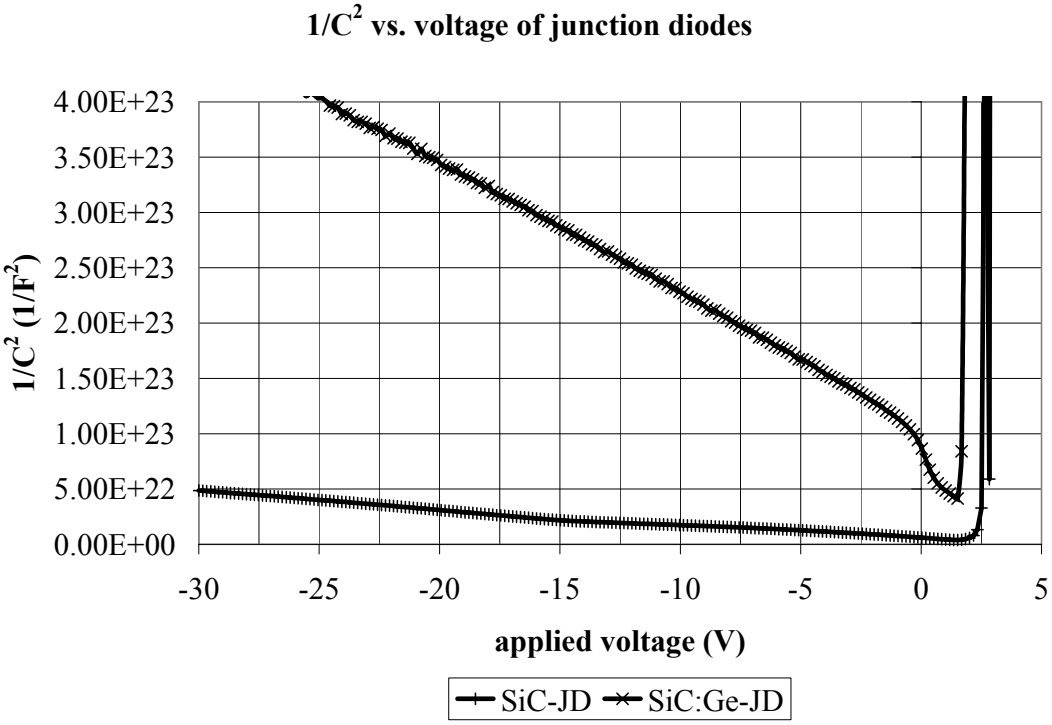

Figure 4.11 **The lower curve shows $1/C^2$ vs. voltage of a common SiC-JD. Its nearly perfect linear behavior confirms its ideality. If extrapolating the straight line until intersecting the x-axis, one will find the built-in voltage to be about 3.5V. The p-type doping concentration was calculated to range from ~10^{16} to $10^{17}cm^{-3}$ among the measured devices. The upper curve shows $1/C^2$ vs. voltage of a common SiC:Ge-JD. It has a rough curvature and a downward kink at about 0V. For this curve I could not extrapolate the built-in voltage because of the downward kink. The p-type doping concentration was calculated to range from ~10^{15} to $10^{16}cm^{-3}$ among the measured devices. The peak at 2V can be ignored for both curves. It is probably due to injected carriers while forward biased.**

Similarly to the case of the Schottky-barrier diodes, the Ge containing junction diodes may suffer from damage due to Ge precipitation. However, the homojunction diodes show a pretty straight slope and an x-axis intersection at about 2.5V. The Ge containing devices seem to have two slopes. The slope close to 0V might be due to a parasitic Schottky-barrier in series to the junction diode. It could also indicate surface amorphization.

$$N_a = \left[\frac{A^2 q \varepsilon_s}{2C^2 \left(\phi_i - V_A \right)} - \frac{1}{N_d} \right]^{-1} \quad (4.2)$$

[20]

$$C = \frac{\varepsilon_s}{x_d} \quad (4.3)$$

In equation 4.2, the p-type doping concentration N_a of a step-junction depends on the capacitance C which is obtained through CV measurements. ε_s is the dielectric constant of 4H-SiC and N_d is the n-type doping concentration of the epitaxial substrate layer. Using equations 4.2 and 4.3, one can quantitatively examine the doping concentration vs. distance for a step-junction diode. If the $1/C^2$ vs. voltage curve is steeper, the carrier concentration of the p-type region is lower, for a given n-type doping concentration. In Fig. 4.11 one can clearly see the difference in the curve slopes. The steepness of the SiC:Ge-JD curve indicates a p-type dopant activation of only 1% to 10% of the value of the SiC-JD. Hence, the high Ge content must have affected the dopant activation.

4.2. Transistor measurements and results

Unfortunately, IV measurements did not exhibit any transistor action on the fabricated devices. The possible reasons are manifold and will be explained in more detail at the end of this chapter. Additionally, the top contacts on the SiC:Ge-HBT's did not adhere very well and only a few devices with contacts could be measured. But they did not show any transistor action either. Therefore, the following graphs show the BJT behaviors only.

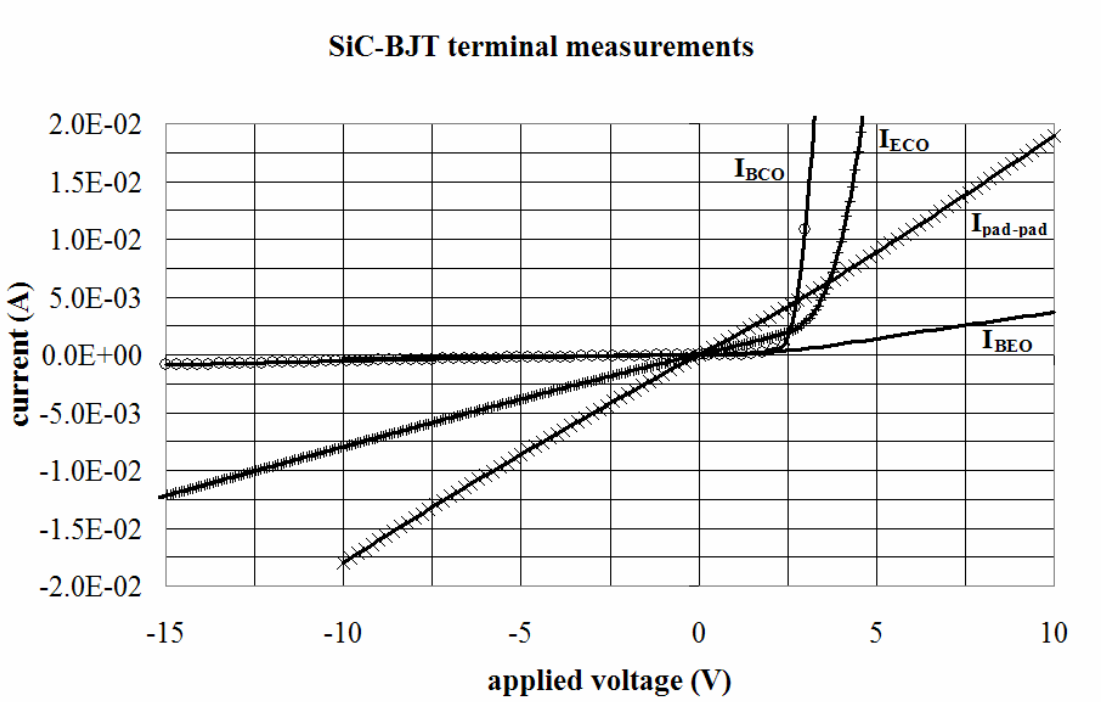

Figure 4.12 **Shown are terminal IV curves of a SiC-BJT, representing the approximate device behavior of many measured devices. I_{BCO}: BC diode (base current was measured, emitter open, collector grounded). I_{ECO}: EC terminals (emitter current was measured, base open, collector grounded). I_{BEO}: BE diode (base current was measured, collector open, emitter grounded). $I_{pad\text{-}pad}$: IV curve measured from one emitter pad to a consecutive one, on devices, on which the emitters are not isolated.**

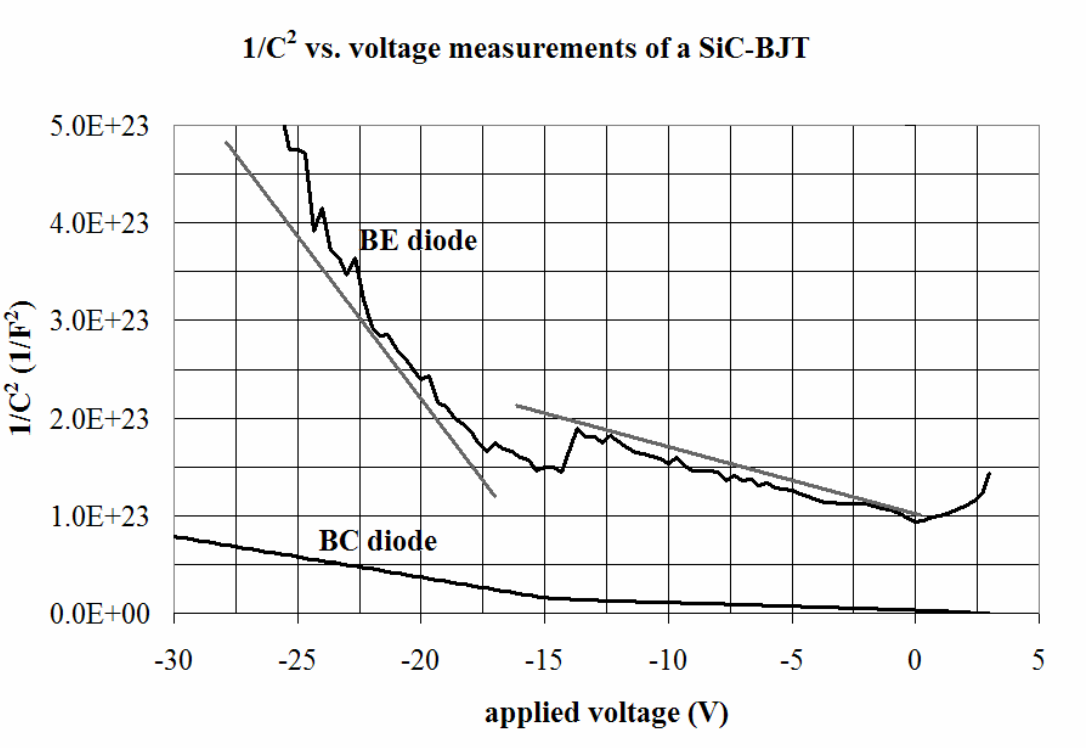

Figure 4.13 **Shown are the $1/C^2$ vs. voltage measurement of a base-collector diode (BC diode) and base-emitter diode (BE diode) of a SiC-BJT. Their results represent an average device behavior of many measured devices. The BC diode is linear over a large region of applied voltage, and a p-type base doping concentration of ~$1*10^{16}cm^{-3}$ can be extracted. Its extrapolated slope intersects the x-axis at 3V. The BE diode, however, did not exhibit a straight line. The lines close the BE diode are its extrapolated slopes. The doping concentration must be much smaller. I can not extrapolate an x-axis intersection.**

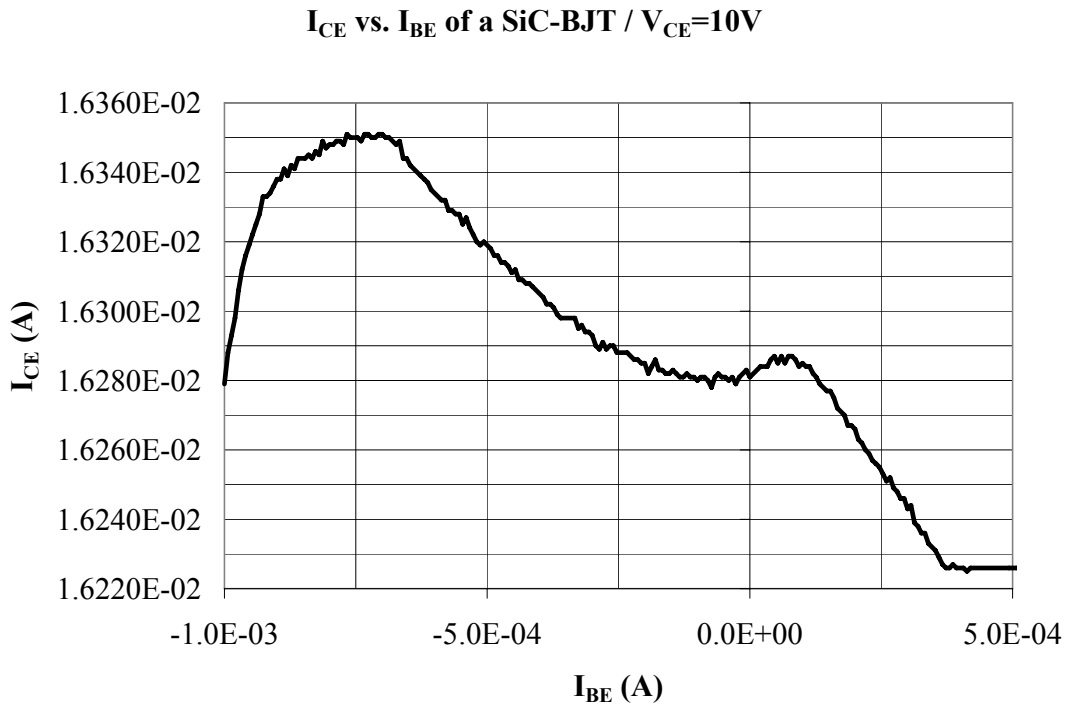

Figure 4.14 **Shown is the collector current versus base current for a common emitter circuitry of a SiC-BJT. Its result represents a few of the measured transistors. The I_{CE} leakage current is about 16mA at V_{CE}=10V. The curve is quite unusual. Especially for negative base current, I_{CE} seems to takes a parasitic path. But one thing is remarkable. At rising positive base current, the collector seems to follow until some other path takes over.**

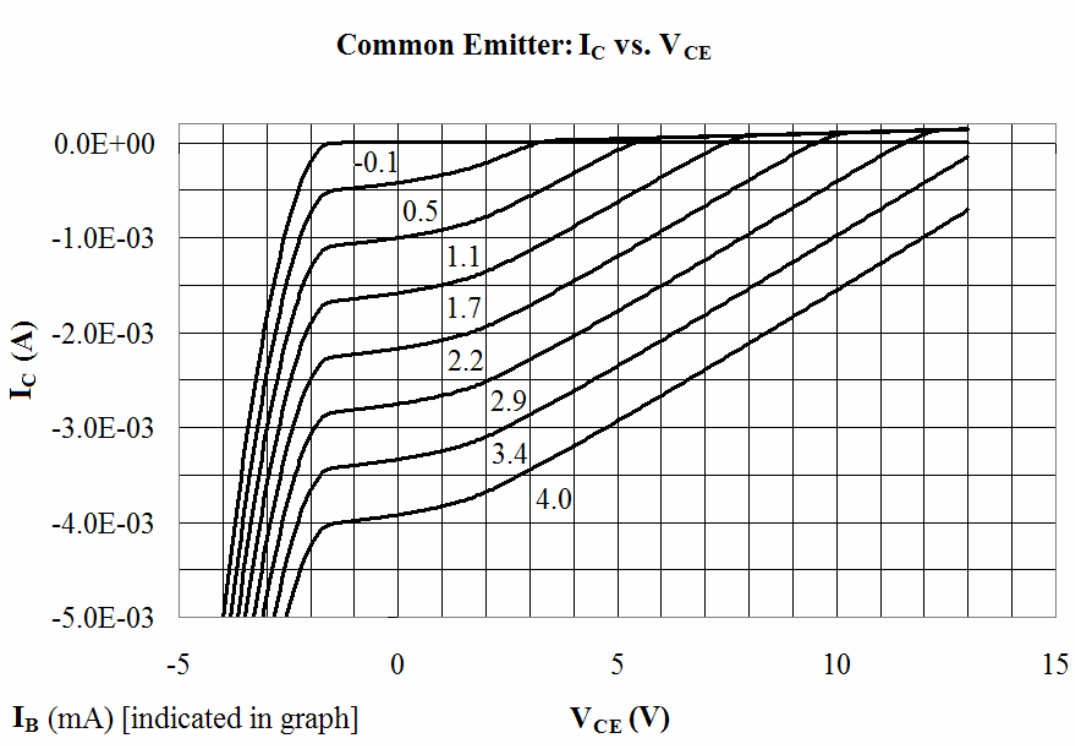

Figure 4.15 **In this common emitter circuitry, I_C vs. V_{CE} was measured while the base current I_B was stepped from -0.1mA to 4mA. At about -3V all currents break down according the diode-like behavior of the CE region (see Fig. 4.12). For most of the applied V_{CE}, I_C remains negative. Only a very small positive current is seen at high V_{CE}. Interestingly, this small positive I_C rises with rising I_B. The emitter was grounded during this measurement.**

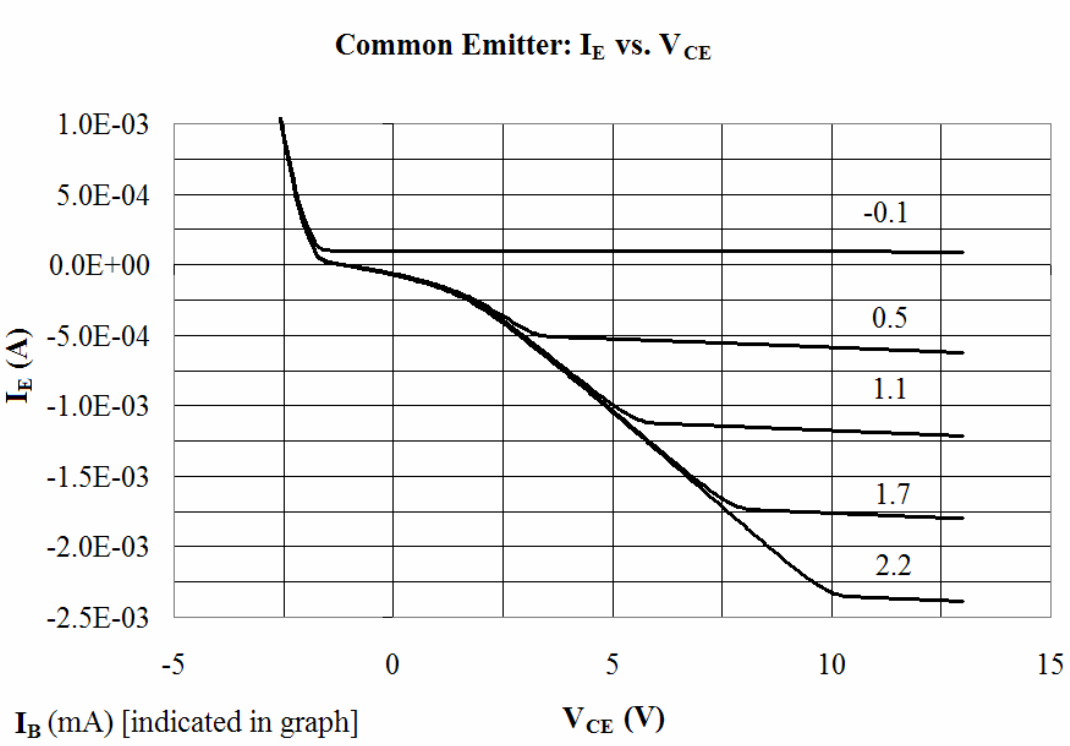

Figure 4.16 **The dependence of emitter current to collector-to-emitter voltage. Negative I_E means that current comes out of the terminal. At a negative voltage, the emitter current breaks down. The forward biased transistor in common emitter mode shows a linear emitter current which becomes saturated at higher voltages. But comparing all currents of this three-terminal device, one can see that the emitter current consists almost all of base current and the collector is nearly not affected. The saturation of the emitter current is still unclear to me.**

As shown in Fig. 4.12, only the BC diode worked properly. Despite a low resistance from emitter to collector (EC region) when forward biased, the n-type region (physical emitter layer) had a high resistance laterally from one emitter pad to a consecutive one. This phenomenon is not yet totally clear to me. The weak rectifying behavior of the BE diode was another unresolved characteristic of most transistors. Since the physical base width was designed relatively narrow, Al dopant diffusion during annealing might explain the BE diode behavior, since a very low doping concentration in the base was found with the CV measurements. It simply might have diffused vertically during post-annealing, leaving a low p-type doping concentration at the BE junction behind. A low doping activation and/ or diffusion in the base (less than 1600Å width) might have resulted in punch-through of the fully depleted physical base. This is also supported by the weak rectifying behavior of the BE diode.

Resulting from these graphs, no obvious transistor action can be extracted. Although some of the effects seen in Fig. 4.14 and 4.16 might be due to carrier injection into the base.

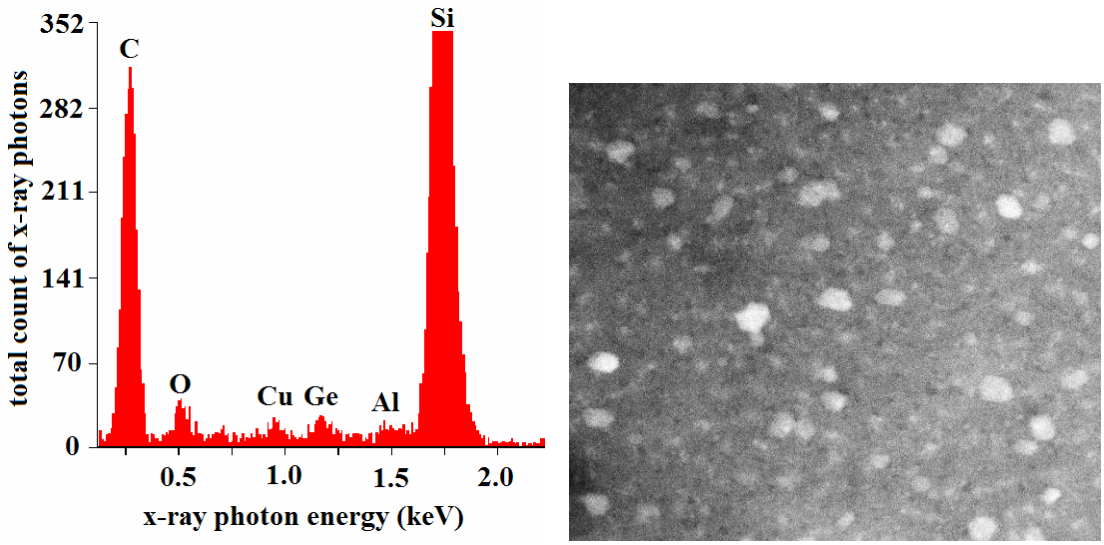

Figure 4.17 **(left) Averaged element concentration spectrum of the ~80X100nm white field TEM image (right). The white dots are precipitated Ge-rich islands.**

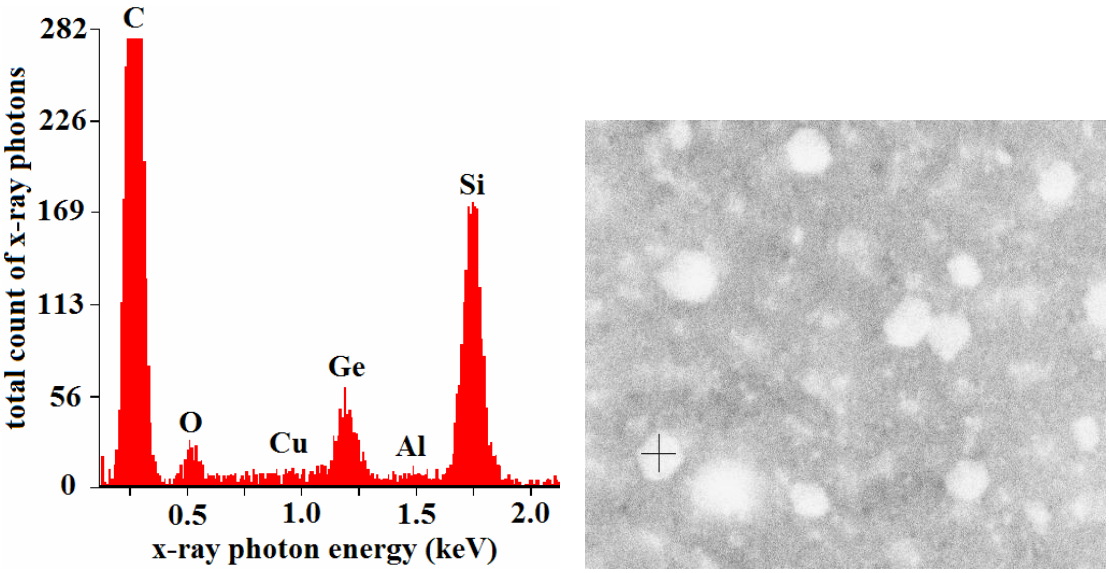

Figure 4.18 **(left) Element concentration spectrum of the cross-marked dot (right) of the white field TEM image.**

4.3. Transmission electron microscopy images

Prof. Ni (ME department, UofD) detected Ge precipitation when performing Transmission Electron Microscopy (TEM) on one of my Ge containing SiC wafer samples. Since the wafer annealing temperature was at 1675ºC, Ge-rich island formation was probably caused during this process step [38]. Comparing Fig. 4.17 with Fig. 4.18, one can clearly see an increased Ge concentration in the white regions of the TEM images. Oxygen and copper can be ignored on these figures. Knowing now the atomic structure of my samples, it strongly indicates to be related to the current steps in Figs.4.5 and 4.10.

4.4. X-ray diffraction spectroscopy on 4H-Silicon-Carbide doped with Germanium

N. Sustersic and Dr. N. Faleev performed X-Ray Diffraction spectroscopy (XRD) on two different samples, produced from part C and D of BX0178-04. Part C was the preprocessed 4H-SiC substrate, whereas part D contained additionally Germanium. XRD was performed on the top surface of the substrate, which is 8.0° off-axis toward <1120> ± 0.5°, on a Philips X`Pert high resolution x-ray diffractometer [39].

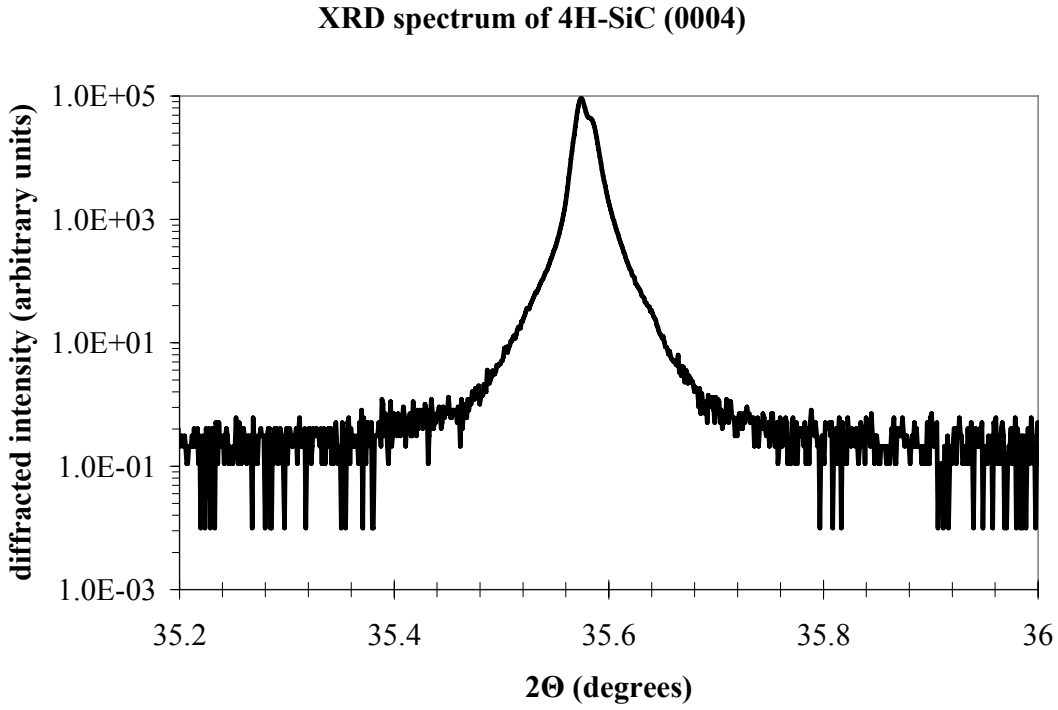

Figure 4.19 **Shown is the high resolution XRD spectrum of sample C. The (0004) peak of the 4H-SiC occurred at 35.575º. The broader shoulder on each side may be due to imperfections in the epitaxial layer.**

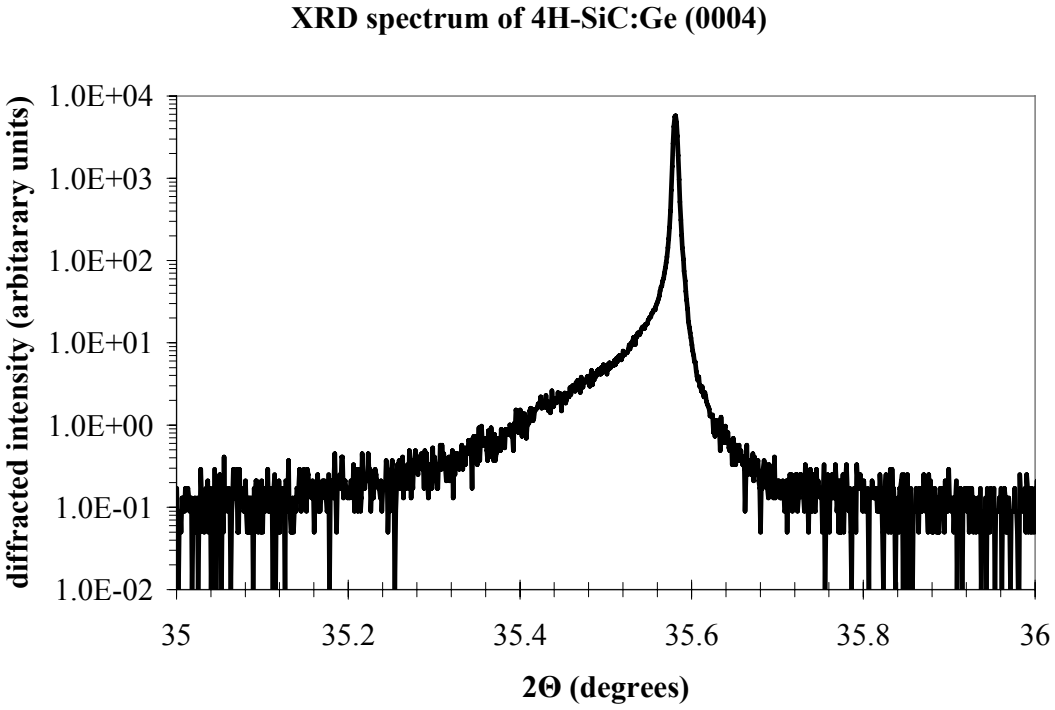

Figure 4.20 Shown is the high resolution XRD spectrum of sample D. The (0004) peak of the 4H-SiC occurred at 35.581º. The broader shoulder on the left side of the peak corresponds to the incorporated Ge.

The (0004) peak of 4H-SiC is clearly seen in both pictures at an angle of about 35.58º. The XRD spectrum of the Ge-containing sample has a broad shoulder on the left side of the SiC peak. Dashiell et al. reported similar results [30]. It is not yet clear, why the Ge does not affect the spectrum more extensively. I would have expected evenly spaced fringes, indicating a strained SiC:Ge substrate. But knowing the results of the measurements and the TEM images, the weak shoulder in Fig. 4.20 might be explained with surface amorphization and Ge precipitation.

4.5. Conclusion of the measurements

In this chapter, all measurements of the 4H-SiC and 4H-SiC:Ge devices were presented and will be concluded in this section. After annealing, the Schottky-barrier diodes without Ge exhibited good results. But it is difficult to compare them with the Ge-containing SBD's because of the current step, resulting possibly from Ge precipitation and surface amorphization. In the case of junction diodes, non-linearities are seen in the semi- log. plots. Even though I did not expect them for the SiC-JD's, it may help to understand the homojunction transistor characteristics better. Could have the implanted Al caused some problems too? The measured transistors did not exhibit any obvious transistor action. Base punch-through or doping problems perhaps made transistor action impossible.

Even though the expected effects of Ge in SiC which were explained in chapter 2, could not be verified by this research, very useful data and information was obtained. The measured devices, XRD and TEM revealed surprising data which will be used for further research on the effects of Ge in SiC.

Chapter 5

DISCUSSION AND CONCLUSION

In my thesis, 4H-Silicon-Carbide Schottky-barrier diodes, 4H-Silicon-Carbide heterojunction diodes and 4H-Silicon-Carbide heterojunction transistors were designed, fabricated, analyzed and compared to their isomaterial counterparts. A final discussion and future prospects will now follow.

On the fabricated SiC-SBD's I could see the necessity of contact annealing. IV measurements showed Ti/Al and Ti/Au Schottky barrier metals to be equally effective after contact annealing. The Ge containing devices suffered possibly from the effects of Ge precipitation and surface amorphization. A low carrier activation percentage [40] and parasitic effects are the predominant results. Despite Ge precipitation and its associated effects, the SiC:Ge-SBD's and SiC:Ge-JD's showed rectifying behavior. However, the HBT's did not exhibit any obvious transistor action. Even though there are several well rectifying SiC-JD's, most of the measured devices did a show a large parasitic series resistance. The same is seen in the BE diodes of the SiC-BJT's. Al dopant diffusion and low activation percentage are considered the explanation for punch-through of the base, since it is also supported by the non-blocking EC terminal of the transistors.

The introduction of Ge in a Silicon-Carbide host lattice through ion-implantation resulted in more complications than expected. Ge seems to have a strong tendency to form clusters (precipitate) during high temperature post-annealing [38] as shown in chapter 4. There seems to be a way to overcome the problems stated above. Dashiell et al. [30] results indicate a strained 4H-SiC:Ge layer when post-annealing is not performed. I believe it would be better not to post-anneal the devices at all. It is still unknown whether the Ge would become interstitional or substitutional. Either case, the strained host-lattice is believed to lower the bandgap as well. And exactly here will be the starting point for future research. A new design is being developed. The major improvements will be an extended base width to 3000Å, 0.5% Ge incorporation and no post-annealing process after Ge implantation. I am very confident, that these changes will yield proper device functionality.

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