CHARACTERIZATION OF FUNDAMENTAL PARAMETERS OF FRONT JUNCTION AMORPHOUS/CRYSTALLINE SILICON HETEROJUNCTION SOLAR CELLS USING VARIOUS ELECTRICAL METHODS

by

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A thesis submitted to the Faculty of the University of Delaware in partial fulfillment of the requirements for the degree of Master of Science in Electrical and Computer Engineering

Summer 2010

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ACKNOWLEDGMENTS

Thank you everyone for all the support while I was working on my thesis. I'd like to thank Dr.Birkmire and Steve for giving me the oppurtunity to work at IEC. I enjoyed my time here, and it has been a learning experience. My advisor, Steve, was very supportive and patient with me. It is not easy, and I thank him for everything he taught me. I also thank Ujjwal for making the samples I measured for my research and thesis work. John, Brad, Chris, and Dan Ryan were always there to lend a hand when I was stuck. Thank you guys! Nupur, you've helped me so much from the time we met. Thanks for putting up with my crazyness. I learned that sometimes it's fun to go out and play just because I can. I blame Elizabeth and Lulu for that. I had so much fun cooking, playing, traveling, and all good times we had. Thank you, Teresa, for solving all my crazy problems whenever I came running to you. I enjoyed chatting with Brian, Andrew, James, and Jianbo when I was bored. Our conversations were interesting in a funny way and sometimes inspiring. Thank you for making me smile! Kathy from Electrical Engineering department got me out of trouble many times. She's a life-saver! Thank you! Last but not least, I thank my parents and my sister for always cheering me on to do my best.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

ABSTRACT

Silicon heterojunction solar cells promise low cost processing and high efficiency cells because they can be processed at low temperatures and have very well passivated surfaces. With a thin intrinsic layer between amorphous doped layers and crystalline silicon, these cells have demonstrated open-circuit voltages greater than 720mV and efficiencies over 22%. In the thesis, electrical measurements are used to characterize the behavior of the front heterojunction silicon solar cells. Doping density, excess defect density, and free-carrier density can be obtained from measurements from the capacitance system using different methods. Impedance spectroscopy utilizes a simple RC parallel circuit model to get parallel capacitance, parallel resistance, and series resistance from a complex impedance plot. Minority carrier lifetime on a completed solar cell is calculated from the Nyquist plot. JV-T measurements are used to get the barrier height that carriers have to overcome to be collected along with some diode parameters. Internal photoemission method is used to get estimated values of valence and conduction band-offset for samples with different structures. The goal of this thesis is to use different methods to determine parameters that relate to open-circuit voltage and fill factor. Our focus is on the effect of the a-Si layer: either none, or 5nm i-layer in front, back, or both sides. This i-layer strongly affects the V_{oc} and FF. The open-circuit voltage correlates with the lifetime determined from impedance spectroscopy.

Chapter 1

INTRODUCTION

About 85% of today's solar modules are fabricated using solar cells made from Si wafers. Typically, these modules are fabricated with a diffused front homojunction and screen printed contact grids and have efficiencies of 13-16%. High-efficiency solar cells can produce more electricity per unit area so fewer of them are required to produce the required electricity leading to cost reduction. Unlike the diffused homojunction crystalline silicon solar cells, Silicon HeteroJunction(SHJ) solar cells with a thin intrinsic layer at the heterojunction interface(called HIT cells by Sanyo Solar) have demonstrated efficiencies of over 23% [1] primarily due to record high open-circuit voltages over 720mV. Modules from these HIT cells are commercially produced with nameplate efficiencies of 17.4%.

SHJ solar cells have their advantages. They do not require high-temperature diffusion or screen printing ($>800^{o}C$) like other standard solar cell structures. Instead, Plasma-Enhanced Chemical Vapor Deposition system is used to make the cell. PE-CVD allows low-temperature deposition ($<200^{o}C$) of a-Si:H layers on the crystalline silicon wafer [2]. Low-temperature deposition improves the lifetime of the c-Si wafer as well [1]. Critical to achieving the excellent passivation of the Si surface are the following steps: Si surface cleaning, deposition of a very thin (2-10nm) a-Si intrinsic

layer on both Si surfaces, and finally doped a-Si emitter and base contact layers on the intrinsic layers. In particular, the intrinsic a-Si (called the i-layer) passivates the wafer making this heterojunction a better structure compared to the homojunction c-Si solar cells. With good passivation and wafer cleaning, it is possible to get high open-circuit voltage and efficiency [1]. Unlike the c-Si wafers used by the majority of the standard solar cell manufacturers, the c-Si wafers used by Sanyo are n-type. The silicon group at the Institute of Energy Conversion has been working to produce cells of 22% efficiency. All of the solar cells reported in this thesis are n-type Si. Currently, we are able to achieve 15% efficiency for front junction and Interdigitated Back Contact (IBC) silicon heterojunction solar cells. There are significant difficulties and challenges in reproducibly fabricating these SHJ devices. We and others often encounter low performance and non-ideal device behavior. Empirical evidence points to the heterojunction and a-Si layer as sources of these problems.

In this thesis, we characterize front-junction SHJ solar cells using various capacitance methods, internal photoemission, and current-voltage measurements. In particular, I will focus on the capacitance methods to analyze SHJ solar cells to obtain the lifetime, excess defect concentration, density of states with respect to energy, ideality factor, recombination current, series resistance and valence/conduction band offsets. These parameters help understand the performance of the solar cell and will reveal any recombination locations and possible problems during fabrication in the solar cell. Moreover, they will help understand how to improve parameters that are directly

related to the performance such as FF, open-circuit voltage, and short-circuit current of our SHJ structure.

1.1. Thesis outline

In chapter 2, we will discuss the structure and fabrication of SHJ solar cell. Then, we will see how a Front Junction Silicon HeteroJunction solar cell operates under illumination.

In chapter 3, equipment for the measurements and a brief introduction to each method is discussed.

In chapter 4, the capacitance system's repeatability is observed by performing a standard capacitance-voltage measurement on a silicon calibration cell every time the system is used. Also, simple parallel RC circuits of known resistance are measured to demonstrate the system's performance abilities.

In chapter 5, capacitance-voltage, excess defect density, c-v profiling, and drive-level capacitance profiling are discussed. In chapter 6, frequency dependent capacitance measurements, parallel circuit model, and Impedance Spectroscopy method to obtain circuit parameters are discussed.

In chapter 7, temperature dependent current-voltage measurements are discussed. The barrier height from these measurements is compared to the barrier height (also called activation energy) from $V_{oc} - T$ plots. A diode analysis method to obtain series resistance and conductance is discussed.

Chapter 8 includes analysis of quantum efficiency measurements. Internal photoemission technique is used to estimate the valence and conduction band offsets of the cells with (p)a-Si/ (n) c-Si junction.

Chapter 9 concludes the thesis with possible improvements to the methods, analysis and future work.

Chapter 2

FRONT HETEROJUNCTION SILICON SOLAR CELL

2.1 Structure of front SHJ solar cells

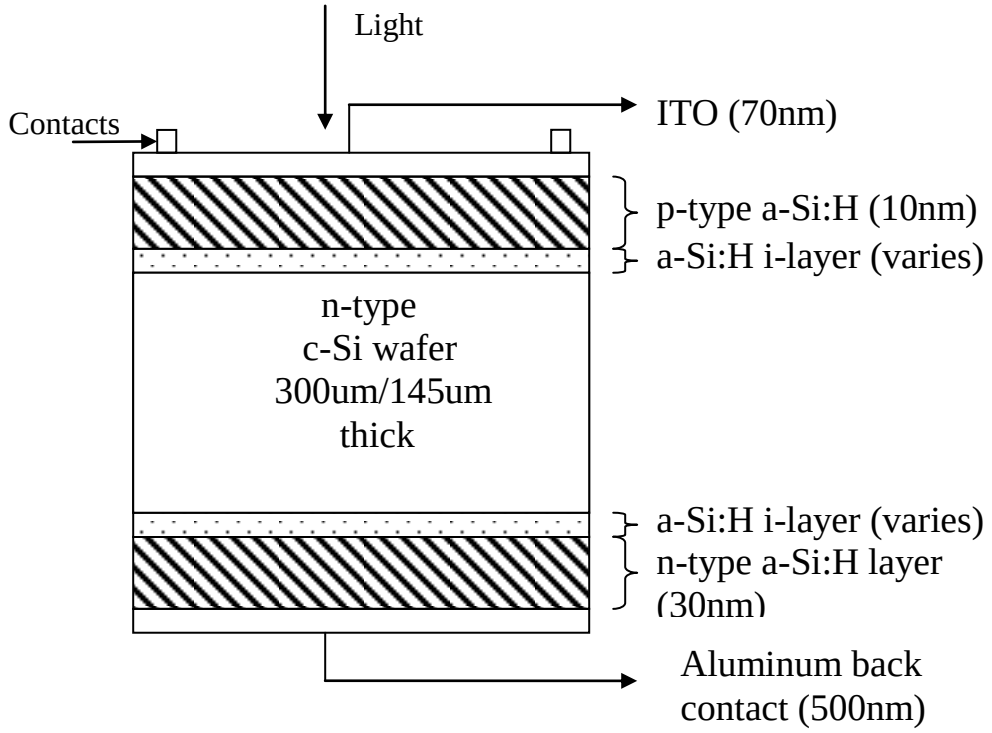

Fig.2.1: Cell structure of Silicon Front Heterojunction solar cell.

The cells analyzed for this thesis were fabricated at the Institute of Energy Conversion (IEC). The Silicon heterojunction solar cell structure is as follows, The c-Si wafers we use are n-type, have (100) orientation, and are either 145um or 300um thick. The wafers are cut into 1" x 1" pieces then chemically etched and cleaned. Following the final HF dip, they are immediately loaded into the multichamber PE-

CVD system. The cleaning and processing of the SHJ solar cells are discussed in the next section.

2.2 Processing

2.2.1 Wafer pre-clean

Polished crystalline silicon float zone wafers (or a textured or CZ polished wafer) of (100) orientation of four inch diameter are mechanically scribed into one inch squares. Then, wafers are pre-cleaned in several steps [3]:

1. Clean ultrasonically in acetone for five minutes.
2. Clean ultrasonically in methanol for five minutes.
3. Rinse with isopropyl alcohol.
4. Rinse with deionized water for five minutes.
5. Blow dry with compressed nitrogen.
6. Sulfuric acid:Hydrogen Peroxide (2:1) piranha etch for five minutes.
7. Rinse with deionized water for five minutes.
8. Blow dry with compressed nitrogen.
9. Hydrofluoric acid etch for one minute.
10. Blow dry with compressed nitrogen.

This standard cleaning procedure was developed over several years and was used for cleaning most of the c-Si analyzed in this paper.

2.2.2 Deposition

The a-Si:H layers are deposited on the wafer in the multichamber Plasma Enhanced Chemical Vapor Deposition(PE-CVD) system at IEC. Electrical energy is used to generate dc or rf plasma, and then the energy is transferred to gas mixture that is highly excited and deposited on the substrate. The a-Si layers can be deposited on multiple wafers on a single tray at the same deposition cycle. The chambers of the system are typically under constant vacuum of 1250mT during deposition while the plasma current is kept at 123mA. Different chambers are used to deposit p, n, and intrinsic amorphous layers to avoid contamination in the wafers. The temperature of the chamber is set at $200^{o}C$. If the structure requires an intrinsic layer, it is deposited first on the wafer. The only difference between p, i, and n layers is the gas flows. The samples are annealed for 25 minutes at $300^{o}C$. For the cells that had silicon nitride to protect and passivate the i-layers, the SiN is deposited from silane and ammonia at $300^{o}C$. The silicon nitride layer is then etched off before the deposition of the doped layers. The n-layer is deposited before p-layer to prevent diborane to diffuse into the i-layer. It is deposited from silane, phosphine, and hydrogen (ratio 1:1:6) gases. The p-layer is formed with silane, diborane, and hydrogen (ratio 1:1:6). If a flipper is not used to easily move samples from one chamber to another, they have to be removed from the vacuum. The flipper can be used to fix the samples on it thereby allowing it to flip from one side to another to deposit a-Si layers. Contamination due to exposure to air occurs when a flipper is not used because the samples are removed

from the chamber and manually flipped even though this takes only a few seconds. To get rid of unwanted oxide growth, defects or contamination, they can receive a second HF etch before another deposition. The second HF dip is a standard procedure to prevent silicon dioxide from forming on the sample which can lower the open-circuit voltage [2,4].

A 30nm a-Si:H n-type layer is deposited on one side, and 10nm a-Si:H p-type layer is deposited on the other side of the wafer. An intrinsic a-Si:H layer between the a-Si:H layers and the wafer is optional. A 70nm ITO layer is the transparent conducting oxide that is deposited by sputtering. The aluminum and nickel grids are deposited on top of ITO using the electron beam deposition system. The ITO and grids make the front contact. Aluminum is deposited by electron beam deposition system as the back contact. In this thesis, we analyze samples with four cells sharing a common substrate back contact (Fig.2.2). The area of each cell is $0.56 cm^2$.

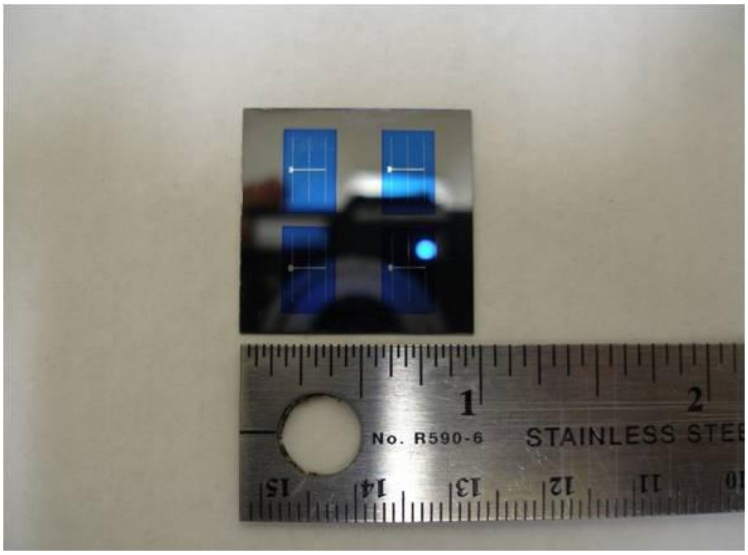

Fig. 2.2: A front junction silicon solar cell piece with four cells is shown.

2.3 The a-Si/c-Si heterojunction

2.3.1 Band diagram of a pn solar cell

The band diagram of a pn homojunction is shown in Fig. 2.3. Light enters through the (p) side and is absorbed in the absorber where the electron-hole pair is generated and the minority carriers are collected an measured. The built-in voltage is ϕ_i. This is bigger than the band-bending or diffusion voltage in the diagram. The band gap (E_g), conduction band (E_c), The Fermi level (E_f), and the valence band (E_v) are shown in the band diagram. The details of junction physics are discussed in any device book [5].

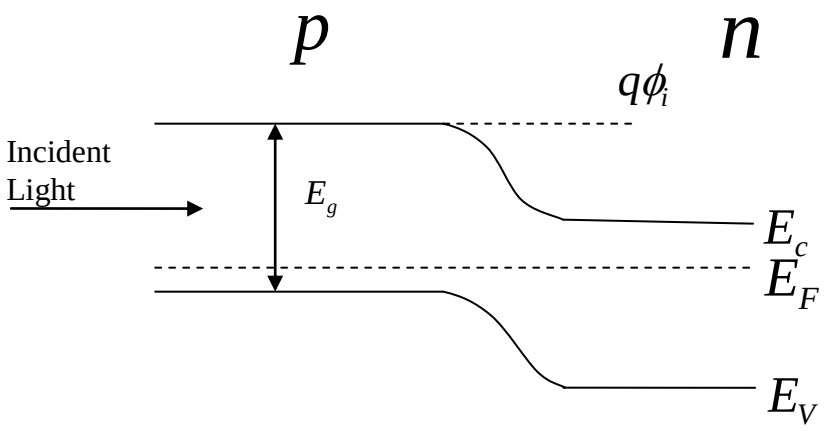

Fig. 2.3: Band diagram of a pn junction in a solar cell. The built-in voltage is higher than the band-bending effect as seen.

2.3.2 Equivalent circuit of a solar cell

The equivalent circuit of a solar cell consists of a diode, current source and parasitic series and shunt resistors as shown in Fig.2.4. Shunt resistance is caused by the loss of current due to defects and impurities. Series resistance is due to the bulk

semiconductor, the contact resistance between the metal and the semiconductor, and the lateral resistance in the ITO and grid contacts. A single diode model is not assumed in this thesis since we assume that the recombination at the junction is lower compared to the recombination at the surface [7].

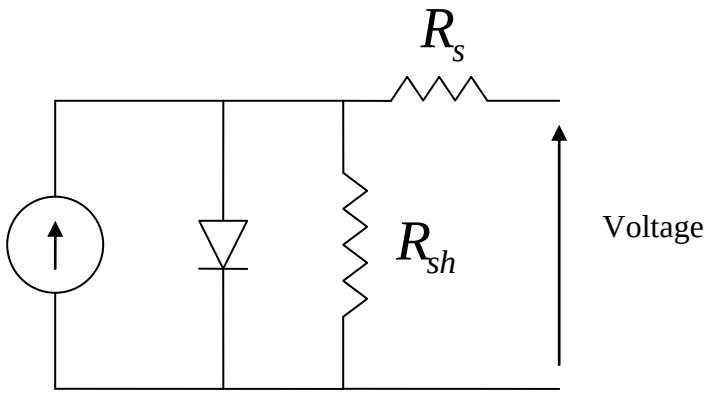

Fig. 2.4: Lumped DC circuit model under illumination of a solar cell.

2.3.3 Inversion layer and interface

At the heterojunction interface, there is an energetic barrier that carriers have to overcome due to the band offsets. The band gap of a-Si is approximately 1.7eV while the band gap of c-Si is 1.12 eV. the (p) a-Si:H/ (n) c-Si wafer junction band-bending is strong due to the difference in Fermi level and the high-doping of the a-Si layer. The strong band-bending induces an inversion layer at the surface. At the inversion location, the fermi level is close to the valence band. The inversion layer

attracts the minority carriers and repels the majority carriers; it works like an electronic junction. The electronic junction is not the actual junction between the two materials, but it is where carriers recombine. Since the electronic junction and the physical material interface junction are spatially separate in this case, the interface defects are low for this SHJ structure compared to other heterojunctions because recombination is low. Moreover, the quality of the surface passivation is improved due to the inversion layer since it reduces the recombination at the material interfaces. Surface inversion is shown in Fig. 2.5 [2].

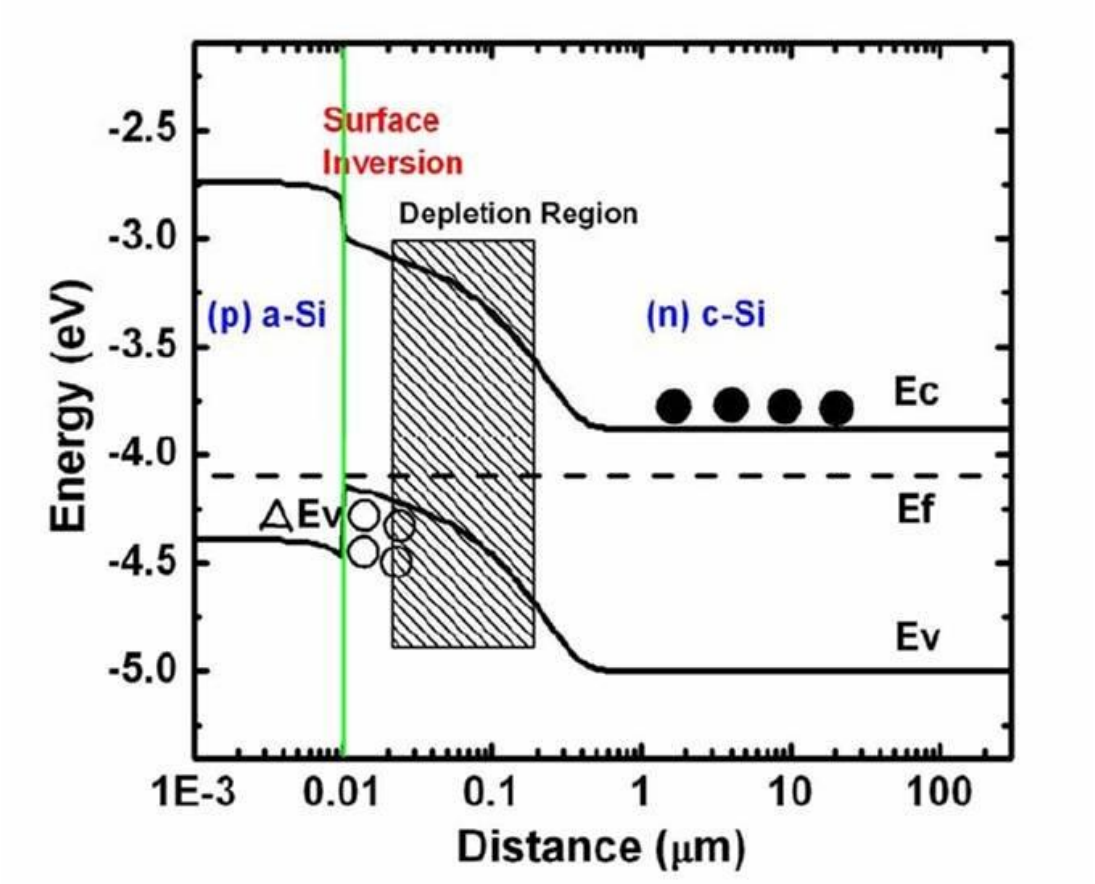

Fig. 2.5 The induced inversion layer improves the quality of passivation and reduces the interface effects [2].

2.3.4 Band offsets

At the junction, the conduction and valence band offsets ΔE_V and ΔE_C are formed due to the heterojunction (Fig. 2.6). In our structure, it is found that the valence band offset is blocking to the holes while the conduction band offset is ohmic to the electrons from modeling using AFORS-HET modeling. Internal photoemission is used to obtain the offsets.

Because the amorphous silicon emitter layer is highly doped and very thin, most of the depletion region is in the c-Si wafer. The depletion region in the a-Si layer is negligible from equation below.

$$x_n N_d = x_p N_a \tag{2.1}$$

where x_n, and x_p are the depletion widths in c-Si and a-Si and N_d and N_a are the doping concentrations[5].

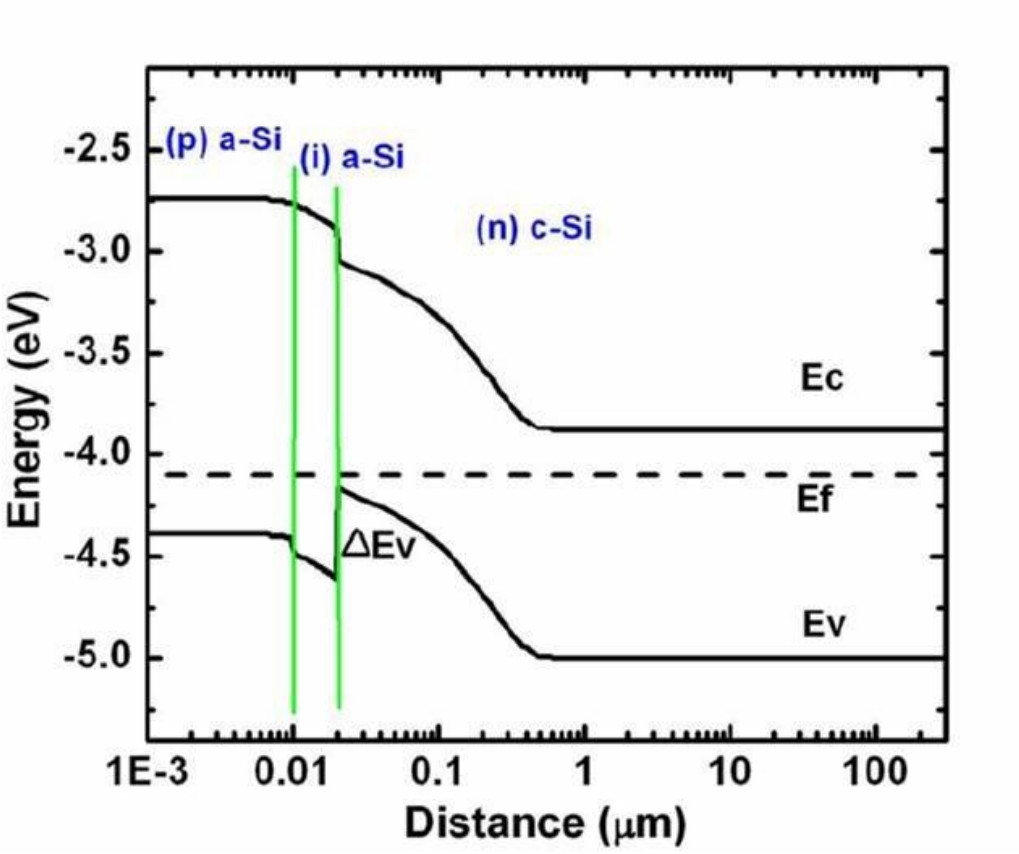

Fig. 2.6 shows the band diagram of a SHJ solar cell from AFORS-HET modeling. The valence band offset is greater due to the difference in Fermi levels of a-Si and c-Si materials [2].

2.4 Types of cells we analyze

The cells we analyze to understand the impact of processing on cell performance belong to three categories that differ in

1. The old and the new etch methods
2. With and without i-layer on either or both sides
3. With and with out piranha etch between depositions

Piranha etch is done using sulfuric acid: hydrogen peroxide (2:1) to clean the surface. Throughout this paper, we will compare cells according to the three categories listed above and demonstrate the differences or similarities in excess defects, lifetime, barrier height, and other parameters. It should be noted that the Si wafers are n-type and the a-Si layer deposition conditions were nominally the same for all samples.

Chapter 3

ELECTRICAL MEASUREMENTS

3.1 Current density - voltage

3.1.1 Current density – Voltage measurement concept

Current density -voltage measurements are used to obtain open-circuit voltage, short-circuit current, fill factor and efficiency, which determine the cell's performance. A four-point probe technique is used to contact and measure the cells under illumination of 1kW per square meter of AM 1.5 spectrum using Oriel solar simulator. The high potential and current probes are connected to the p-side and the low potential and current probes are connected to the n-side. The cell temperature is held constant at $25^{o}C$. A voltage source is used to set the voltage, and an ammeter measures the current. No current flows through the voltage loop. Fans and shutters are also part of the system.

3.1.2 Current density-voltage measurements

Before the solar cells are measured, the lamp is calibrated with a standard silicon solar cell. The light intensity is adjusted by varying the power to the 1000 W Xe arc lamp to match the short-circuit current of the standard cell obtained when it was calibrated at NREL under a Class A simulator. Then a current density-voltage (J-V) curve is obtained using the J-V system. The standard silicon solar cell is then

contacted in the front (p-side) by the high current and voltage probes, and cell is placed on a stage. The back of the cell (n-side) is connected to the other set (low potential and current) of probes. A mask is used for our front heterojunction silicon solar cells because the cell can collect current from the edges leading to inaccuracies in short-circuit current and open-circuit voltage. Source Measure Unit (SMU) consists of a voltage source and an ammeter. The voltage source sweeps the voltage from -0.6V to 1.2V taking 400 points, and the ammeter measures the current in the device. Dark and illuminated J-V curves are obtained.

Fig 3.1: JV system at the Institute of Energy Conversion. The simulator lamp shines on the sample placed on the stage. On the right is the source measurement unit which sweeps the voltage and measures the current.

3.1.3 Temperature dependent current-voltage equipment and measurements

Standard J-V measurements must be performed with the sample at 25^oC, However, additional insight can be gained by measuring the J-V curves as a function of temperature to identify thermally dependent recombination mechanisms, activation energy, and contact barriers. To accomplish this, we have assembled equipment including the thermoelectric cooler, power supply and a circuitry board. This setup can be used for controlling temperature for a range of measurements: current density-voltage, capacitance-voltage, or quantum efficiency. The cooler temperature can be set from 0^oC to 100^oC. A thermocouple is placed on the stage to a side. In Fig. 3.2, the stage in the J-V system is replaced by the cooler for JV-T measurements. A (magnetic) metal piece with cut-out hole is placed over the stage to conveniently place the probes on the metal and contact the cell. The cell is placed in the cut-out hole. The temperature is set using the keypad on the circuitry board. Optionally, the temperature can be set using a monitor. Initially, a J-V measurement is made at 25^oC using the standard stage and probes for later comparison with the measurement made on the stage. Then, the measurements are taken starting from 15^oC to 95^oC in increments of 10^oC. Frost and condensation becomes a problem for temperatures below 10^oC. The temperature is brought back down to 25^oC and J-V measurements are taken again. The JV measurements made at 25^oC before, during, and after are compared to observe changes in the cell performance. This method also assures accuracy and reliability of the measurements. Voc-T plots are also obtained from the same data.

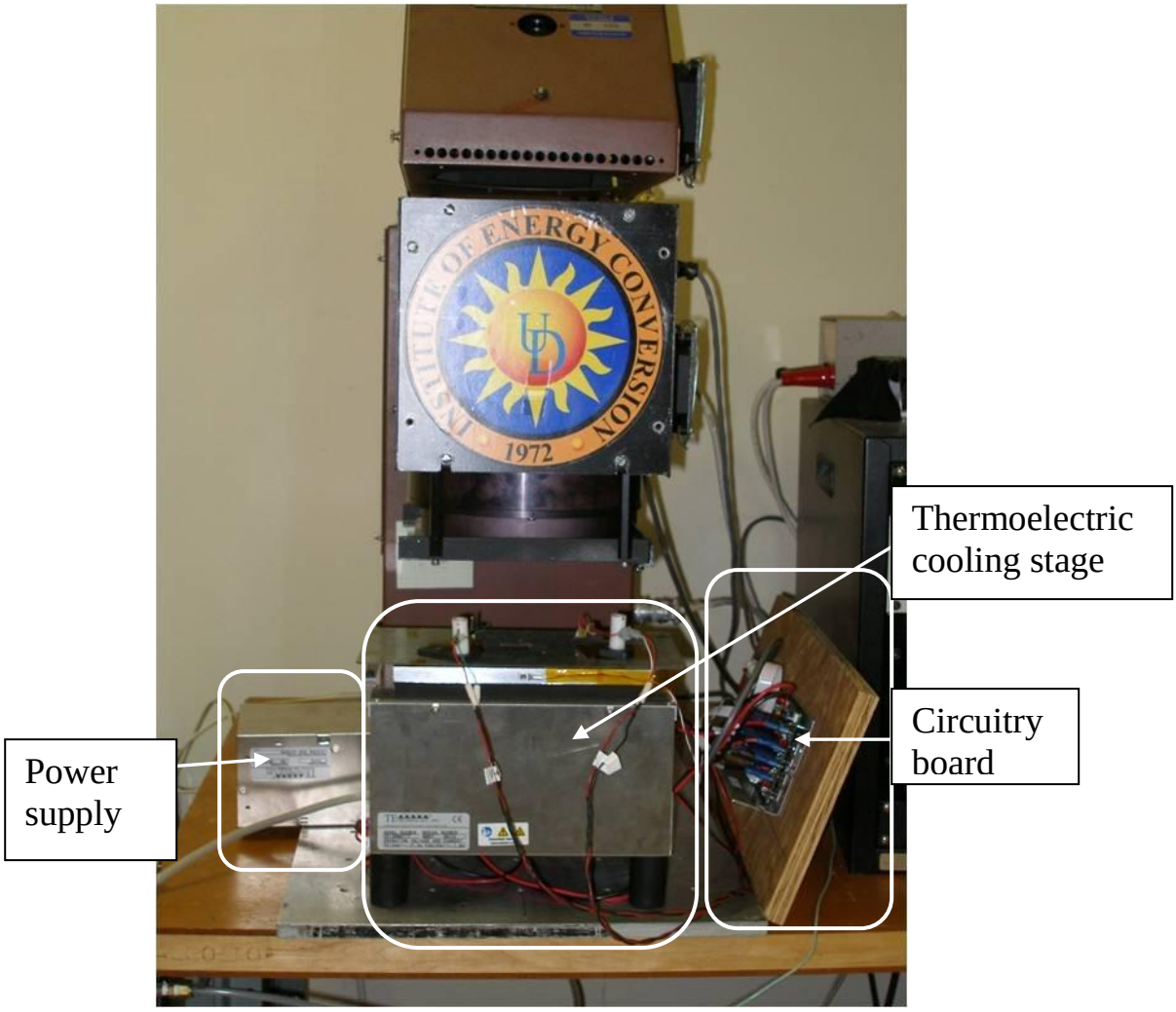

Fig. 3.2: JV-T measurement setup. A monitor can be used in place of the circuitry board.

3.2 Capacitance

3.2.1 Capacitance measurement Setup

The capacitance measurement setup includes an Agilent 4284A LCR (inductor, capacitor, and resistor) meter, a voltage source, a multimeter, and a bipolar power supply. Four coaxial cables connect the LCR meter to the sample [8]. The voltage

source provides the DC bias while the multimeter reads the voltage bias of the cell. The bipolar power supply sets the voltage determined by the LabView program. The LCR meter produces a small alternating current signal to measure the impedance of the solar cell. The DC and AC signals are applied additively to the sample via the external bias adaptor shown in the foreground of figure 3.3. Four-point probe system is used to measure the capacitance of the Device Under Test (DUT) or the sample.

Fig. 3.3: Capacitance system. Shown are the LCR meter (bottom), the external bias adaptor, multimeter, bipolar power supply, and the voltage source.

3.2.2 Capacitance-Voltage measurements

For the devices studied here, the voltage is swept from -2.0V to 0.5V and the capacitance of the cell was measured at each frequency, which is varied from 100Hz to 1MHz. LabView software is used to set the conditions for the capacitance system. A plot of capacitance-voltage and another plot of $\frac{1}{C^2}$ vs. V are displayed during the measurement. From $\frac{1}{C^2}$ vs. V plot, the diffusion voltage, the i-layer thickness, the free and the excess carrier density are obtained. At different frequencies, the C-V measurements can probe different energy levels, E_t:

$$E_t = kT\ln(\frac{\nu}{\omega}) \tag{3.1}$$

Where $\omega = 2\pi f$ is the angular frequency, kT = 0.026eV, k is the Boltzmann's constant, T is temperature, and $\nu = 10^{12} s^{-1}$ is the attempt-to-escape frequency.

E_t separates the shallow states that can follow the angular frequency from the deeper states that cannot respond [9].

3.2.3 Impedance Spectroscopy measurements

For admittance measurements, frequency-dependent capacitance is measured where the frequency is varied from 100Hz to 1MHz at a voltage bias in the dark. The ac voltage is kept small during the measurements to ensure a linear charge response

dQ = C dV [13]. Admittance measurements are used to determine the density of states as a function of energy level in the band gap. Several sources [10,11,12] have shown that the minority carrier lifetime is obtained in forward bias where minority carrier injection and accumulation occurs. We measured our cells at 0.4V bias in the dark. Capacitance measurements performed in forward bias are labeled impedance measurements. Impedance Spectroscopy measurements used to obtain minority carrier lifetime are discussed in detail in chapter 6.

3.2.4 Deep-Level Capacitance Profiling measurements

Deep-Level Capacitance Profiling is used to obtain the distribution of density of states as a function of distance and energy. This measurement is only sensitive to the bulk states, and does not measure the interface or trap states. It was developed specifically to detect the density and spatial profile of defects in a-Si devices [13,14]. In all other capacitance or admittance measurements, the ac voltages must be much smaller than the applied dc voltage so that the small signal approximation can be applied. Unlike these other measurements, the ac voltages used in DLCP are large, so the nonlinear terms are important to consider:

$$\frac{dQ}{dV} = C_0 + C_1 dV + C_2 (dV)^2 + \ldots. \qquad (3.2)$$

The free-carrier density is given by eq.3.3 [13]. A is the area of the cell, and C_o and C_1 are the coefficients from eq. 3.2.

$$N_{DL} = -\frac{C_o^{\ 3}}{2q\varepsilon A^2 C_1} \tag{3.3}$$

The emission energy is given by,

$$E_e = -kT \ln \frac{\omega}{2\pi \nu_o T^2} \ , \ \nu = \nu_o T^2 \tag{3.4}$$

The frequency and the temperature can be set to determine the emission energy at which the charge can follow fast enough to respond to the signal.

DLCP measurements use both ac and dc voltage to change the depletion width region allowing to accurately determine the free-carrier density. At each fixed dc voltage bias point, a varied ac voltage ΔV_{ac} is added. V_{ac} is varied from 10mV to 310mV in steps of 30mV (Fig. 3.4). At each ac voltage, the dc voltage is adjusted accordingly so that the total voltage applied is always the same. The measurements are repeated for a range of dc voltages at frequencies ranging from 1 kHz to 1 MHz in decades to obtain carrier concentration at different frequencies as a function of spatial position.

$$V_{total} = V_{dc} + \Delta V_{ac} \tag{3.5}$$

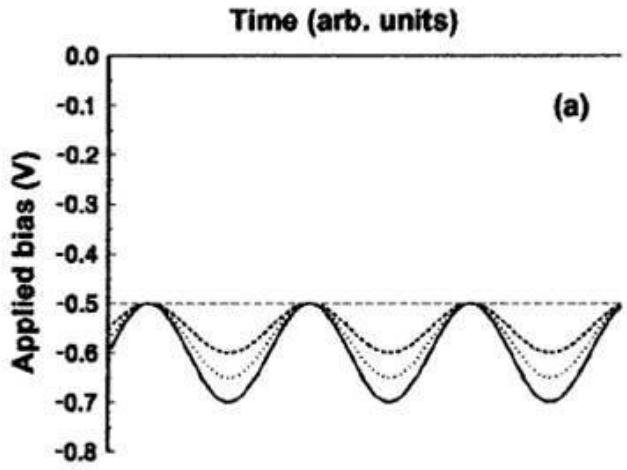

Fig. 3.4: The ac signal of decreasing amplitude is applied at a dc voltage of -0.5V in an example [13].

The total voltage increases as the ac voltage is increased. Assuming the depletion width is at x for a given dc bias, the edge of the space charge region will increase by Δx as the ac voltage oscillates. The only charge that can respond is from the edge of SCR to the new position or from x to $x + \Delta x$. The response time is short and only static charge can respond. Therefore, it is possible to measure free-carrier density more accurately using this measurement [13].

3.3 Quantum Efficiency

3.3.1 Quantum Efficiency equipment

Quantum Efficiency is the ratio of the number of electrons collected to the number of photons incident on cell. The efficiency ranges from 0 to 1, where no collection of electrons is a QE of zero and absorption of all incident photons and

conversion to collected electrons yields a QE of unity. The QE setup is shown in figure 3.5.

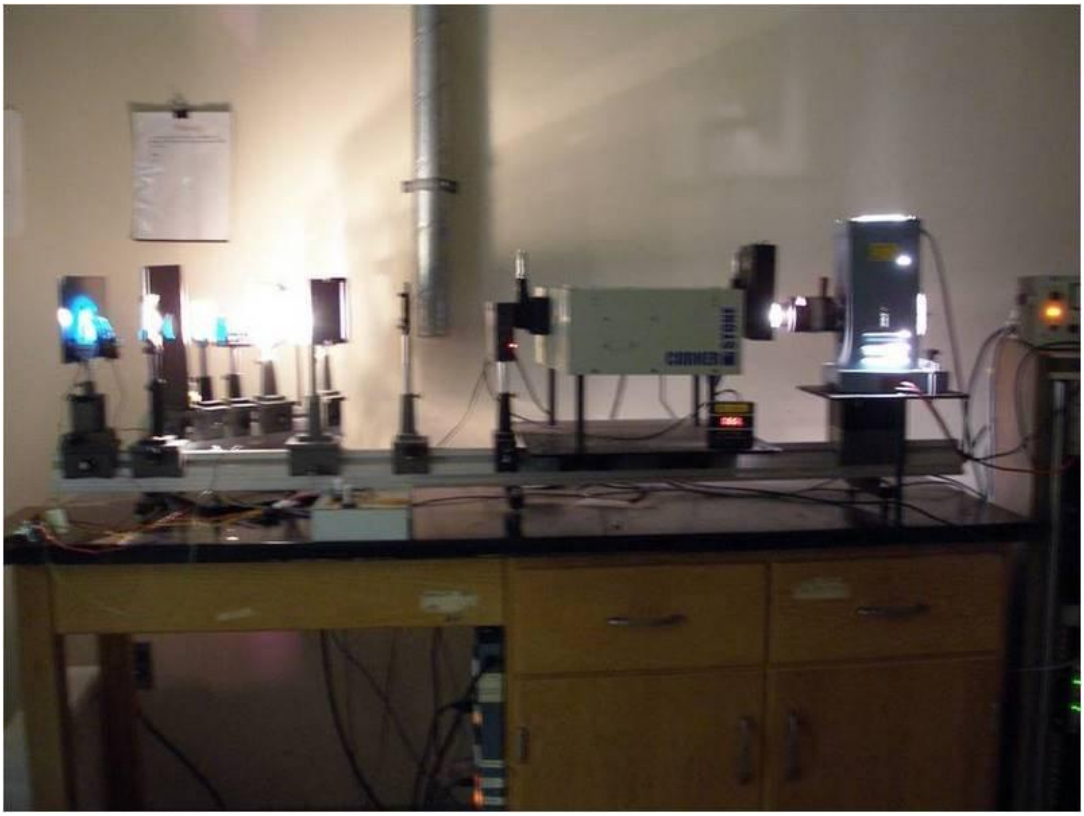

Fig. 3.5: (from left side) Sample mount, collimating and focusing lenses, chopper, monochromator, filter wheel, and the light source.

From the right side of the picture, a 200W quartz tungsten halogen projector lamp in blue is the light source. Light passes through the filter wheel and through the monochromator, which disperses the white light using the ruled grating. The monochromatic light goes through the light chopper that operates at 72 Hz and passes the collimating and focusing lenses. A small beam with an area of 4 millimeter square is focused on the sample, which is mounted on the stage as shown on the left side of

the picture. The probes at the sample collect the signal and send it to the IV converter where gain can be adjusted if necessary. The signal is then sent to the oscilloscope and the lock-in amplifier; the amplifier matches this signal with the signal from the chopper. The ammeter and the voltmeter monitor the current and voltage of the system. The QE system is controlled by a computer.

3.3.2 Internal Photoemission measurement

Quantum Efficiency measurements are usually taken at a voltage bias in a typical range of 350-1200nm either in light or dark. A LabView program is used to set the conditions. At each wavelength, a number of samples per point and the step size of the wavelength are chosen.

Internal Photo Emission (IPE) measurements use the same equipment. This measurement looks at the response of the junction to very weakly absorbed photons, hence the signal is very small. This requires different conditions compared to standard QE where the signal is much greater. The number of samples per point is increased to 20 points per sample, and the wavelength step size is decreased to 5nm to improve sensitivity of the measurement. The wavelength range chosen for Si IPE is between 900-1400nm, which is near the band gap of Crystalline Silicon. The valence and conduction band offsets can be obtained from these measurements. They will be discussed in detail in chapter 8.

Chapter 4

PERFORMANCE OF CAPACITANCE SYSTEM

4.1 Parallel RC Circuit model

A parallel Resistor-Capacitor (RC) circuit model is assumed for the solar cells analyzed here. The impedance of the circuit can be written as:

$$Z = R + iX, \tag{4.1}$$

where R is the resistance and X is the reactance. Admittance is the inverse of Z, and can be written as:

$$Y = G + iB, \tag{4.2}$$

where G is the conductance, and $G = \frac{1}{R}$.B is the susceptance, and $B = 2\pi fC = \frac{1}{X}$.

C is the capacitance and f is the frequency. The LCR meter measures the conductance and the capacitance at the set frequency range. A more realistic model would include series resistance, but the series resistance of the cells we measure is about 1Ωon average, so it can be ignored in comparison to other resistance values in the device [8] .The impedance for the parallel equivalent circuit model can be rewritten as:

$$Z = \frac{1}{i\omega C + \frac{1}{R}} \tag{4.3}$$

$$Z = \frac{R}{1 + i\omega\tau} \text{ and } \tau = RC. \tag{4.4}$$

Equation 4.3 is simplified into equation 4.4. Equation 4.4 can be separated into the real and the imaginary parts by multiplying the numerator and denominator by the complex conjugate as show in equation 4.5. τ is the recombination lifetime [15].

$$Z = \frac{R}{1+\tau^2\omega^2} - i\frac{R\tau\omega}{1+\tau^2\omega^2} \tag{4.5}$$

The real part and the imaginary part of the impedance are plotted to obtain minority lifetime in a solar cell. The details on obtaining the minority carrier lifetime are discussed in chapter 6.

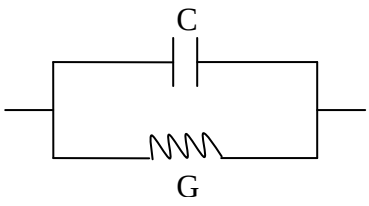

Fig. 4.1: A simple parallel circuit model of a solar cell is shown.

4.2 LCR meter reliability

Before discussing the capacitance measurements and results, it is important to show that the capacitance system measurements have only minor error deviations. Moreover, the measurements are repeatable. The error in measurements is checked using simple RC circuits made from twisting and soldering a capacitor and a resistor together in parallel. Repeatability of an instrument is crucial to be able to compare different sample data adequately. The repeatability of the measurements was checked using a standard diffused junction silicon calibration cell used to calibrate the quantum efficiency system at IEC.

4.2.1 Measurement error

Two parallel RC circuits were made for the purpose of demonstrating the performance of the LCR meter. They are shown in table 4.1. In each case, a resistor was soldered on to a capacitor to make a parallel RC circuit. Both capacitors have the same value while the resistors had values of 3 and 13 kohms. Then, admittance measurements from 1 kHz to 1 MHz were performed and the resistance of the circuit was derived from the real (conductance) part. The two models shown in table 4.1 were selected to represent two different scenarios during capacitance measurements. Model A represents the device at forward bias when the depletion width is narrow, and the resistance is small. Model B represents the device at reverse bias when the depletion width is wide, so the resistance is large. The measured average values over a range of frequencies agree well for Model A. But they do not agree for Model B. This could be because as the frequency increases in Fig. 4.1, the impedance of the capacitor increases so the resistance across the resistor decreases. Therefore, the average resistance is lower than the rated value.

Circuit model	Capacitor Rated Value (nF)	Capacitor measured average (nF)	Resistor Rated value (ohms)	Resistor measured average (ohms)
A	33.0 +/- 10%	39.9 +/- 9.8%	3.00 +/- 5.0 %	3.30 +/- 0.6%
B	33.0 +/- 10%	33.9 +/- 1.6%	13000.00 +/- 5%	5911.85 +/- 78.1%

Table 4.1: Comparison of the resistor and capacitor values obtained from applying Eq. 4.3 to two pairs of discrete R and C.

There is some discrepancy between the average capacitor value from the measurements and the standard capacitor value. The difference could be because the values of capacitance and resistance of a circuit vary when the frequency is varied. It is also possible that when performing the measurements, they had to be made separately for each frequency range. For instance, a measurement was taken from 1 kHz to 10 kHz in steps of 1kHz. Then, another measurement was taken from 10 kHz to 100 kHz in steps of 10kHz at a later time and so on. The values are close, however, and this shows that the measurements are reliable.

4.2.2 Repeatability of the system

Each time the capacitance system was turned on, a capacitance-voltage measurement was swept from -2.0V to 0.5V at 100 kHz on the calibration cell before doing the actual measurements. The data for the calibration cell was collected and compared periodically to check the system's repeatability.

From the plots of $\frac{1}{C^2}$ vs. V, the doping concentration of the silicon was obtained and the results are shown for nine measurements (Fig. 4.2) taken over eleven months. Their carrier concentrations, standard deviation, and the percent error are shown in table 4.2. Clearly, the C-V system has excellent repeatability and stability.

Measurement number	carrier concentration (cm^-3)
1	6.15E+15
2	6.15E+15
3	6.09E+15
4	6.15E+15
5	6.18E+15
6	6.15E+15
7	6.15E+15
8	6.18E+15
9	6.18E+15
average	6.15E+15
standard dev.	2.52E+13
%error	0.41

Table 4.2: Results of carrier concentration obtained from Si calibration cell for 9 measurements over eleven months. Actual data is plotted in figure 4.2. The small percent error shows that the measurements are repeatable.

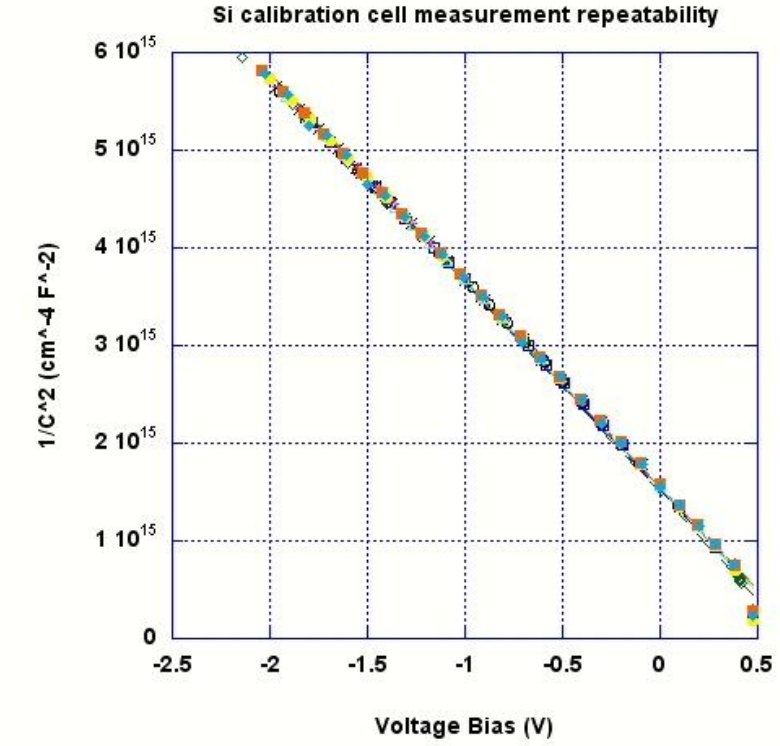

Fig. 4.2: Shown are nine different measurements plotted together. All the measurements agree well.

Chapter 5

VARIOUS C-V METHODS

5.1. Junction capacitance

The junction capacitance is given by:

$$C = \sqrt{\frac{q\varepsilon_s N_d}{2(\phi_i - V_a)}}, \text{ where } \varepsilon_s = \varepsilon_0 \varepsilon_r \qquad (5.1)$$

N_d is the free-carrier concentration, ε_0 is the permittivity of vacuum, ε_r is the relative permittivity, ϕ_i is the diffusion voltage, and V_a is the applied voltage [5]. The above equation can be rewritten as

$$\frac{1}{C^2} = \frac{2(\phi_i - V_a)}{q\varepsilon_s N_d}. \qquad (5.2)$$

Carrier concentration is obtained from the slope of the $\frac{1}{C^2}$ vs. V_a plot (also called Mott-Schottky plot). However, not all plots are linear, and some assumptions are made for a linear slope.The assumptions are that the junction is abrupt and there is low-injection of carriers in the cell [16]. The measured carrier concentration is the same as the doping density of the c-Si wafer, (approximately $1-3\times10^{15} cm^{-3}$) at 1MHz. They are the same because at this frequency, the time is too short for the carriers to respond to the signal, and only shallow states are probed allowing only the free-carriers in the wafer to be detected. The x-intercept gives the band-bending or the diffusion voltage.

This is not the same as the built-in voltage which is greater than band-bending (see Fig. 2.3) [5].

Impedance measurements at IEC can be performed between 100Hz to 1MHz, allowing us to probe energy levels 0.55eV (at 100Hz) and 0.31eV (1MHz) in energy, assuming T = $25^{o}C$. These correspond to the deepest and shallowest states that can respond at that temperature, assuming

$$E_t = kT\ln(\frac{\nu}{\omega}) \tag{5.3}$$

and an attempt-to-escape energy, $\nu = 10^{12}s^{-1}$ as discussed in chapter 3 [9].
A typical C-V plot of a pn junction solar cell is shown in Fig.5.1.

5.2 Excess defects

At high frequencies, the signal is too fast for the charge in deep states to respond so only the shallow states are probed, therefore only the dopant density of the c-Si wafer is measured. At lower frequencies the deeper energy levels (defects) can follow the signal by capturing and emitting charge during the ac cycle. Thus, frequency dependence probes shallow and deep states. Any excess defects can be measured at sufficiently low frequencies or high temperatures. Typically in c-Si, the deep defect density is low and there is no frequency dependence but for some of our cells, we see significant increase in capacitance at low frequency, corresponding to an excess of defects over the background free carrier density. The total carrier density responding to the ac signal can be expressed as

$$N_{total} = N_d + \Delta N_{excess}, \qquad (5.4)$$

and N_d is the c-Si wafer dopant density determined from high frequency response. The excess defects can be due to poor surface passivation during cleaning or fabrication processes. They can be located at the interface or the bulk.

C-V measurements were performed on two different groups of cells. Most of the $\frac{1}{C^2}$ vs. V_a plots from the first group were not frequency dependent. This is expected since the deep defects in c-Si wafer and interfaces should be very low if the cell was properly designed and fabricated. In the second group, the charge concentration obtained from the slope of $\frac{1}{C^2}$ vs. V_a plot is frequency dependent for most samples. Although both groups had similar structure and fabrication methods, they had different defect densities at lower frequencies. The wafer source, bulk properties, texture, and the fabrication of the solar cells from wafer scribing to the deposition of contacts were supposedly the same. The first group of cells was cleaned using detergent using the following procedure:

1. Detergent ultrasonic for two minutes.
2. High pressure water rinse for two to three minutes.
3. DI water ultrasonic at ~90C for three minutes.
4. Piranha etch for three minutes.
5. DI water rinse for five minutes.
6. HF etch (10%) for one minute.

The cleaning procedure used for the second group is similar to the cleaning procedure given in chapter 2 without steps 3 and 4. Both samples shown in Fig. 5.1 and Fig. 5.2 have the same structure and fabrication process except for the cleaning as noted above. The sample shown in Fig. 5.1 does not show frequency dependence while the sample in Fig. 5.2 does. There is also a correlation between open-circuit voltage and excess defects. Most samples with higher open-circuit voltage have low defects. The relation between open-circuit voltage and excess defects is discussed further in section 6.2.1. However, no relation is observed between fill factor and excess defects. It is possible that the excess defects affect the open-circuit voltage but not the fill factor.

Samples from First Group				
Sample	**Structure**	**Voc (V)**	**FF %**	**Excess defects (cm^-3)**
MC0261	10nm.p/10nm.i/n.c-si(100)/10nm.i/30nm.n	0.591	48.9	1.51E+15
MC0080-14	100Ap/150Ai-n-10Ai/100An	0.627	73.1	6.62E+13
MC0080-10	100Ap/50Ai-n-10Ai/100An	0.626	71.2	9.45E+13
MC0081-12	100Ap/10Ai-n-150Ai/100An	0.6	76.3	6.02E+13
MC0080-04	100Ap/100Ai-n-10Ai/100An	0.681	24.5	1.16E+14
MC0468-03	Al/20nm.n/n.Si/10nm.std-p Fz(100)	0.606	73.6	1.67E+17
MC0468-11	Al/20nm.n/n.Si/10nm.std-p sptex	0.591	65.9	3.12E+17
MC0461-03	Al/a-si(30nm).n/a-si(8nm).i/n.Si(100)/a-si(8nm).i/a-si(10nm).p sptex	0.642	67.5	9.87E+14
MC0461-07	Al/a-Si(30nm).n/n.Si(100)/a-si(10nm).p sptex	0.583	68.6	2.74E+17

Table 5.1: Device structure and illuminated solar cell junction properties.

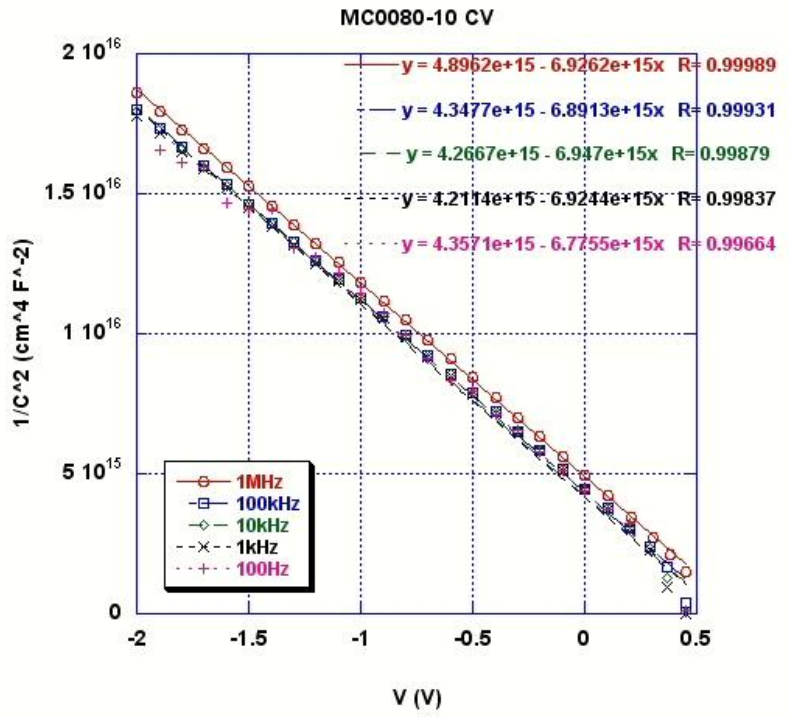

Fig. 5.1: 1/C^2 vs. V plot of a sample from first group at f =100Hz, 1kHz, 10kHz, 100kHz, and 1MHz. The slope is the same at all frequencies. Capacitance is not frequency dependent.

The slope is independent of the frequency from 100Hz to 1MHz in Fig.5.1. The slope gives charge densities of $1.88\times10^{15} - 1.93\times10^{15} cm^{-3}$ (from high to low frequency), and the intercept is 0.61-0.71V. This charge density is very consistent with the doping expected for a wafer with resistivity of 1-3 Ohm-cm. However, as seen in Fig. 5.2, the plots over the same range of frequencies for samples in the second group are frequency dependent for several samples. At 1MHz only shallow states are measured, the carrier density is similar to the cells in the first group. But at lower frequencies, as the measurements probe deeper states, excess defects that are present

in the samples from the second group are also measured. The samples in second group are shown in table 5.2.

Samples from Second Group Set 1 i-layer in back and no i-layers				
Sample	**Structure**	**Voc (V)**	**FF %**	**Excess defects (cm^-3)**
MC0534-01	30nm.n/n.Si(100)/10nm.p	0.616	71.3	9.44E+16
MC0537-02	30nm.n/10nm.i/n.Si(100)/10nm.p	0.554	68.5	2.88E+14
MC0532-01	30nm.n/n.Si(100)/10nm.p	0.616	70.9	1.24E+17
MC0532-08	30nm.n(H2=400, DC)/n.Si(100)/10nm.p	0.614	72.0	5.43E+17
MC0521-03	30nm.n/n.Si(100)/10nm.p	0.581	68.9	1.20E+17
Set 2	**i-layer in front and both i-layers**			
MC0534-04	30nm.n/n.Si(100)/5nm.i/10nm.p	0.651	76.3	7.04E+16
MC0534-05	30nm.n/n.Si(100)/10nm.i/10nm.p	0.654	75.8	1.22E+17
MC0534-08	30nm.n/n.Si(100)/20nm.i/10nm.p	0.662	68.7	2.59E+16
MC0537-04	30nm.n/10nm.i/n.Si(100)/5nm.i/10nm.p	0.646	52.6	6.92E+16
MC0537-10	30nm.n/10nm.i/n.Si(100)/10nm.i/10nm.p	0.663	46.6	1.09E+16
MC0537-12	30nm.n/10nm.i/n.Si(100)/20nm.i/10nm.p	0.663	46.1	2.86E+16
MC0544-04	30nm.n/145um Si(100)/5nm.i/20nm.SiNx/10nm.p	0.672	76.7	1.17E+16
MC0544-03	30nm.n/145um Si(100)/5nm.i/20nm.SiNx/10nm.p	0.645	76.4	5.78E+15

Table 5.2: Samples from second group are shown. The excess defects for most samples are relatively high compared to excess defects in the first group.

The slopes give charge densities of $1.77\times10^{15} - 7.8\times10^{16}$(from high to low frequency) and the intercept ranges from 0.66 to 2.96V. Unlike the sample in table 5.1,

the carrier density changes by an order over the frequency range. The diffusion voltage changes dramatically as well. However, at high frequency, the carrier density and the diffusion voltage are the same in both samples. This shows that at high frequency, only the shallow levels are probed and the carrier density is close to the wafer doping density that determines the junction capacitance (eq. 5.1).

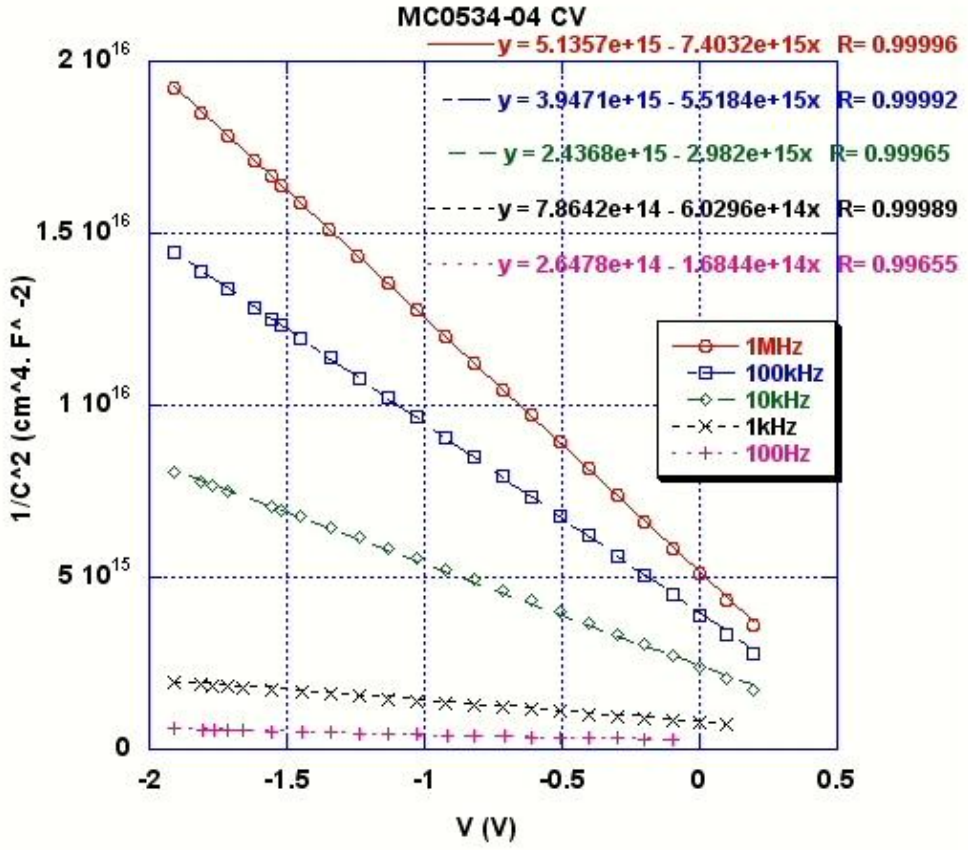

Fig. 5.2: The difference between the two groups is obvious. The samples in second group are frequency dependent.

The difference between the two groups can be observed with a plot of excess defects as a function of frequency. The excess defects that we measure can be calculated by subtracting the carrier concentration at high frequency from the carrier concentration at low frequency.

$$\Delta N_{ex} = N_{tot}(100Hz) - N_{tot}(1MHz) \tag{5.5}$$

A plot of excess defects vs. frequency is shown in Fig. 5.3. At high frequencies, there is no difference between the two groups, but at lower frequencies, the excess defects are observed in second group. The correlation between excess defects and device processing and device structure will be discussed later in this chapter.

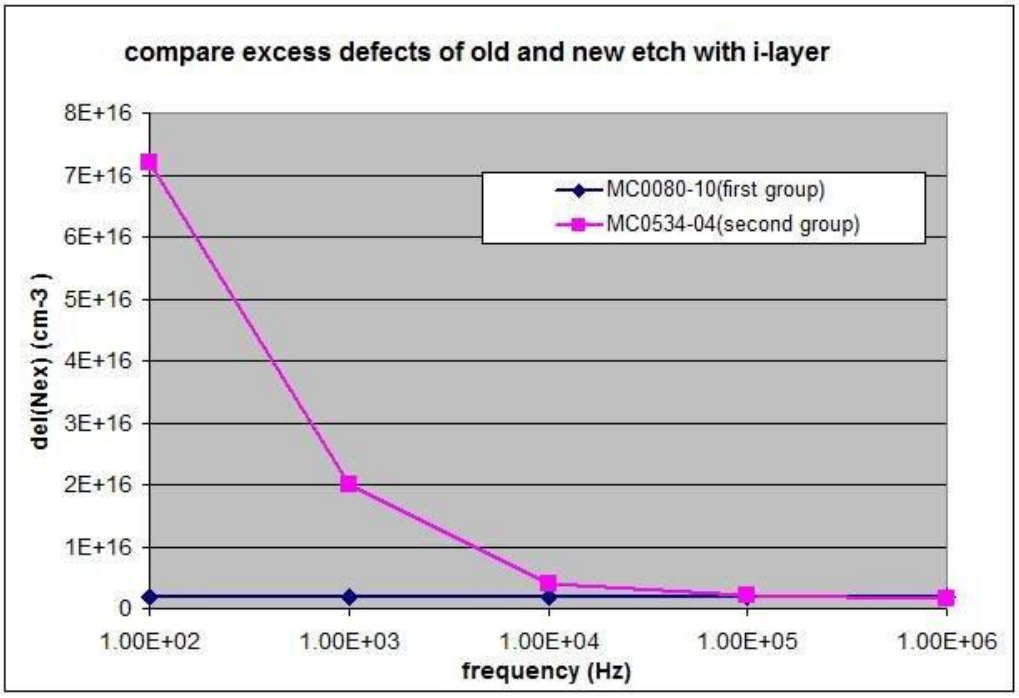

Fig. 5.3: At lower frequencies, the excess defects in the sample from second group are shown.

5.2.1 The effect of i-layer on Excess defects

The location of the excess defects is hard to figure out. Given that most of our c-Si wafers are float-zone, it is not likely that there are any defects in them. The amorphous silicon doped and intrinsic layers are no more than 30nm. They are too thin; therefore the depletion region is thin on the a-Si side, and it is possible that most of the excess defects that are measured using this method are in the depletion region on the c-Si side. The only other location is at the (p) a-Si/ (n) c-Si and the (n) c-Si/(n) a-Si interfaces where band misalignment exists. Part of the reason for the excess defects could be that the newer cleaning procedure is not cleaning the surface as

effectively. Further work is needed to determine the cause of excess defects in the samples from the second group.

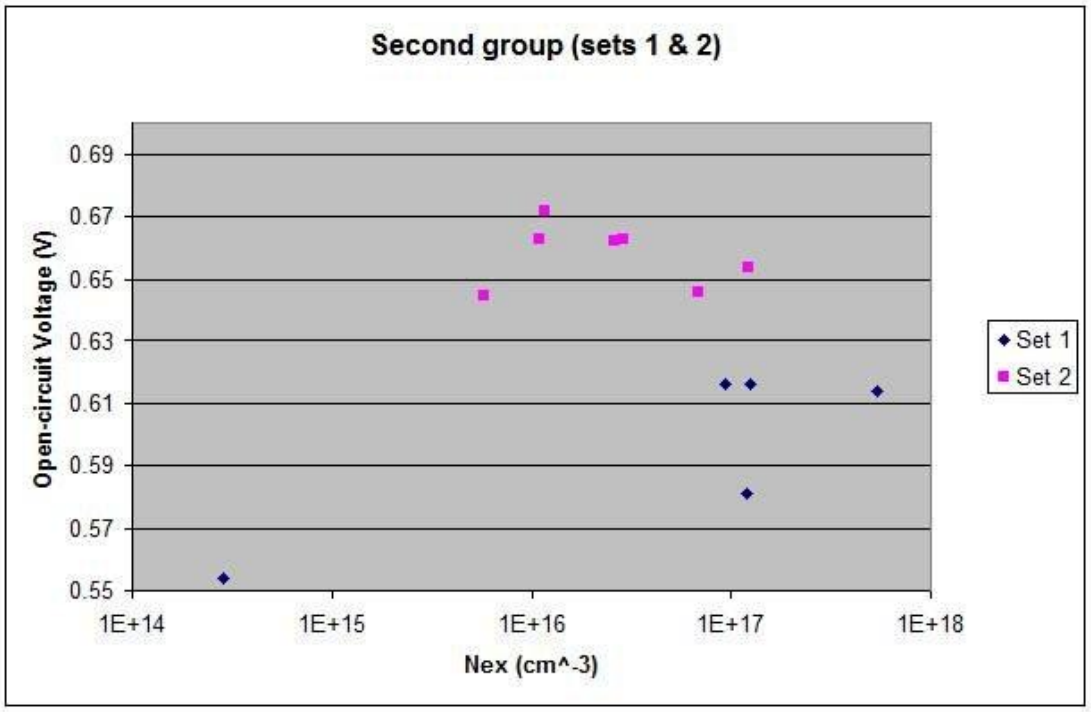

Fig. 5.4: samples from second group. Set one consists of sample with i-layer and Set two consists of samples without i-layer. Set one has an outlier on the left with low Voc and Nex.Voc from set two are on average 62mV higher than voc from set one and Nex is on average higher than the first set.

In the second group, the cells can be subdivided into two sets. The first set consists of samples without i-layer or with an i-layer only in the back (table 5.2). Second set has samples with front i-layer or with i-layers on both sides. The results are shown in the Fig 5.4. First set has an outlier. It is the only sample with just an i-layer in the back. Our results show that it has lower open-circuit voltage and low defects. But in general, it is observed from the figure above that the open-circuit voltage and excess defects improve with an i-layer in the front or on both sides. Moreover, it

seems that excess defects decrease drastically when a back i-layer is added. We only have one sample with just a back i-layer for this group, so we processed more samples, and we discuss them later.

The results suggest that by adding i-layer on both sides, the a-Si/c-Si interface is passivated by the i-layer. Using a better cleaning procedure (chapter 2) on some recent cells, we were able get lower excess defects overall. Our C-V measurements on them showed that the open-circuit voltage improves and the defects decrease by an order when i-layer is deposited on both sides (table 5.3). Therefore, it is logical to assume that excess defects reside at the interface. The effect of adding an i-layer in the back to the excess defects is shown in these samples.

5.2.2 Effect of back i-layer on excess defects

Another set of samples from the third group (table 5.3) had 20nm silicon nitride deposited on the i-layer (both front and back) and etched off later. These had some of the highest FF of any SHJ solar cells we made during this study. The results are shown in the graph (Fig. 5.5). The excess defects are independent of the fill factor as can be seen in the table. The samples that have lower excess defects also have higher open-circuit voltage.

Samples from Third Group				
Sample	Structure	Voc(V)	FF %	Excess defects (cm^-3)
MC0584-03 (run 1)	30nm.n/Si(100)/10nm.p	0.605	33.1	2.86E+16
MC0584-06 (run 1)	30nm.n/Si(100)/10nm.p	0.589	78.9	5.23E+16
MC0584-12 (run 2)	30nm.n/Si(100)/5nm.i/20nm SiNx/10nm.p	0.638	79.1	3.49E+16
MC0584-14 (run 2)	30nm.n/Si(100)/5nm.i/20nm SiNx/10nm.p	0.632	79.7	5.54E+16
MC0584-18 (run 3)	30nm.n/5nm.i/Si(100)/5nm.i/20nm SiNx/10nm.p	0.67	78.5	3.11E+15
MC0584-19 (run 3)	30nm.n/5nm.i/Si(100)/5nm.i/20nm SiNx/10nm.p	0.647	73.5	3.85E+15

Table 5.3: Samples from the third group are shown. The excess defects decrease by an order of magnitude for run 3 when the back i-layer was added.

We believe that during depositions and etching of SiNx, the defects at the interface between the i-layer and the doped layer decrease thereby improving the cell's performance. From Fig. 5.5, it's obvious to see that the open-circuit voltage improves by about 30mV from the first run to the second. The second run had a 5nm i-layer deposited in the front; there is no improvement in the excess defects. In the third run, a 5nm i-layer is deposited on both sides. And the open-circuit voltage is improves on average by 20mV and the excess defects reduces by an order. Adding an i-layer in the back improved the excess defects here as well. In the previous section, it is not so obvious between front and both i-layers. This might be because etching SiNx removed impurities at the interface and it is clear to see here. We also saw that there is a

significant improvement in excess defects when i-layer is in the back in this group. In conclusion, after the i-layer is deposited in the back, and if SiNx is deposited on the i-layer and etched off at the interface, the reduction of excess defects in the back is observed.

5.2.3 The effect of piranha etch

There is no difference in open-circuit voltage and excess defects between 584-03 and 584-06 (table 5.3). However, the FF improves drastically for 584-06 with piranha etch. We are still trying to understand this. A possible explanation is that during piranha etch, a layer was removed. Since the excess defects of the samples are the same, the layer that was removed may have changed the band alignment between the layers. This is discussed further in section 7.3.

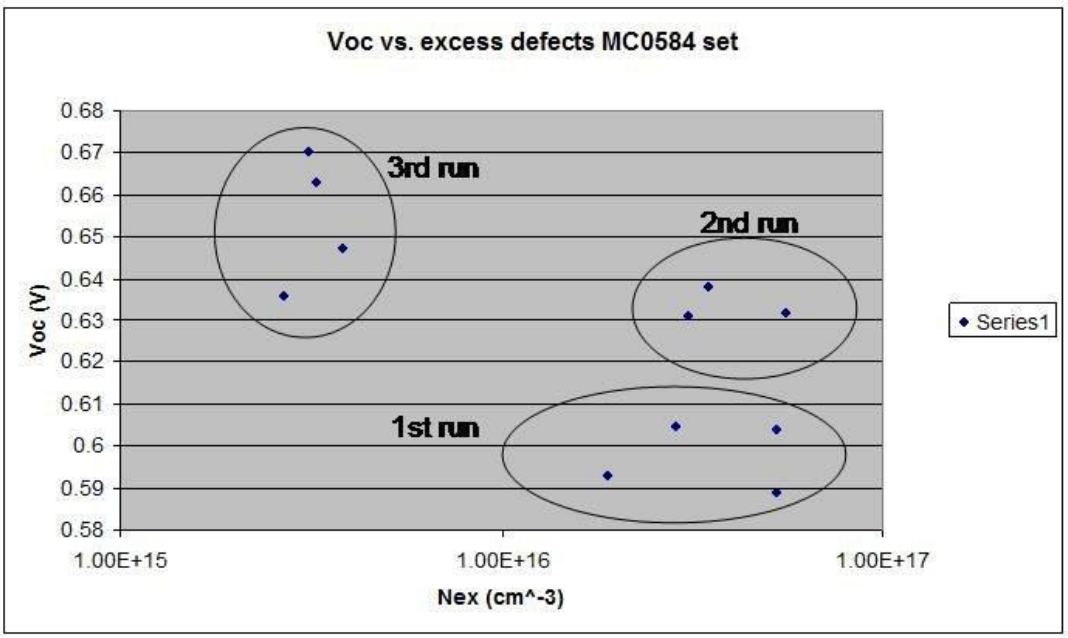

Fig. 5.5: Samples from the three runs for third group are shown. The samples in the third run have excess defects an order less than the first two runs. The addition of an i-layer in the back (for third run) could have decreased the defects [38].

5.3 C-V profile vs. DLCP

5.3.1 Capacitance-Voltage profiling

The previous C-V analysis assumed the charge density is uniformly distributed. But the net dopant or charge concentration can be plotted with spatial distance for a better understanding of the dopant variations using the relationship:

$$N_{cv} = -\frac{C^3}{\varepsilon q A^2}\left(\frac{dC}{dV_A}\right)^{-1} \tag{5.6}$$

vs. x where $x = \frac{\varepsilon A}{C}$ and x is the spatial distance(position) into the junction. The depletion edge probes the boundary between depleted and field free bulk.
The concentration profile gives the dopant density as a function of distance at different frequencies. It shows the defect density in the interface and trap states [17].

5.3.2 Deep-level Capacitance Profiling

Deep-level capacitance profiling is commonly used to determine the bulk carrier density in CIGS films, amorphous silicon, polycrystalline silicon, and other materials with high defect states in the band gap. This method can yield density of states in the bulk as a function of spatial position and energy. As discussed in section 3.2.4, the ac voltage is varied at a range of fixed dc voltages to obtain the free-carrier density as a function of distance. The measurements are performed at various

frequencies (10 kHz to 1 MHz) while varying the dc and ac voltages. The free-carrier density is

$$N_{DL} = -\frac{C_o^{\ 3}}{2q\varepsilon A^2 C_1} \tag{5.7}$$

as a function of spatial position. The coefficients C_o and C_1 are obtained from the plot of capacitance vs. applied ac voltage (fig 5.6). The measurement method was discussed in chapter 3.We will only use DLCP to look at the spatial distribution of defects in this paper. Moreover, this method is a more accurate way to determine the free-carrier density of the c-Si wafer compared to the C-V profile because unlike the C-V measurements, it is insensitive to trap states and the interface. Therefore, DLCP measurements give carriers concentrations about a couple of orders lower than the CV measurement [18,13].

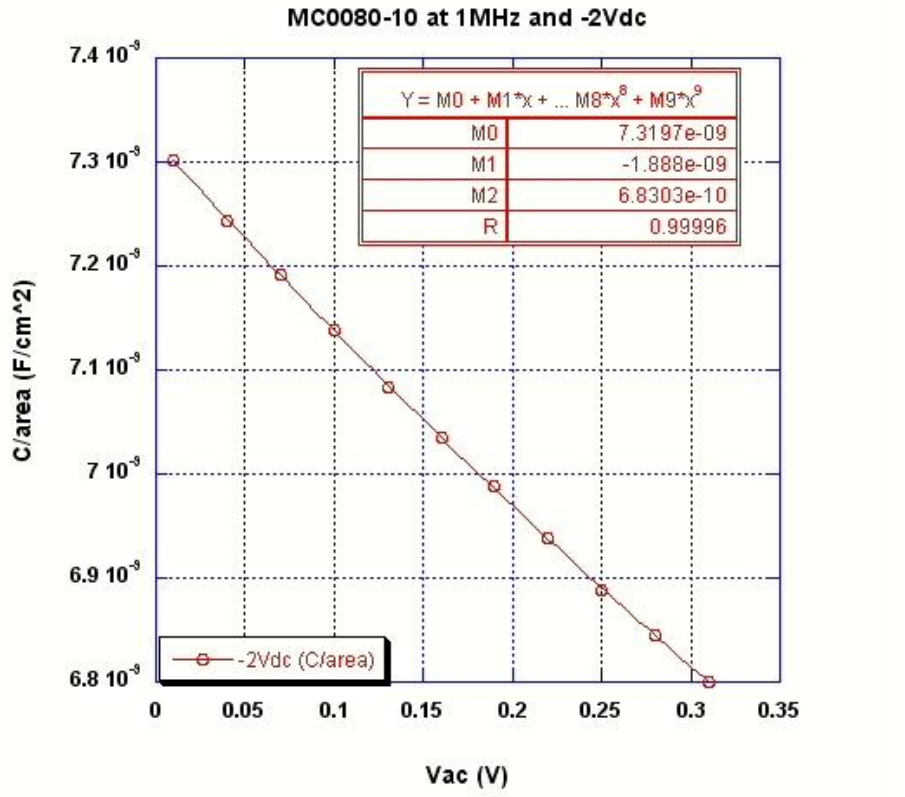

Fig. 5.6: A plot of capacitance vs ac voltage shows a polynomial curve from which the coefficients M0 (Co) and M1 (C1) in the graph are used to get the carrier concentration in equation 5.6.

5.3.3 C-V vs. DLCP method results

C-V profile and DLCP were obtained for two samples discussed in section 5.2 (MC0080-10 and MC0534-01). MC0080-10 is a sample with an older etch with frequency-independent capacitance while MC0534-01 is the sample with the newer etch with independent capacitance as discussed earlier. The results are shown in Figs. 5.7 & 5.8.

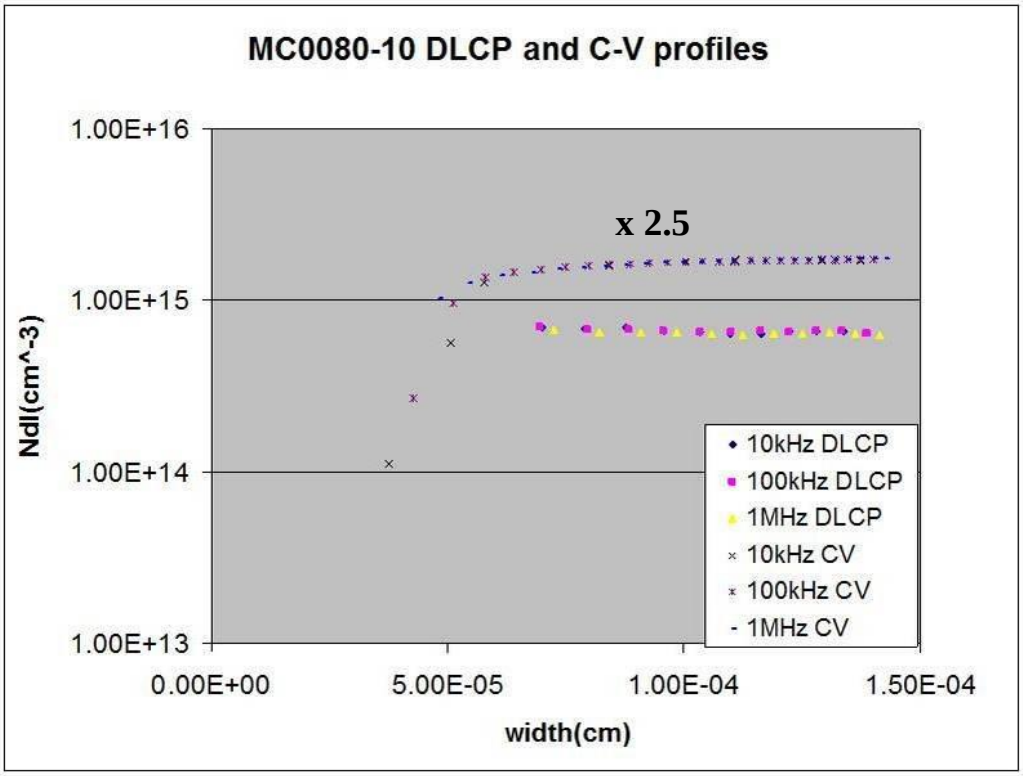

Fig. 5.7: DLCP and C-V profiles of a sample (MC0080-10) with old etch at 10kHz, 100kHz, and 1MHz. They differ by a factor of approximately 2.5.

For the sample with old etch (MC0080-10), Figure 5.7 shows that C-V measurements were the same at all frequencies and independent of depth. The same is true for DLCP measurements. For sample MC0080-10, the carrier concentration is $6.50\times10^{14}cm^{-3}\pm1.12\times10^{13}cm^{-3}$ from the DLCP measurements, and it is $1.65\times10^{15}cm^{-3}\pm2.38\times10^{13}cm^{-3}$ from C-V measurements. The carrier concentration from C-V measurements is approximately 2.5 times larger than carrier concentration from DLCP method. Cwil et al [18] attribute the difference in concentrations to the sensitivity of the DLCP measurements compared to C-V measurements where holes and charges in metastable traps are detected. DLCP measurements only measure the

free-carrier concentration. They have also reported that carrier concentrations from both measurements differ by a factor of 2. The authors concluded that the factor of 2 is a feature typical in MIS-type device.

Frequency	Average $N_{cv}(cm^{-3})$	Average $N_{dl}(cm^{-3})$	by factor
1MHz	1.42E+15	5.55E+14	2.56
100kHz	2.09E+15	8.44E+14	2.48
10kHz	6.44E+15	3.02E+15	2.13

Table 5.4: Data for MC0534-01 is shown. The carrier concentrations at different frequencies from both profiles are shown. They all differ by approximately a factor of 2. Table 5.2 shows basic parameters and defect density for the sample.

Sample MC0534-01 has an average carrier concentration which is strongly frequency dependent (table 5.4). At lower frequencies, the carrier concentration is higher while it is lower at high frequency. Once again, the concentrations from CV and DLCP differ by a factor close to 2. The similar difference in both profiles between the old and new etch suggests that measurements and calculations are not a problem. Table 5.2 shows that this sample has an excess defect density of $9.44\times10^{16}cm^{-3}$, and this suggests that defects were introduced into the sample somehow. Even the DLCP method, which is expected to be immune to trap or defect density shows that carrier concentration is frequency dependent. The differences between the two etches was discussed in section 5.2. Further work is required to understand the significance of the factor and the difference between the two etches. Profiling method is simply a way of expressing carrier or defect density discussed earlier. The carrier concentration is clearly seen here as the spatial position varies. Except the free-carrier density, no new

information is obtained. The carrier and defect density were related to basic parameters in this chapter.

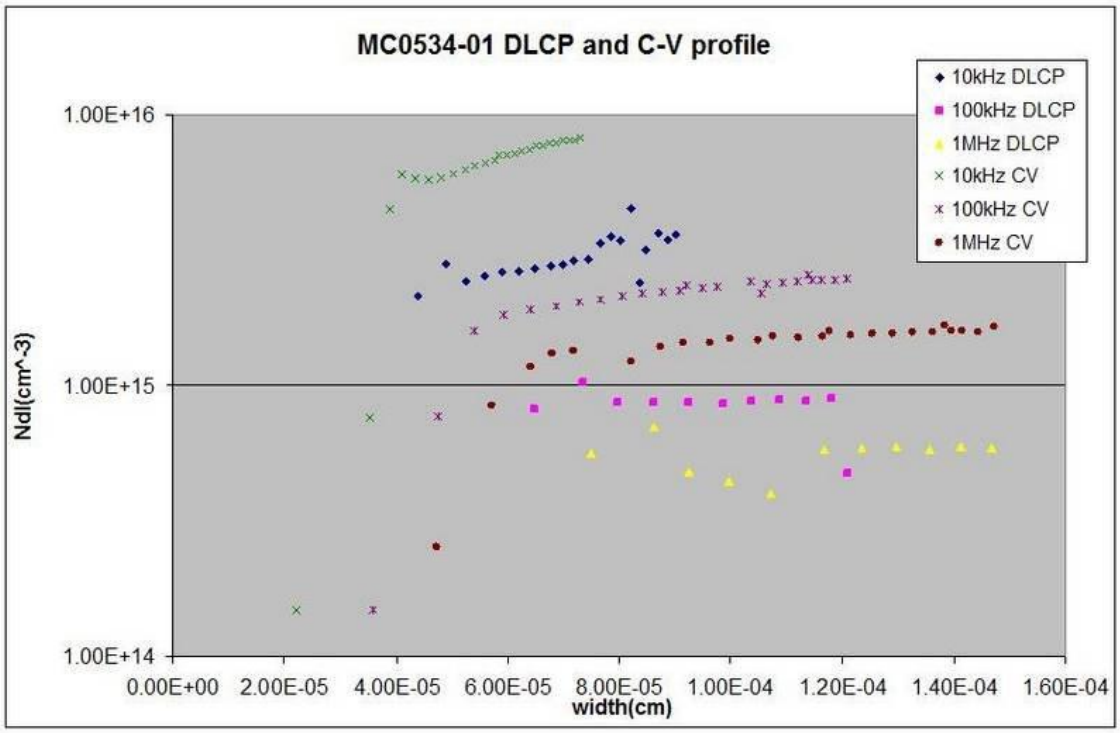

Fig: 5.8: The carrier concentrations as a function of spatial postion of a sample MC0534-01 with new etch at 10 kHz, 100 kHz, and 1 MHz. The carrier concentration increases with decreasing frequency. This suggests that defects were detected in both methods.

Chapter 6

IMPEDANCE SPECTROSCOPY

Admittance Spectroscopy (AS) and Impedance Spectroscopy (IS) are reciprocal functions, and they are essentially the same measurement. While admittance spectroscopy measurements are performed at reverse voltage bias to obtain the energy levels of the trap density of states, Impedance Spectroscopy measurements are performed in forward bias. This is where the injection and accumulation of minority carriers allows one to obtain parameters from which minority carrier lifetime is derived [19]. For both AS and IS measurement, a small ac voltage is applied across the completed solar cell with a fixed dc bias while capacitance and resistance (real and imaginary components of impedance) are measured at a range of frequencies. The IS-derived lifetime measured on a completed solar cell can be compared with the lifetime derived from the Sinton lifetime tester during fabrication.

6.1 Equivalent Circuit model of a solar cell

Impedance spectroscopy is used for solar cells that are modeled by an equivalent circuit to study the junction, interface, and contacts. In particular, the cells in this thesis are modeled by a parallel RC circuit (Fig. 6.1) discussed in chapter 4. From the impedance spectra (complex plane plot) of Z’ and Z’’ that are defined in eq. 6.1, parallel resistance, parallel capacitance, and the series resistance are obtained.

Equation 6.1 is the equivalent parallel circuit model. Z' is the real part, and Z" is the imaginary part of the impedance.

$$Z^*(\omega) = Z' + Z'' = R_s + \frac{R_p}{1+(\omega R_p C_p)^2} - j\frac{\omega C_p R_p^{\,2}}{1+(\omega R_p C_p)^2} \quad \left(\Omega \bullet cm^2\right) \qquad (6.1)$$

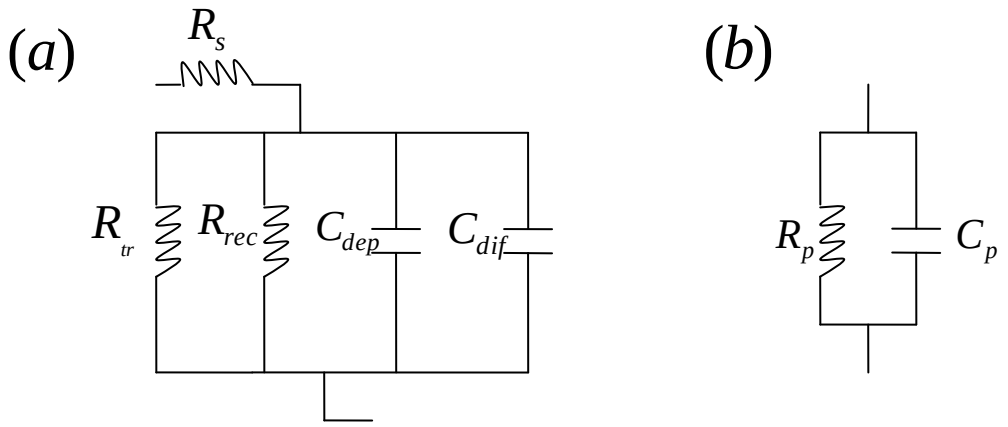

Fig. 6.1: Equivalent circuit model of a solar cell. Circuit (a) simplifies to (b) when C_{dep} and R_{tr} become insignificant.

R_{tr} = Transport resistance

R_s = Series resistance

R_{rec} = Recombination resistance

R_p = Total parallel resistance

C_{dep} = Depletion capacitance,

C_{dif} = Diffusion capacitance

C_p = Total parallel capacitance

6.1.1 Depletion and diffusion Capacitance

In figure 6.1, series resistance is very small for silicon heterojunction solar cells. It is composed of bulk Si wafer resistance and lateral resistance through the ITO/grids. It is around 1-2 ohms, and it can be neglected in the relation to the other components in the simplified equivalent circuit. The series resistance is obtained from dv/dj analysis in sec. 7.2.1. The two capacitances shown are depletion and diffusion capacitance. Since they are in parallel, their equivalent capacitance value is determined by the smaller of the two. Depletion capacitance is the same as junction capacitance discussed in chapter 5. Depletion capacitance dominates the total capacitance, C_p, at reverse bias and is defined in equation 6.2.

$$C_{dep} = \sqrt{\frac{\varepsilon_r \varepsilon_o q N_d}{2(\phi - V)}} \tag{6.2}$$

This equation is identical to eq.5.1 in chapter 5. For the Impedance spectroscopy method, diffusion capacitance dominates the total capacitance. At forward bias, the diffusion capacitance varies exponentially with voltage bias due to incremental injection and accumulation of minority carriers with small voltage changes, while the depletion capacitance varies only as the square root of V. A plot of capacitance as a function of voltage bias of a silicon calibration cell is shown in Fig. 6.2; the region below 0V is dominated by depletion capacitance while diffusion capacitance takes over at higher voltages. The diffusion capacitance, C_{dif}, is

$$C_{dif} = \frac{q^2 L_n n_o}{kT} e^{\frac{qV}{AkT}} \tag{6.3}$$

Where n_o is the minority carrier concentration, A is the ideality factor, and L is the diffusion length. Since $C_{dif} >> C_{dep}$ for the IS measurements, the depletion capacitance in Fig. 6.1 can be disregarded and $C_p \approx C_{dif}$ as shown in eq. 6.4.

$$C = C_{dep} + C_{dif} \tag{6.4}$$

The data in Fig.6.2 is plotted as $\frac{1}{C^2}$ vs. V (Fig. 6.3), and the linear slope is seen. This confirms that depletion capacitance (eq.6.2) exists. Also, the data in Fig. 6.2 is plotted as log C vs. Vand is shown in Fig. 6.4. Diffusion capacitance from eq. 6.3 is also a capacitance that is measured.

The transport resistance is the resistance due to the carrier transport in the material, and it becomes irrelevant since at long diffusion lengths, $R_{rec} >> R_{tr}$. The relation is shown in eq. 6.5. The thickness of the cell is W. For silicon solar cells, the bulk diffusion length is typically larger than the thickness with a float-zone wafer. The samples analyzed in this thesis either have a thickness of $145\mu m$ or $300\mu m$ with bulk diffusion lengths around $700\mu m$ on average, which is greater than the cell's thickness [19,5].

$$R_{tr} = \left(\frac{W}{L}\right)^2 R_{rec} \tag{6.5}$$

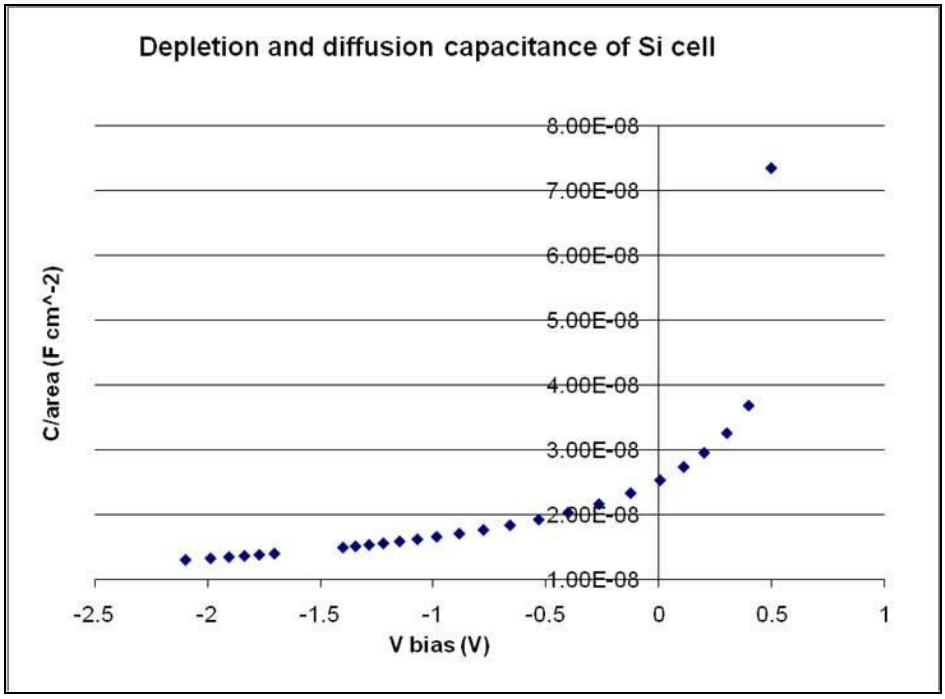

Fig. 6.2: depletion capacitance dominates in the reverse bias where the plot is linear, and diffusion capacitance is dominant in forward bias

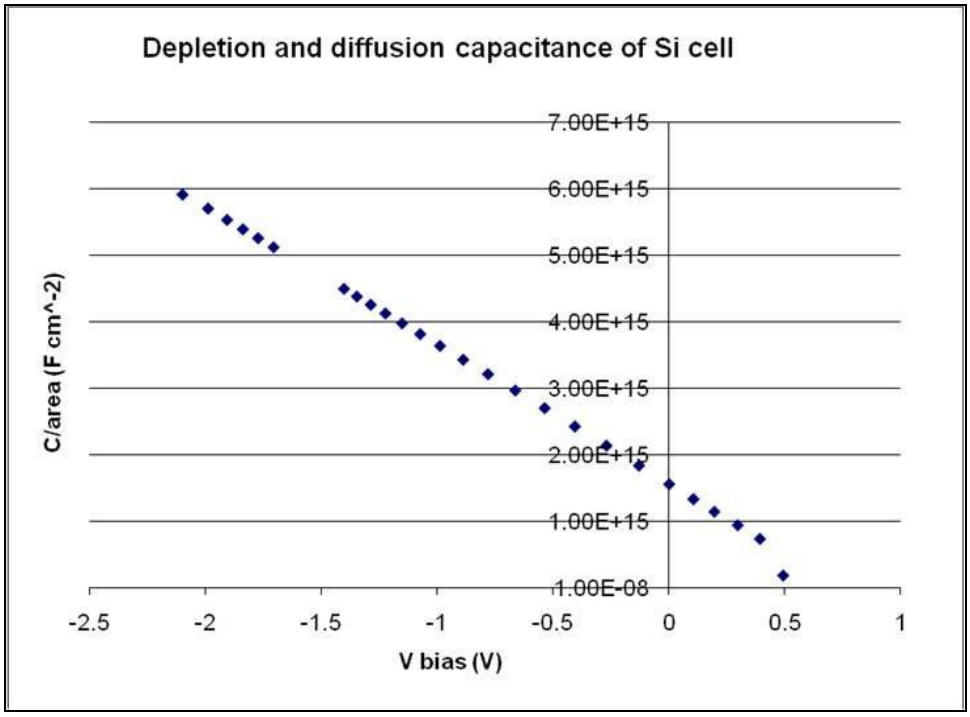

Fig. 6.3: Data from Fig. 6.2 is plotted as 1/C^2 vs. V. The plot is linear (eq. 6.2)

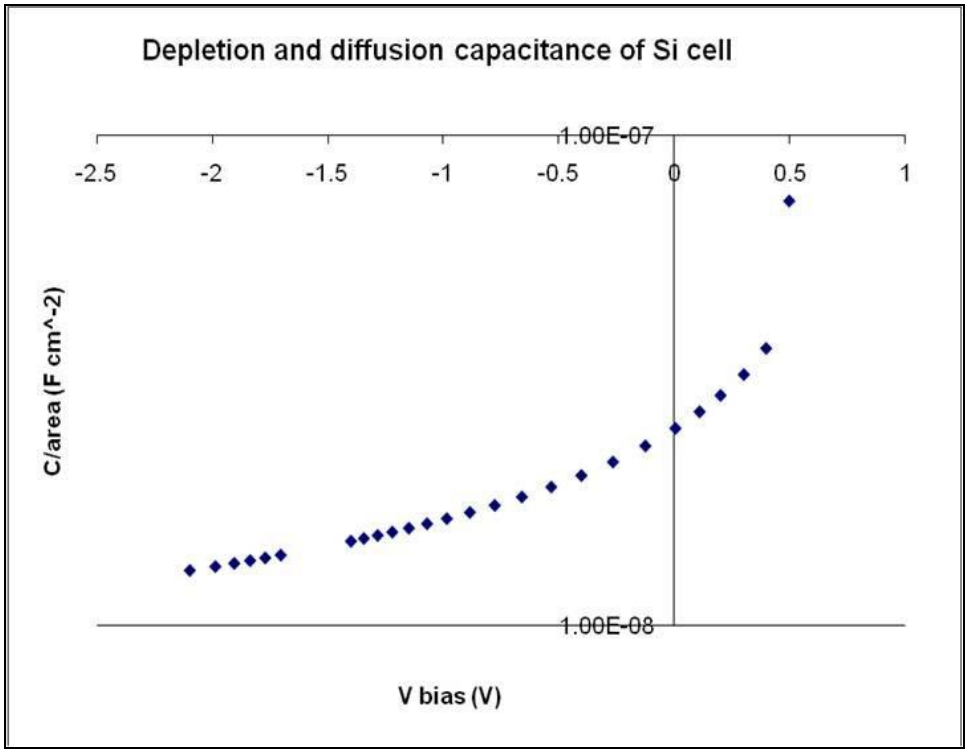

Fig. 6.4: Data from Fig. 6.2 repotted as log C vs. V. The plot is exponential (eq. 6.3)

The parallel resistance can be defined as eq. 6.6 where D_n is the diffusion constant [16]. Parallel capacitance is defined in eq. 6.3. The product of the parallel capacitance and parallel resistance is shown in eq. 6.7 after canceling some terms.

$$R_p = \frac{kT}{q}\left(\frac{L_n}{qD_n n_o}\right)\exp\left[-\frac{qV}{AkT}\right] \tag{6.6}$$

$$C_p R_p = \frac{D_n}{L_n{}^2} \tag{6.7}$$

$L = \sqrt{D\tau}$ so $C_p R_p = \tau$. This is defined as the response time in a circuit model, but in a solar cell, it is the recombination lifetime of the minority carriers.

6.2 Obtaining minority carrier lifetime

From the capacitance and conductance values from the IS measurements, the real (Z') and imaginary (Z") parts are calculated in the impedance equation (eq.6.1). The measured capacitance values are plugged in for C_p. R_p is calculated from the measured conductance, G_p. Note that Z' and Z" are not obtained directly from the impedance meter but are calculated from measured capacitance and resistance values assuming a certain circuit model.

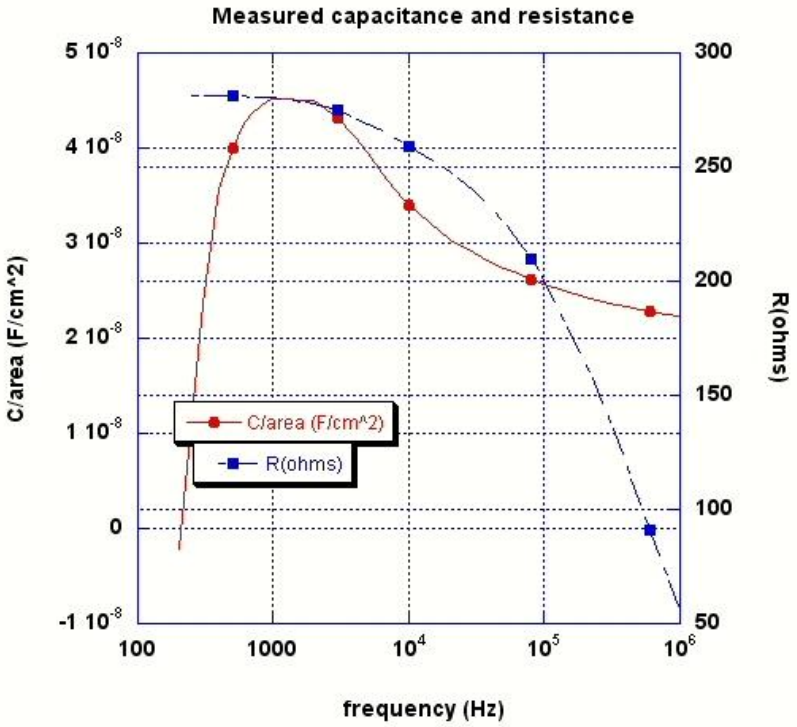

Fig. 6.5: Plot of C/area (red) and Resistance vs. frequency (blue). The lifetime is 11.2 us when both values are at a maximum.

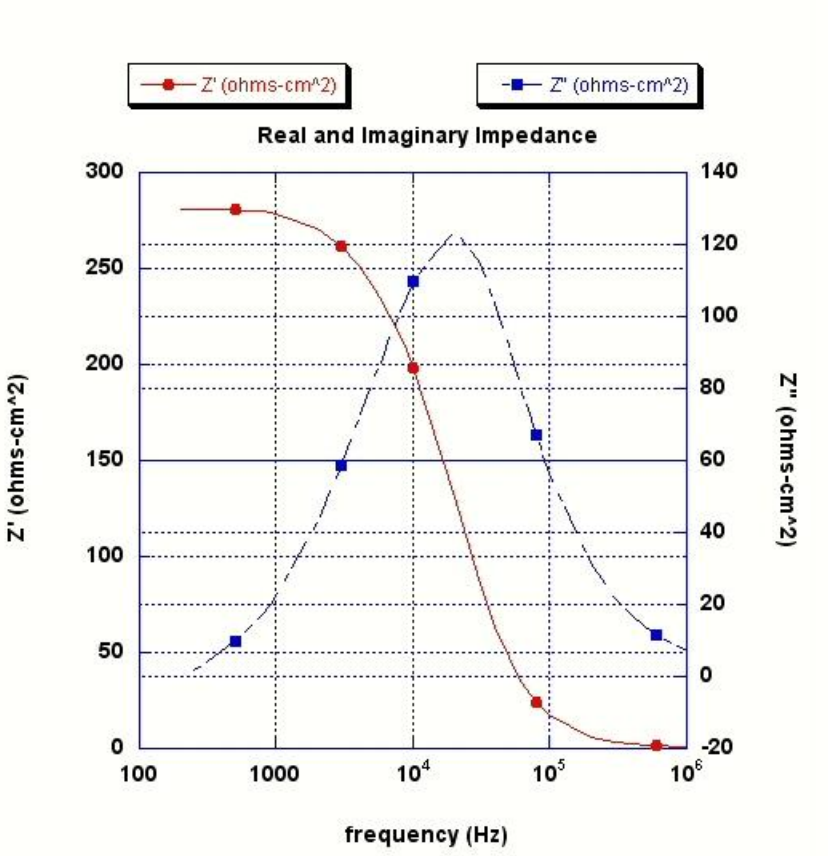

Fig. 6.6: Plot of Z'(in red) and Z"(in blue).vs. frequency. The maximum of Z'(around 280 ohms) is the value of parallel resistance and Z" is maximum at 120 ohms and is the maximum reactance value (see Fig. 6.7).

Measured parameters are plotted in Fig. 6.5. The graph shows the maximum capacitance and resistance values. Maximum lifetime of the carriers is obtained from their values and is about $11.2\mu s$. Figure 6.6 shows Z' and Z" which are calculated from eq. 6.1 using the measured capacitance and resistance, and their maximum values are 280 ohms and 120 ohms respectively.

An example of the impedance spectra is shown in Fig. 6.7. The impedance plot is also called a Nyquist plot. As the frequency increases, the semicircle points move from the far right (highest Z') to the left, approaching the origin. The horizontal displacement of the semicircle from the origin is the series resistance R_s. From the plot, the parallel resistance can be calculated, which is the diameter of the semicircle extrapolated to the Z' axis. The diffusion capacitance can be calculated from eq. 6.8, where $Z''_{\max}$ is the maximum reactance from the plot [11].

$$C_{dif} = \frac{1}{2\pi f Z''_{\max}} \tag{6.8}$$

The minority carrier lifetime is shown in eq. 6.9. The equation was derived earlier in sec. 6.1.1.

$$\tau = R_{rec} C_{dif} \approx R_p C_p \tag{6.9}$$

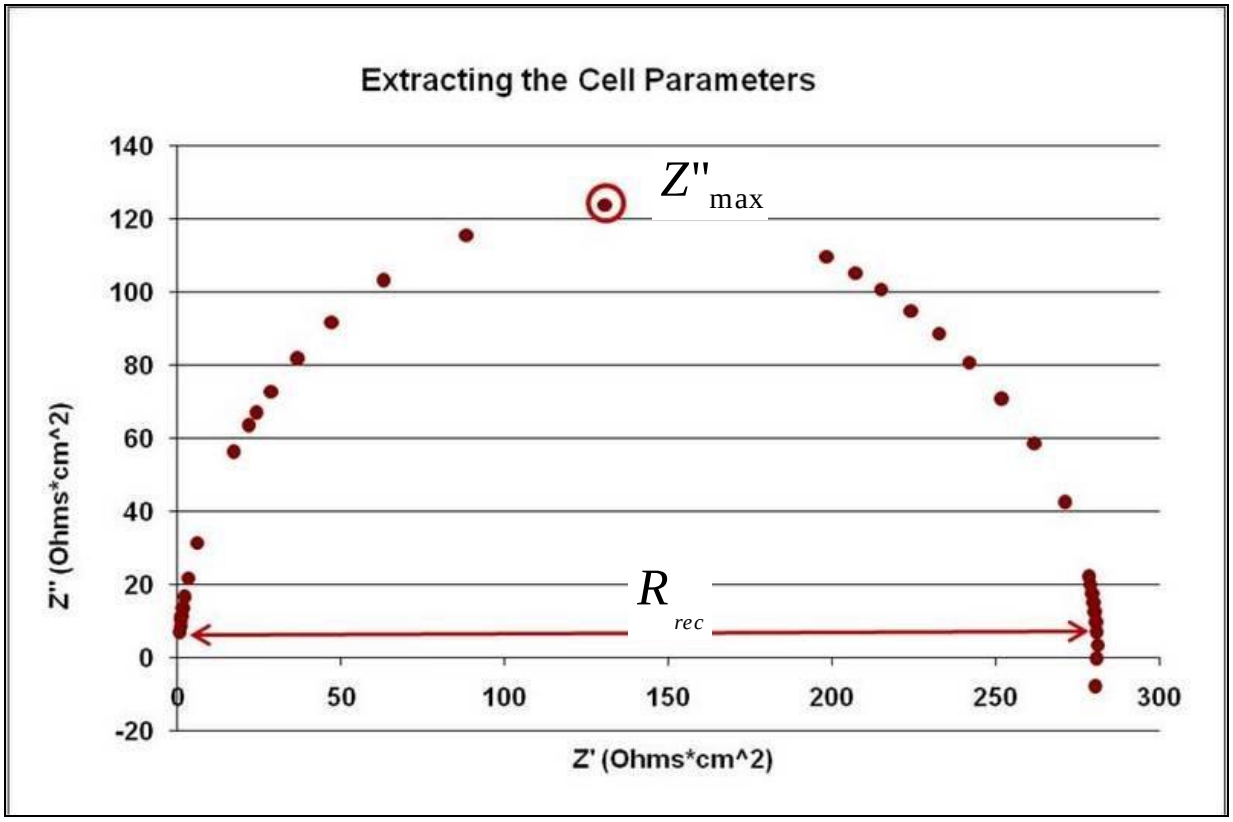

Fig: 6.7: Nyquist plot (complex plane plot) of a SHJ solar cell measured from 1MHz to 1kHz at +0.4V. The maximum reactance and recombination resistance are identified in the plot. The data at high frequency is essentially all real with Z'=285 ohms.

From this graph, we extract values of the lifetime of $17.9\mu s$, maximum reactance is about 120 ohms, and the parallel resistance is 280 ohms. These values agree quite well with values obtained from Fig. 6.5 and Fig. 6.6. This shows that the complex impedance plot in Fig. 6.7 is accurate and can be used to obtain minority carrier lifetime. At high frequency and a low frequency, the imaginary part Z" is essentially zero. A possible explanation is that the charge is 'frozen out' and cannot respond to signal at high frequencies, but all the charge can respond to the signal at the low frequency. Therefore, all the current measured is in-phase for both cases, and the

imaginary part is nearly zero. At maximum reactance, the out-of-phase current has the maximum imaginary value.

6.3 Applying Impedance Spectroscopy

6.3.1 Nyquist plots at various voltages

A complete semicircle can be obtained at 0.4V bias on most of our samples. As the voltage decreases, the diameter increases, and the plot looks less like a completed semicircle (Fig. 6.8). A larger diameter is due to a larger parallel resistance in the sample. At lower voltages, samples tend to have higher resistances. At reverse bias, the space charge region is depleted and only majority carriers can be measured. Although IS was measured at a range of voltages, only those at 0.4V forward bias consistently yielded nearly completed semicircles. Some become distorted and some failed to cross either origin. Therefore, in this thesis, only Nyquist plots at 0.4V bias are analyzed using the impedance spectroscopy method. Fig. 6.8 is magnified in Fig. 6.9 to show the plot near the origin. All three samples seem to converge at around 0.5 ohms on the x-intercept. This confirms that they all have the same series resistance

which was what we expected.

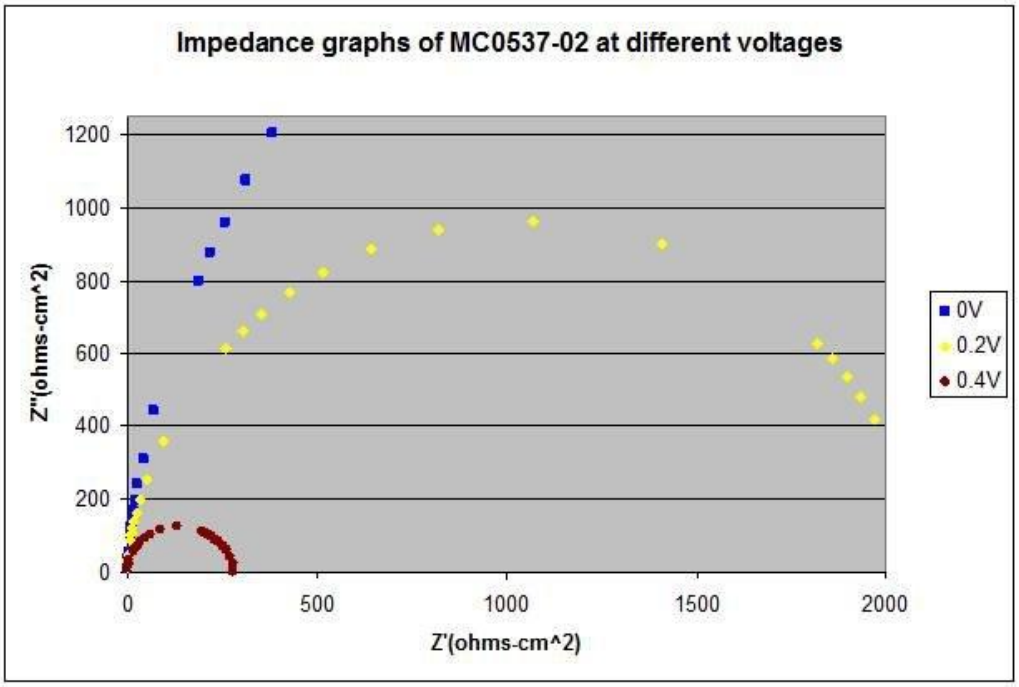

Fig. 6.8: Nyquist plots of MC0537-02 at 0V, 0.2V, and 0.4V. The diameter increases with decreasing voltage.

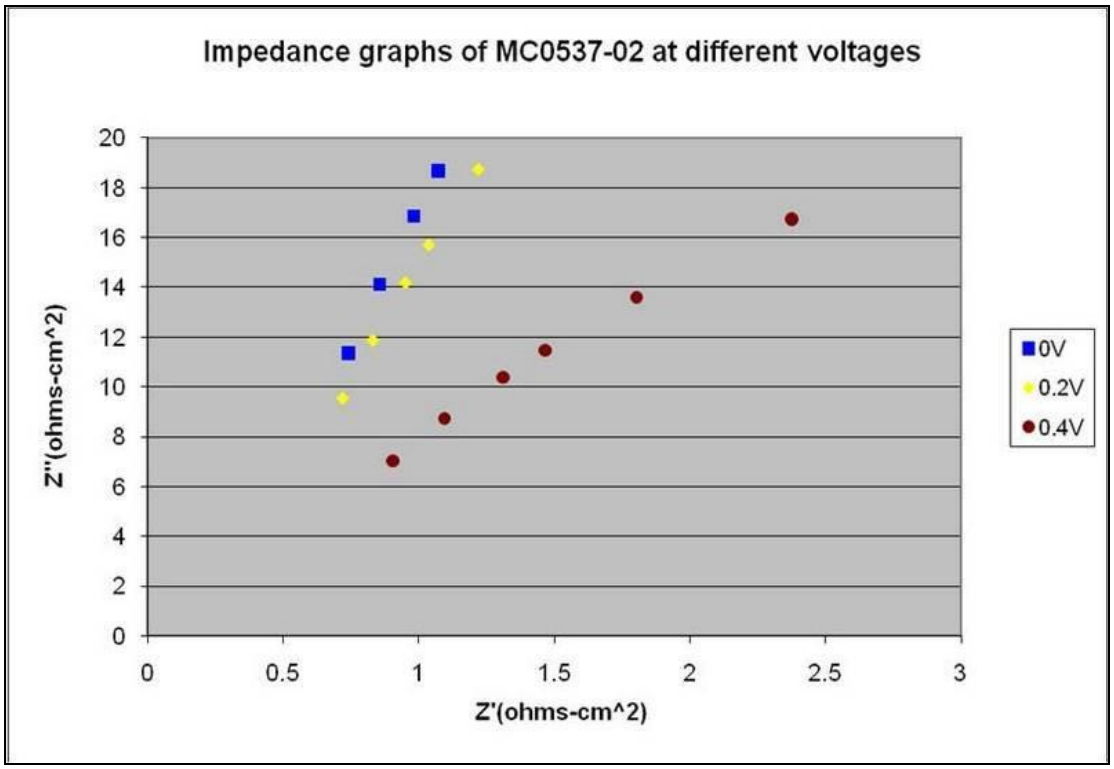

Fig. 6.9: Zoom in on Fig. 6.8. All samples have the same series resistance below 1 ohm as expected. This also confirms that series resistance is independent of voltage.

6.3.2 Lifetime of samples with and without piranha etch

As mentioned in chapter 5, the third group in table 6.1 has a sample without piranha etch (584-03), and a sample with piranha etch (584-06). The only difference between them is the fill factor. The excess defects and the open-circuit voltage are the same as discussed earlier. There is also no difference in lifetime from the IS method between the two samples. However, Fig.6.10 suggests that both samples are different since 584-03 sample has a larger semicircle. This is not the case. Sample 584-03 has a larger diameter and a larger peak than sample 584-06. The minority carrier lifetime is the product of the capacitance and resistance (eq. 6.7). The resistance is approximately

the diameter of the semicircle, so a larger diameter will increase the lifetime of a sample. However, the capacitance is inversely proportional to the maximum reactance (peak) of the semicircle. For a large peak value, the capacitance is small. Although 586-03 has a larger semicircle, it is the product RC that determines the lifetime. 584-03 has a lifetime of $44\mu s$ and 584-06 has a lifetime of $38\mu s$. So, the samples have approximately the same lifetime.

The lifetime measurements from the Sinton tester were lower by four times for both samples (584-03 and -06) compared to the lifetime from IS method, but both samples have similar Sinton lifetimes (table 6.1). 584-03 has a lifetime of $179\mu s$ and 584-06 has a lifetime of $121\mu s$. Although the values from both measurements differ by four times, they both show that the lifetime is the same for both samples. This shows that the IS method is consistent and can be used as a method to find out the lifetime of a completed solar cell. The differences between the two measurements are discussed in section 6.3.5.

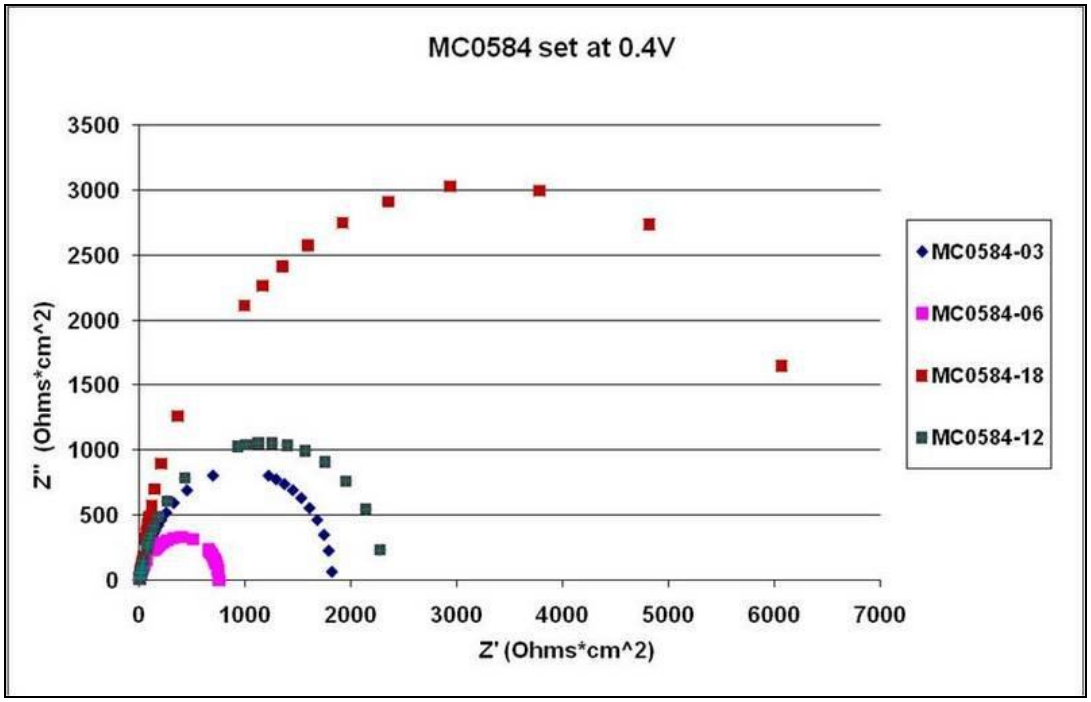

Fig. 6.10: Nyquist plots from four samples whose differences are listed in table 6.1. All data is obtained at 0.4V. Lifetime is calculated from the diameter(resistance) and the peak of the semicircle. The resistance is estimated for 584-18 since the semicircle does not reach the x-intercept. The error due to estimation is less than 2%.

6.3.3 Lifetime of samples with and without i-layers

IS was measured on samples which had a 5nm i-layer in the front between the n-Si wafer and p a-Si emitter, after the piranha etch (sample 584-12). The i-layer increased the open-circuit voltage by 49mV and increased the IS lifetime by $368\mu s$ or approximately by a factor of 4-8 compared to the sample without an i-layer (sample 584-06). Furthermore, with an i-layer in front and the back (sample 584-18), the lifetime shows another substantial increase. The results are shown in table 6.1 and Fig. 6.10. In addition, sample 584-12 has a lower lifetime compared with 584-18 for both methods.

Piece	Condition	$\tau(\mu s)$ (IS)	$\tau(\mu s)$ (Sinton)	V_{oc} (V)
MC0584-03	without piranha etch	179.24	43.78	0.605
MC0584-06	with piranha etch	121.00	37.98	0.589
MC0584-12	Piranha, front i-layer	489.12	269.50	0.638
MC0584-18	Piranha, both i-layers	796.61	343.77	0.670

Table 6.1: Samples 584-03, 584-06, 584-12, 584-18 and their lifetimes from IS method and the Sinton tester are shown.

6.3.4 Lifetime of samples with various i-layer thicknesses

The diameter (R_p) changes when the voltage bias is varied (Fig. 6.8). Figure 6.10 showed that R_p is strongly influenced by the device processing, including the presence of the front i-layer. It is well established in the literature and in our own results (see sec. 7.3) that the front i-layer thickness has a critical influence on the J-V performance. Figure 6.11 shows Nyquist plots for three devices whose only difference is their front i-layer thickness. All three samples shown in the figure have a 10nm i-layer in the back and had the same surface etching. Table 6.2 gives their lifetimes and open-circuit voltages. The parallel resistance increases when the i-layer thickness increases (Fig.6.11). The sample with 20nm i-layer thickness in the front has the

largest parallel resistance compared to samples with 5nm i-layer and no i-layer.

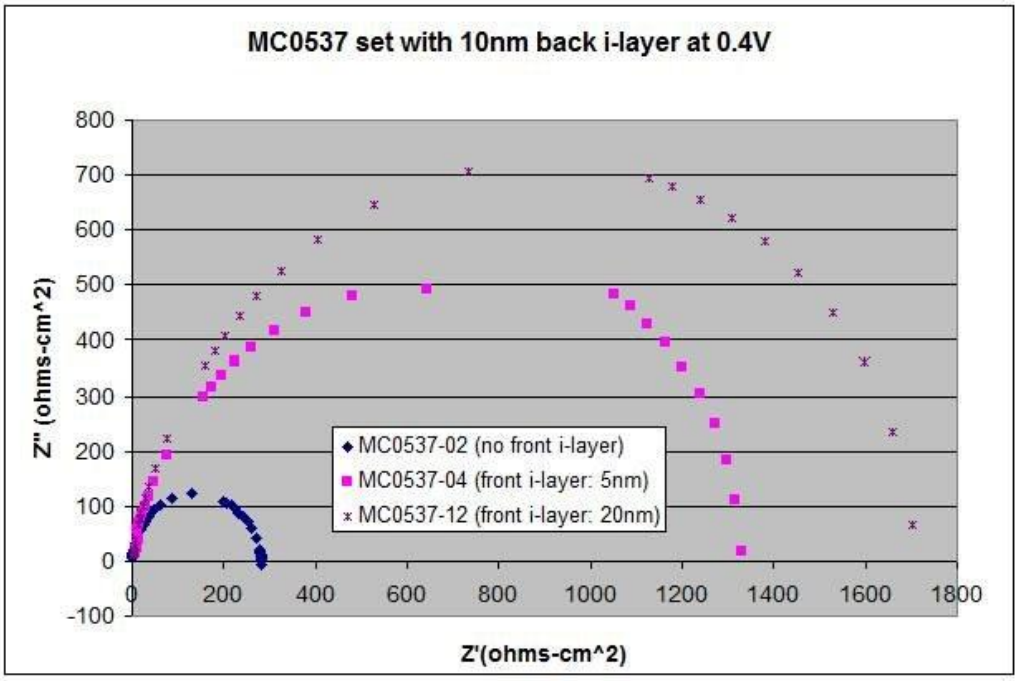

Fig. 6.11: Nyquist plots for samples with no i-layer, 5nm i-layer, and 20nm i-layer in the front.

It is possible that the thicker i-layer is the cause of an increased parallel resistance in the cell. In table 6.2, the lifetime from Impedance Spectroscopy method shows that 537-04 has the highest lifetime. However, the lifetime from Sinton tester is higher for 537-12. A possible explanation is that a solar cell with a 5nm i-layer in the front performs well compared to the other two samples. Fujiwara and Kondo [34] reported an i-layer of 40nm as the optimum thickness for SHJ solar cells. Other sources [27, 20] suggest that an i-layer around 10nm improves the cell performance while i-layers thicker than 10nm can lead to poor performance. The results in table 6.2 agree with their results. It is also likely that the sample, 537-12, degraded during the

deposition of the grids and contacts or even during impedance spectroscopy measurements. As the i-layer thickness increases, the open-circuit voltage tends to increase with lifetime.

Piece	Conditions	$\tau(\mu s)$ (IS)	$\tau(\mu s)$ (Sinton)	FF (%)	V_{oc} (V)
MC0537-02	no i-layer in front	17.90	34.15	68.5	0.554
MC0537-04	5nm i-layer in front	214.00	679.57	52.6	0.646
MC0537-12	20nm i-layer in front	191.24	1159.10	46.1	0.663

Table 6.2: All samples have a 10nm back i-layer. The i-layer thickness in the front varies. When the i-layer thickness increase, the lifetime tends to increase (but not always true), and the open-circuit voltage increases too.

J-V curves of these three samples are shown in 6.12. 537-02 has good diode behavior while 537-04 and 537-12 have poor s-shape curves (fill factors). It is more prominent in 537-12(table 6.2). This shows that what governs lifetime does not affect the carrier transport, and therefore the fill factor. Although the fill factors are poor, the samples have high lifetime.

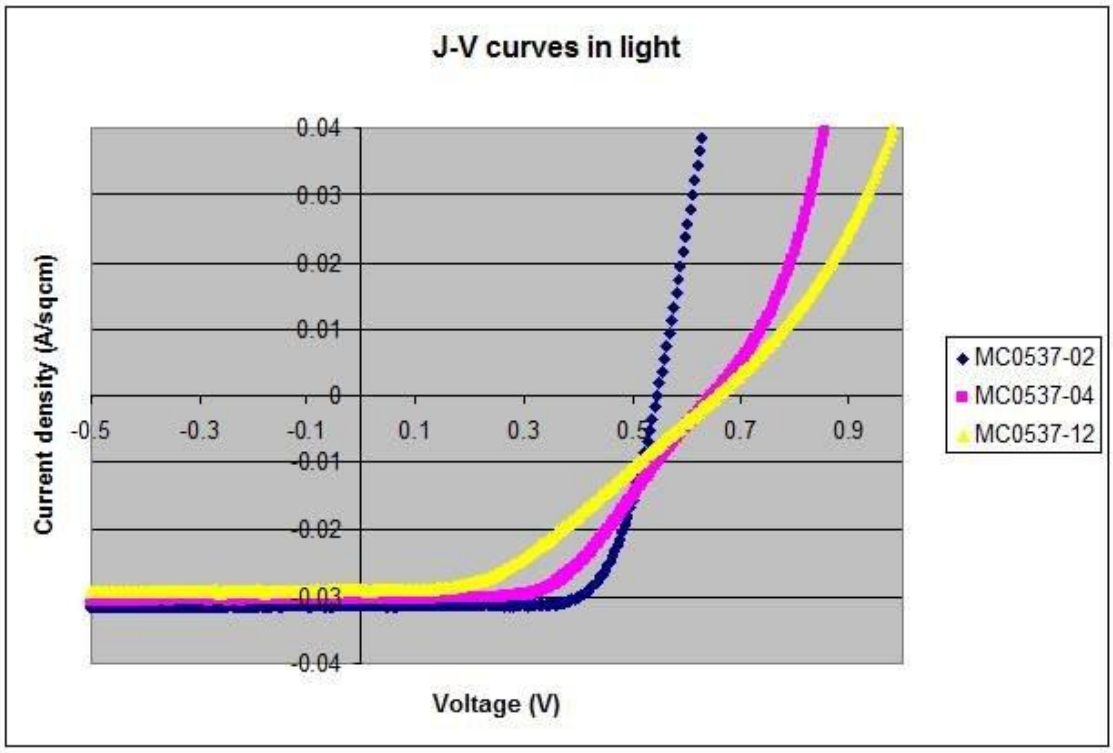

Fig. 6.12: J-V curves are shown for the three samples. The samples with s-shaped curves also have high lifetime and open-circuit voltage.

6.3.5 IS method lifetime vs. Sinton lifetime

In general, tables 6.1 and 6.2 show that the lifetime of samples with both i-layers or just the front i-layer have a higher lifetime compared to samples with just the back i-layer or no i-layers. This supports device modeling using Sentaurus that devices with only the back i-layer are not significantly better than those with no i-layer [2]. Rather, our results indicated that an i-layer in the back seems to improve the passivation of the cell only when the front i-layer is deposited as well.

Figure 6.13 is a plot of lifetime vs. open-circuit voltage of 32 samples with different processing and structures [27]. As the lifetime increases, the open-circuit

voltage increases. Also, Fig. 6.13 shows that the lifetimes from the IS method and the Sinton tester correlate well. The outlier circled at the top has an s-shaped curve, and the outliers at the bottom were processed differently and are at least six years old. Sinton measurements are performed immediately after depositions for the solar cell while IS measurements could have been made years later. This also explains noise in the data for IS lifetime. The samples could have degraded overtime. The correlation between both methods further supports that Impedance spectroscopy method is a reliable method to get lifetime on a completed solar cell. Moreover, this method can be compared with Sinton lifetime to note degradation or other issues in the cell.

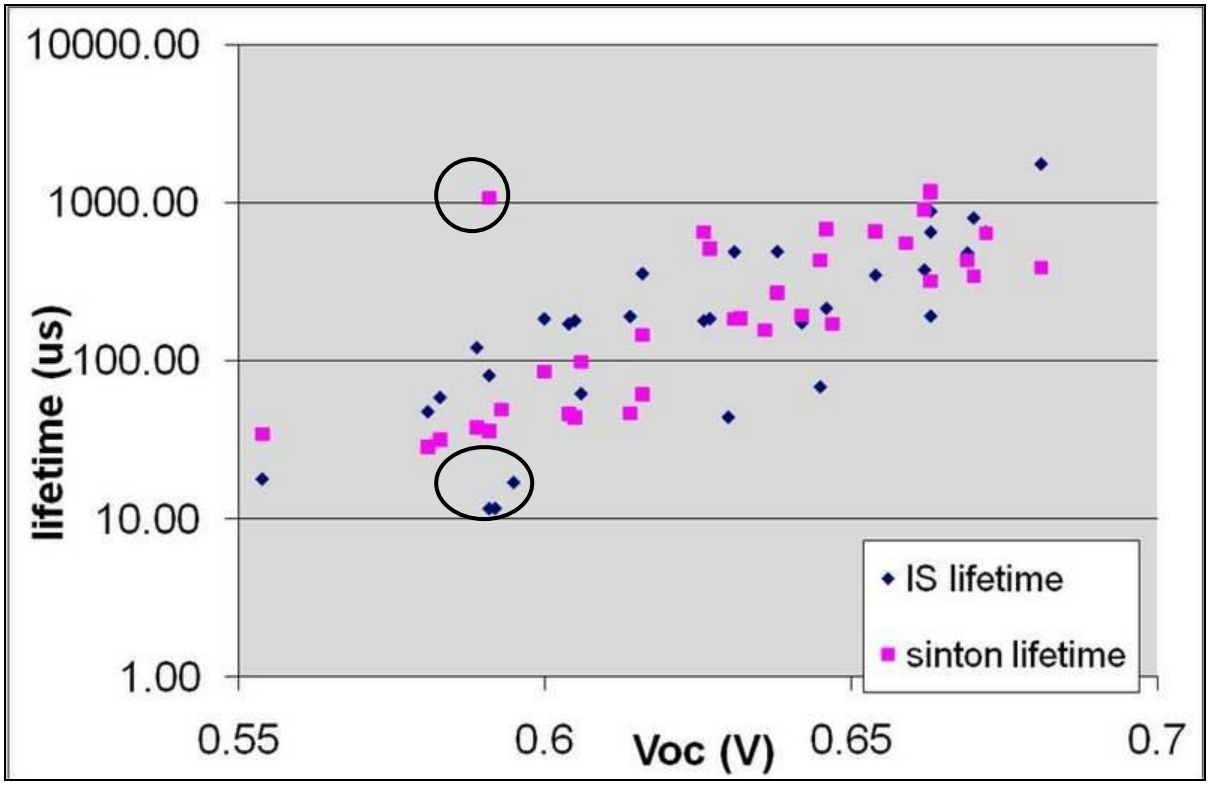

Fig. 6.13: The correlation between the lifetime from IS method and the lifetime from Sinton tester is shown [36].

Chapter 7

DIODE ANALYSIS

7.1 Parameters from current density-voltage curves

A solar cell is a diode that operates in light. The J-V (current density-voltage) curve of an illuminated solar cell is a dark diode curve (Fig. 7.1) that is displaced on the current axis due to current collection under illumination. The ideal diode J-V relation composed of only two elements, the photocurrent and the junction diode, can be written as:

$$J = J_0 \exp\left[\frac{qV}{AkT} - 1\right] - J_L \tag{7.1}$$

J = Current density

J_o = Saturation or diode current density

A = Ideality factor

k = Boltzmann's constant

J_L = Current density under illumination

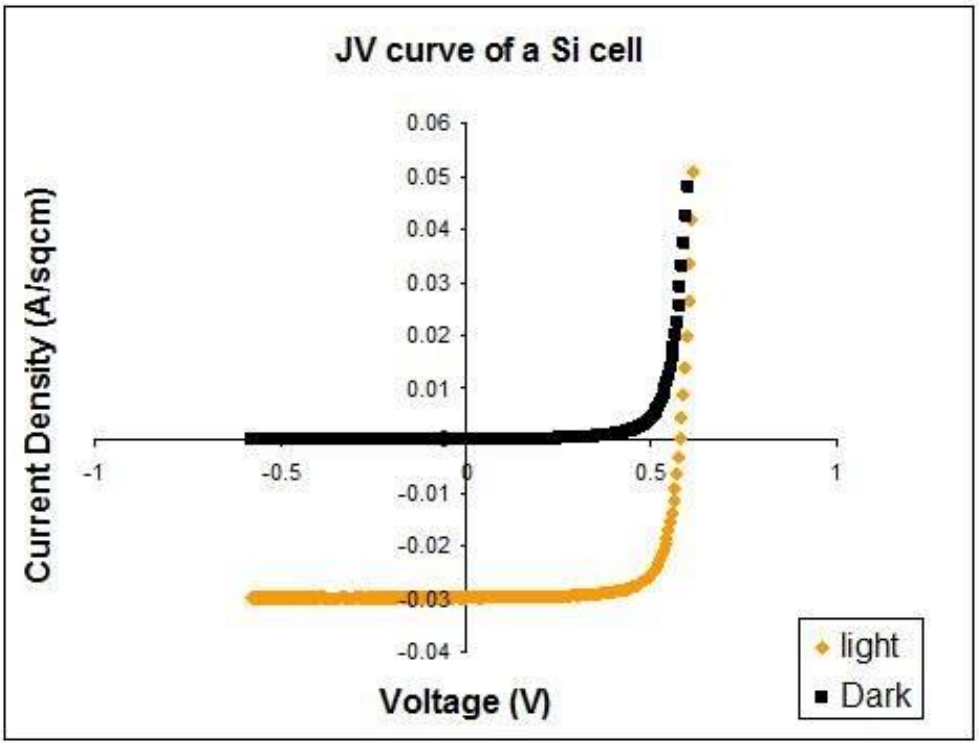

Fig. 7.1: JV curves in dark and under illumination. When illuminated, the light curve is displaced on the y-axis

The basic parameters obtained from a current density-voltage curve provide information on a cell's performance. They are short-circuit current (J_{sc}), open-circuit voltage (V_{oc}), fill factor (FF), efficiency (η), ideality factor (A), saturation current (J_0), and series resistance (R_s).

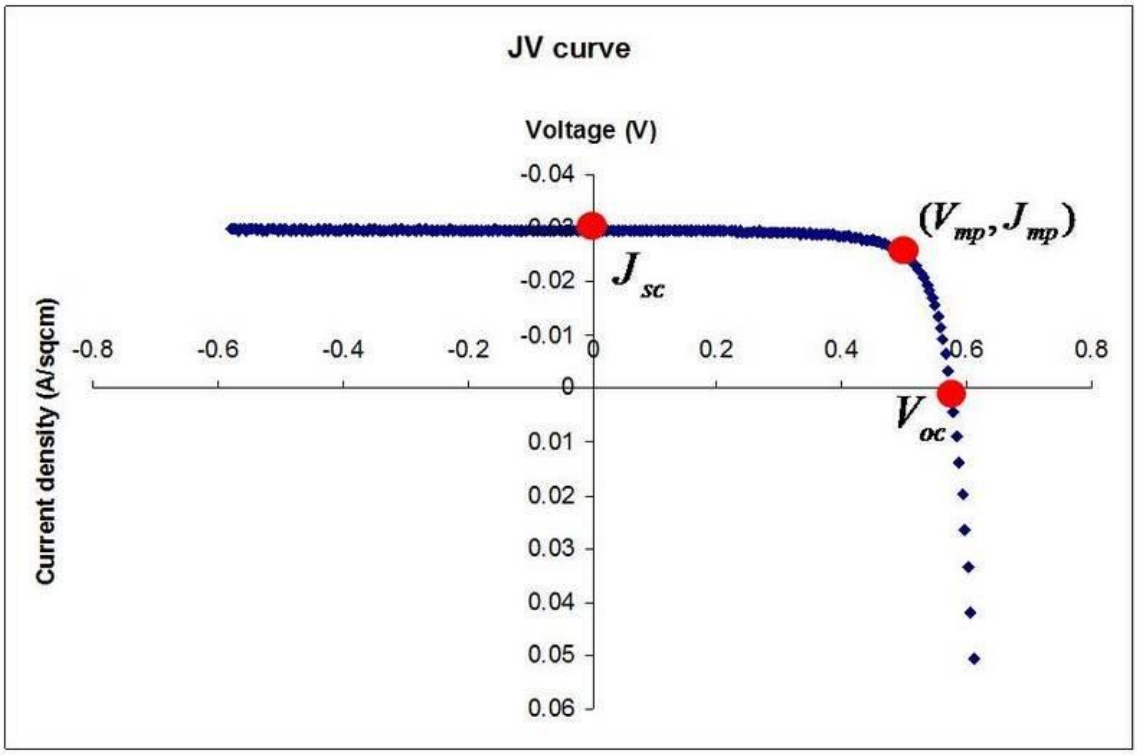

Fig. 7.2 : Short-circuit current, open-circuit voltage, and the maximum power point are shown.

Short-circuit current density is the measure of current per area when there is no voltage across the cell. Only generation and collection of current occurs at short-circuit current, therefore light-generated current (J_L) is approximately equal to J_{sc} and are interchanged often. The short-circuit current density is the maximum amount of current that can be drawn from the cell, assuming there are no field dependent collection losses as are common in thin film solar cells [6]. This is generally a good assumption for c-Si based devices.

Saturation current density, J_0 , is determines by the recombination in a solar cell. This quantity depends on temperature (eq. 7.2). Φ_b is the barrier height of the cell.

$$J_0 = J_{00} \exp\left(-\frac{\Phi_b}{AkT}\right) \tag{7.2}$$

Open-circuit voltage is the voltage measured when zero current flows through the device. It is inversely proportional to the log of the saturation current; saturation current density (eq. 7.2 & 7.3) depends on the amount of recombination in the solar cell. Therefore, V_{oc} is a measure of recombination. For high open-circuit voltage, a solar cell needs to have low bulk recombination as well as good passivation at the surface and interface.

$$V_{oc} = \frac{\Phi_b}{q} - \frac{AkT}{q} \ln\left(\frac{J_{00}}{J_L}\right) \tag{7.3}$$

Fill factor is a measure of the 'squareness' of the curve that represents the maximum power output from a cell. The output power at open-circuit voltage and at short-circuit current conditions is zero. The maximum output power can be obtained from a point in the curve where the product of the voltage and current give a maximum value. Ideally, this is where a module would be forced to operate by the maximum power point tracking circuitry.The voltage and current density at this point are represented as V_{mp} and J_{mp}respectively (Fig.7.2). Fill factor is defined as the maximum power from a solar cell to the product of J_{sc} andV_{oc}:

$$FF = \frac{V_{mp} J_{mp}}{V_{oc} J_{sc}} \tag{7.4}$$

Efficiency of a cell is the ratio of the energy out of the cell to the energy from the sun. The energy or power generated in the cell is given by the point in the curve where maximum power is generated to the power input from the sun [21].

$$\eta = \frac{J_{sc} V_{oc} FF}{P_{in}} \tag{7.5}$$

The ideality factor, A, determines the junction quality and the type of recombination. Usually, the ideality factor is between 1 and 2 for solar cells. Silicon heterojunction solar cells are typically reported to have an ideality factor between 1 and 1.2.

The series resistance of a Silicon heterojunction solar cell is small. It is often caused due to contact resistance between metal and silicon, the metal contacts, and the current transport in the emitter and absorber layers. The resistance values derived from the diode analysis agree well with the resistance values calculated using impedance spectroscopy [21,7,6,35].

7.2 Diode analysis

Open-circuit voltage, short-circuit current, fill factor, and efficiency are the basic parameters that can be obtained from the current density-voltage curves. There are other parameters that can be derived from the J-V curves measured under $100\frac{mW}{cm^2}$ illumination AM1.5 spectrum at $25^o C$. Before the data collected is analyzed

further, the parasitic losses are separated from the recombination losses. The parasitic losses are small in HIT solar cells. Two parasitic losses: shunt conductance and series resistance effects are subtracted from the raw data (see Fig. 6.1).

The ideal diode equation 7.1 can be written as eq. 7.6 by including the parasitic lumped elements of shunt conductance (G) term and resistance (R_s) as

$$J = J_0 \exp\left[\frac{q}{AkT}(V - R_s J)\right] + GV - J_L . \qquad (7.6)$$

7.2.1 Obtaining parameters

Using kaleidagraph or excel, the raw data is used to get the derivative of current with respect to voltage, $\frac{dJ}{dV}$. When V = 0 volts, $\frac{dJ}{dV}$ = G (see eq.7.6). If the shunt term is ohmic and the short-circuit current is constant, the $\frac{dJ}{dV}$ curve at the y-intercept is flat. The shunt value is subtracted from the current, and the corrected current values are designated as the new current, J'.

$$J' = J - VG \qquad (7.7)$$

The shunt conductance is now accounted for.

Next, a plot of $\frac{dV}{dJ}$ vs. $\frac{1}{J'}$ gives a linear plot with equation:

$$\frac{dV}{dJ} = R_s + \frac{AkT}{q}\left(\frac{1}{J'}\right) \qquad (7.8)$$

From this equation, the series resistance and the ideality factor can be obtained. The effect of series resistance is then subtracted:

$$V' = V - R_s J' \qquad (7.9)$$

This new voltage, V', and the new current, J', are the actual voltage across and current through the pn junction. When they are plotted in a semi log plot, and the saturation current and the ideality factor are obtained from the high current region. The two ideality factors derived from the different equations are compared and should be approximately the same [6].

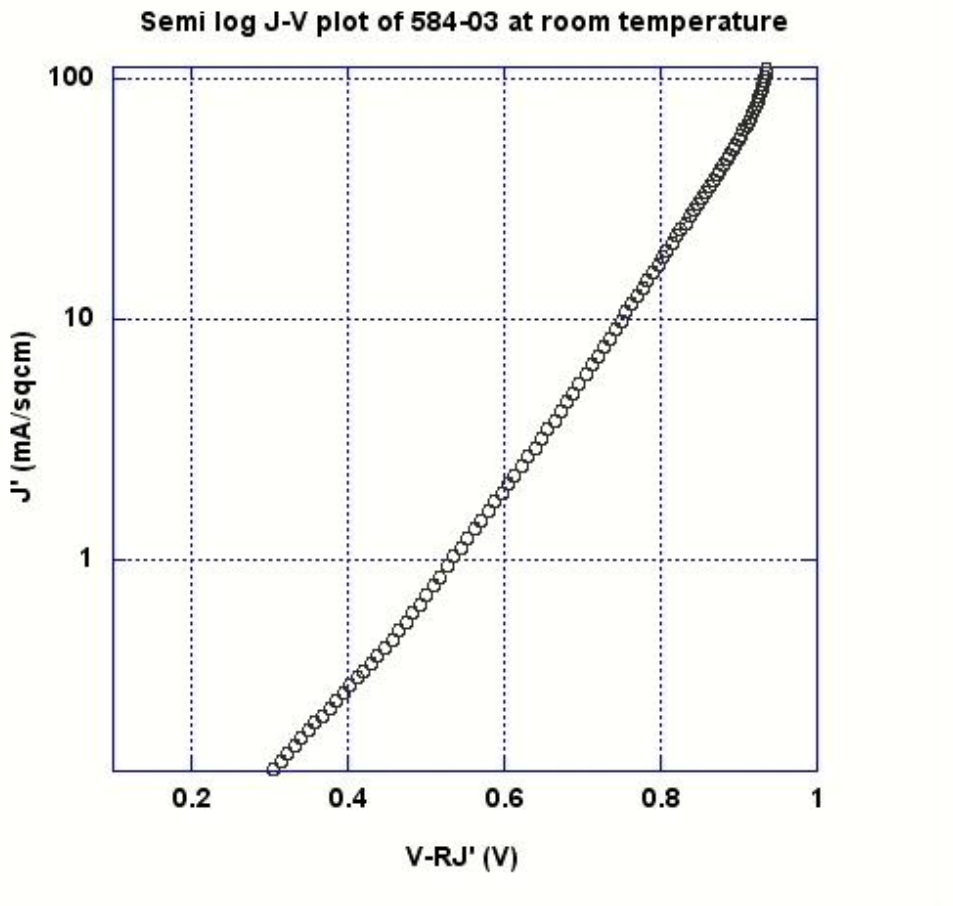

Fig. 7.3: Semi log J-V plot of MC0584-03 sample at room temperature. The fitting region is 1 and 100mA/sqcm

7.3 Results for current density -voltage measurements

In table 7.1, there is no obvious difference in structure, the excess defects or the lifetime between 584-03 and 584-06. The structure, cleaning procedure (except the piranha etch), and manufacturing procedures were also the same. The major difference is that one sample had a piranha etch with a high fill factor, and the other sample that

did not have piranha etch has low fill factor. Since the difference is only in the fill factor, we deduce that during the piranha etch, a layer was removed. The removal of this layer changed the band alignment and improved the fill factor. The ideality factor is greater than 2 and the saturation current is high for 584-03, and both values suggest that this piece's performance is poor [22].

Sample	Conditions	V_{oc} (V)	FF (%)	A factor	Series Resistance (ohms)	Saturation Current (mA/sqcm)	N_{ex} (cm^{-3})	Lifetime (μs) Sinton
MC0584-03	No piranha, no i-layers	0.605	33.1	4.72	2.20	4.29E-3	2.86E+16	43.78
MC0584-06	Piranha, no i-layers	0.589	78.9	0.99	1.55	2.06E-6	5.23E+16	37.98
MC0584-10	Piranha, front i-layer	0.631	81.2	1.05	0.94	5.36E-9	3.07E+16	183.19
MC0584-19	Piranha, both i-layers	0.647	73.5	1.16	3.47	2.21E-8	3.85E+15	171.32
MC0584-24	Piranha, both i-layers	0.636	44.7	3.56	5.16	5.66E-3	3.28E+15	156.76

Table 7.1: The open-circuit voltage, fill factor, ideality factor, series resistance, saturation current, excess defect density, and the lifetime of the samples are shown.

The ideality factor of 584-06 and 584-10 is about 1 while it is 1.2 for 584-19. It was reported that interface recombination can occurs when the ideality factor is 1, and A = 1.2 is noted for samples that perform well. The saturation current is also low suggesting that the device is good. Ideality factor of 1 can also be due to radiative recombination. This is often the only recombination included in some modeling. To know which recombination is occurring, $V_{oc} - T$ analysis is needed [23].

The open-circuit voltage improves by 40mV when an i-layer is added to the front (584-10); however, the excess defects did not change and the ideality factor is

still 1. So, it is possible that the front i-layer only changed the band alignment and passivated the front interface. But, interface recombination is still occurring in the back interface. When the front and back i-layers were added, the open-circuit voltage improves by about another 20mV, and the excess defects decrease by an order. This suggests that the back layer reduced the recombination in the back. Ideality factor of about 1.2 further supports that the interface recombination in the cell is reduced. Good ideality factors are usually accompanied with low saturation current (table 7.1), and it is a good indication the recombination is low and that the sample is a good device.

In conclusion, the i-layer in the front with our structure changes the band alignment while the i-layer in the back reduces the interface recombination. Moreover, i-layers on both sides improves the cell performance overall [24]. The series resistance values in table 7.1 are slightly higher than anticipated. This is usually due to problems relating to the fit in the plot.

7.4 Results for temperature dependent current density-voltage

Temperature dependent current density-voltage measurements in the dark can give the barrier height, Φ_b , that the carriers have to overcome to be collected. Taguchi et al [1] proposed recombination by multitunneling capture emission model for low voltages (0.1<V<0.4V), and by diffusion current mechanism at higher voltages for (p) a-Si/ (n) c-Si cell structure in the semi log J-V plot. Marsal et al [25] demonstrated similar results for cell structure (n) a-Si/ (p) c-Si. Fitting the data at higher voltages with an exponential equation (eq. 7.6) gives the ideality factor and

saturation current as discussed in section 7.2. The A factor and J_0 are obtained from analysis of the J-V data, including the parasitic effect of R and G, at various temperatures from 15^oC to 95^oC in steps of 10^oC. An Arrhenius semi log plot of J_0 vs. $\frac{1}{T}$ (Fig. 7.4) gives an activation energy which we equate with the barrier height.

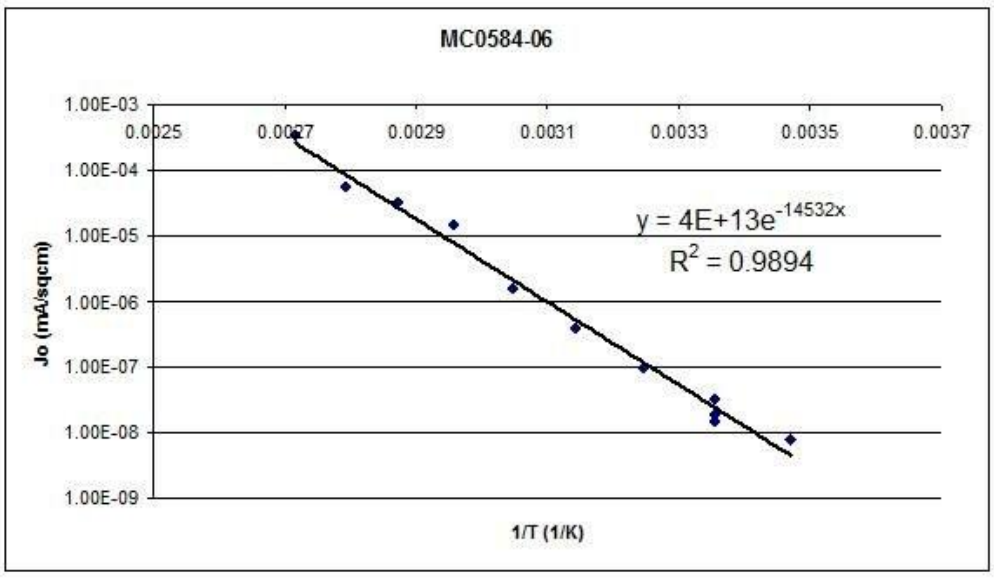

Fig. 7.4: Arrhenius semi log plot of J_0 vs. $\frac{1}{T}$ for MC0584-06 (See Table 7.1). Barrier height of 1.25eV is obtained from the slope of the exponential equation.

The magnitude of barrier height can determine if recombination is occurring in the neutral bulk or at the interface. If the barrier height is approximately equal to the band gap of the crystalline silicon with A=1.2, neutral bulk and space charge region recombination dominate. However, if the barrier height is less than the band gap and A=1, then interface recombination dominates (table 7.2)[1,23,26,27]

The ideality factor should not vary significantly with the temperature is varied because material properties such as defect distribution in energy are independent of temperature applied. Accordingly, we observe that for most of our samples, the average of the ideality factors at all temperatures matches the ideality factor at room temperature. Sample 584-24 has temperature dependent ideality factor, and it will be discussed later (see tables 7.1 & 7.2).

Sample	Avg. A factor	Φ_b (eV) JV-T method	Φ_b (eV) (Voc-T method)
MC0584-03	3.21	0.36	1.11
MC0584-06	1.02	1.25	1.31
MC0584-10	1.04	1.28	1.32
MC0584-19	1.14	1.04	1.33
MC0584-24	3.63	0.16	1.29

Table 7.2: The average ideality factor and the barrier height from both methods are shown. The barrier heights vary significantly. Table 7.1 shows that samples 584-03 and 584-24 had significantly poorer FF than the others.

In addition to the high ideality factor and low fill factor leading to poor cell performance, 584-03 and 584-24 also have an s-shaped current density-voltage curve. The samples with poor performance (584-03 and 584-24) have very low activation energy compared to the other samples. Recombination at the interface or defect sites at the valence band offset have been proposed by Jensen et al. (27) as the cause of high ideality factors and low barrier height such as seen for these pieces.

In addition to the low barrier height, the ideality factor is temperature dependent for 584-24. The ideality factor decreases with increasing temperature and

the dependence is linear as seen in Fig. 7.5. Several groups reported tunneling in the case of a temperature dependent ideality factor. Hegedus and Shafarman [6] explain that the change in the ideality factor depends on energies of the deep defects that act as traps. The temperature dependence of the A factor can be due to the distribution of traps or tunneling. Jensen et al. [27] suggested a recombination in the SCR due to tunneling into defect states. The high electric field might be due to charged defects that function as dislocations or grain boundaries leading to tunneling. Furthermore, this would lower the open-circuit voltage and the ideality factors could be greater than 2. Increased amounts of Boron contamination leading to macrostructural defects can also lead to tunneling mechanism in the device [29].

The barrier height of the other pieces in the table is similar. The sample with an A factor of 1.2 has a barrier height of 1.04eV. This value is close to the band gap of crystalline silicon. Diffusion in the c-Si space-charge region was suggested as the reason that the barrier height is equal to the band gap of crystalline silicon, which is about 1.12eV. Samples 584-06 and 584-10 have similar barrier height and ideality factor. Interface recombination (because A=1) could have lead to a barrier height that is not equal to 1.12eV.

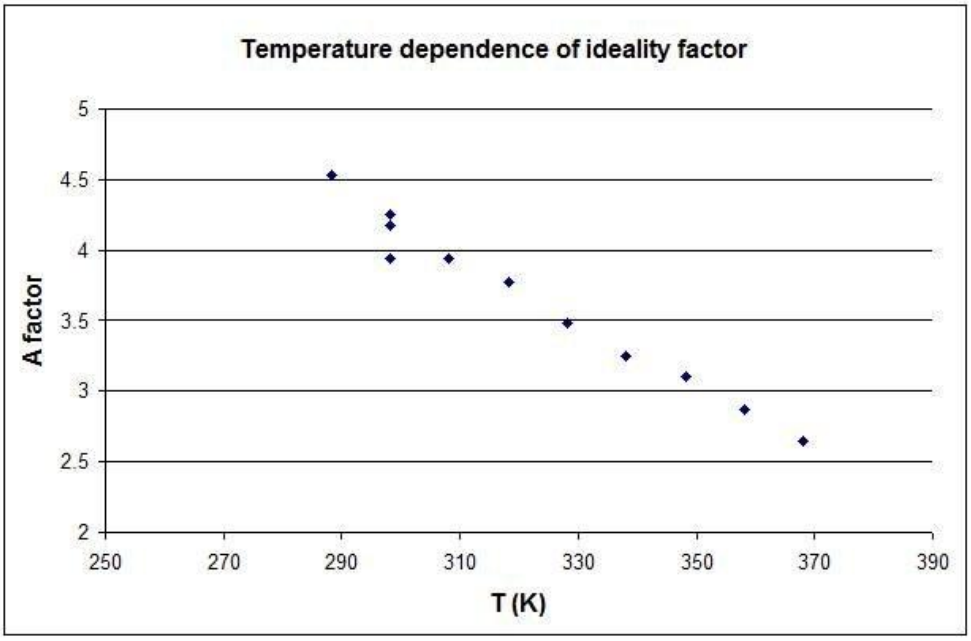

Fig. 7.5: A linear temperature dependence of A factor for sample 584-24 is clear.

7.5 Open-circuit voltage –temperature results

In table 7.2, the activation energy (barrier height) of the samples from the open-circuit voltage – Temperature method is shown. The barrier height is obtained from the y-intercept of the graph (eq. 7.3). A plot of V_{oc} vs. T of 584-06 (FF=79%) and 584-24 (FF=45%) are shown in Fig. 7.6. For many types of heterojunction solar cells, a plot of V_{oc} vs. T lead to linear extrapolation at T = 0K of a value equal to the absorber layer band gap [94]. When the barrier height obtained from V_{oc} vs. T is equal to the band gap of absorber layer (c-Si), Shockley-Read-Hall (SRH) recombination is reported as the dominating recombination in the absorber layer. However, other recombination mechanisms are reported as the dominating mechanisms when the

barrier height is not equal to the band gap [28]. Note that the two devices in this plot had significantly different FF and hence shape of their J-V curves: one had s-shaped curve and other a nearly ideal curve. But since V_{oc} is obtained where there is no current flow, the influence of poor contacts or high resistance is negligible. This suggests that the mechanism which causes the distorted and low FF is due to photocurrent collection, not fundamental recombination or series resistance.

Our barrier height for the two methods in Table 7.2 are in close agreement on two samples, moderate agreement on the third, and do not agree well at all for the two devices having distorted J-V curves leading to s-curves and high A factors. The samples that have extremely low barrier height from JV-T method(s-curves) have barrier heights close to the band gap for V_{oc}- T. Ideally, both methods are supposed to agree since saturation current and open-circuit voltage are inversely related, and they both determine the recombination in a cell (eq. 7.3). However, the consistency between both methods is observed for all samples. Therefore, experimental error is not the problem. The recombination mechanism suggested from the barrier height of each method is contradictory for each sample. Further work is needed on understanding what we are measuring for each method.

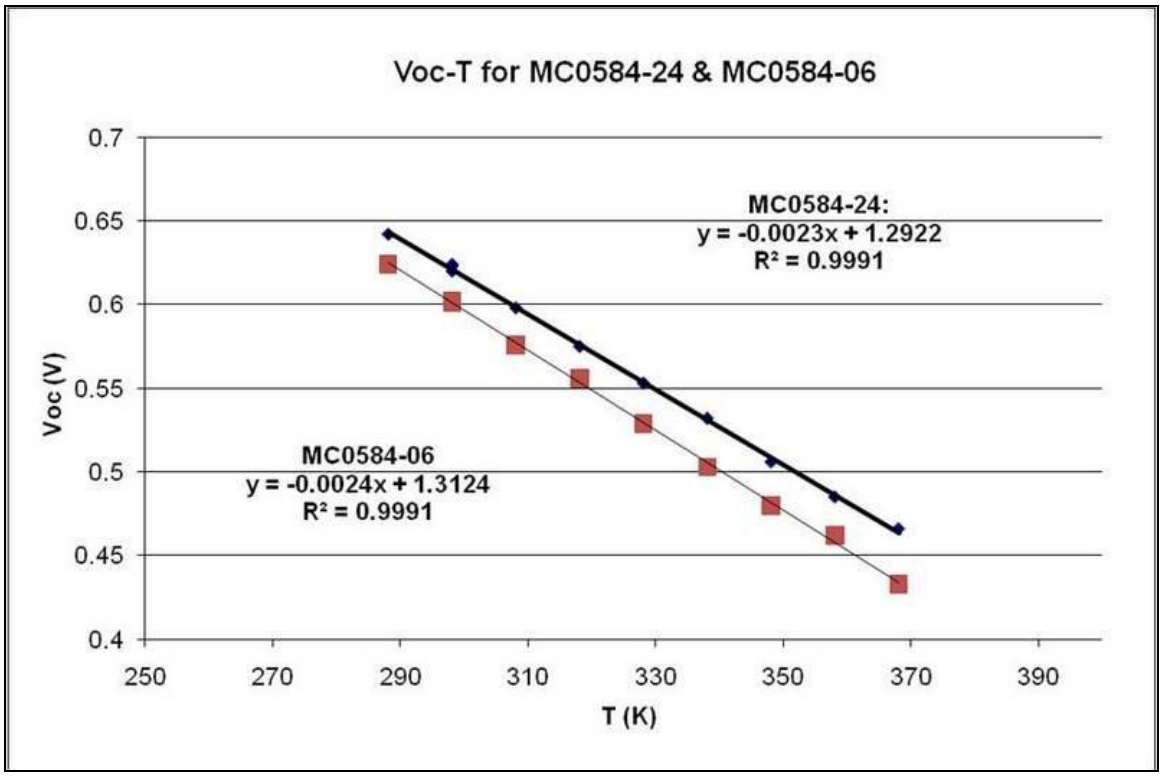

Fig. 7.6: Voc vs. T plot. The barrier height is 1.29eV for 584-24 taken from the y-intercept in the graph. The barrier height is 1.31eV for 584-06(well-behaved device). They have about the same barrier height, yet one of the samples has good performance compared to the other.

Chapter 8

INTERNAL PHOTOEMMISION SPECTROSCOPY

8.1 Internal Photoemission method

The valence and conduction band offsets in Silicon heterojunction solar cells are fundamental parameters which can have an effect on each of the device parameters by influencing the carrier recombination (V_{oc} and J_{sc}), the photocarrier collection (FF), and the built-in voltage (ϕ_i). Therefore, a proper method is needed to measure the offsets. Internal Photoemission (IPE) has been used for c-Si wafer-based solar cells to find the band offsets [30]. While C-V and J-V measurements can be used to find the band offsets, they are affected by the defects in the solar cell. The IPE method is immune to the defects; therefore, it is not influenced by recombination losses since the carriers generated in c-Si side can be collected (Fig.8.1) [19].

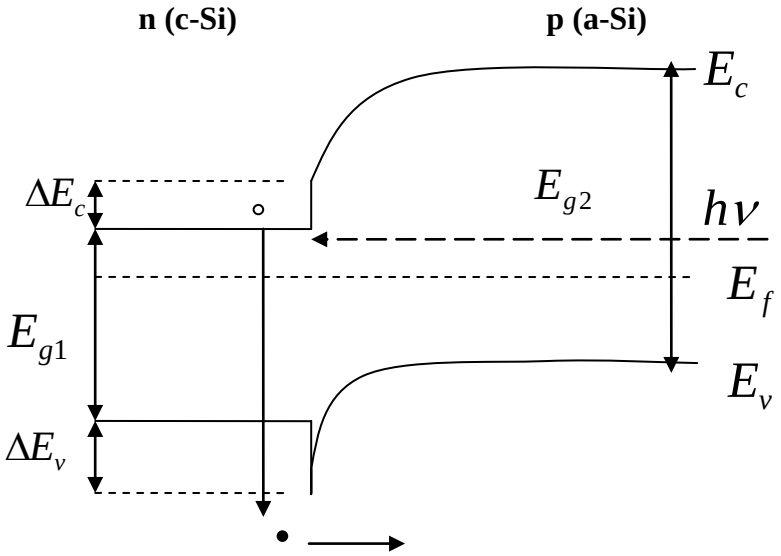

Fig. 8.1: The internal photoemission process is shown. Light is incident on the cell through the wide bandgap a-Si p-layer heterojunction window, and the electron-hole pairs are generated in the narrow bandgap (n-type c-Si). Note that band diagram of c-Si is not complete.

8.1.1 Collection process due to IPE

Photons are transmitted through the (p) a-Si side at only long wavelengths and absorbed in the c-Si where photons with energy closer to the band gap of c-Si wafer are collected. When the electron-hole pair are generated, carriers that have enough energy to overcome the band-offsets and crossover to the wide band gap side (fig 8.1). The basic theory predicts a square dependence for a direct band gap due to parabolic energy bands [16,32]. It has been shown by Kane [32] that the yield for an indirect band gap with imperfect surface will have 5/2 dependence. The yield, Y, of photoemission current for an indirect band gap is given by:

$$Y \propto (E - E_t)^{\frac{5}{2}} \tag{8.1}$$

Where, $E = h\nu$ is the incident photon energy, and E_t is the threshold energy the minority carriers (holes for n-type c-Si) have to overcome for current collection. A plot of $Y^{2/5}$ with respect to the photon energy will have a flat region below the threshold energy when carriers cannot overcome the barrier. Above the threshold energy, a linear region is observed in the plot of $Y^{2/5}$ vs. Energy. As the photon energy increases, an increasing number of carriers overcome the barrier and crossover to the a-Si side to be collected (Fig.8.2). An extrapolation to the x-intercept gives an approximate value for E_t [32,33].

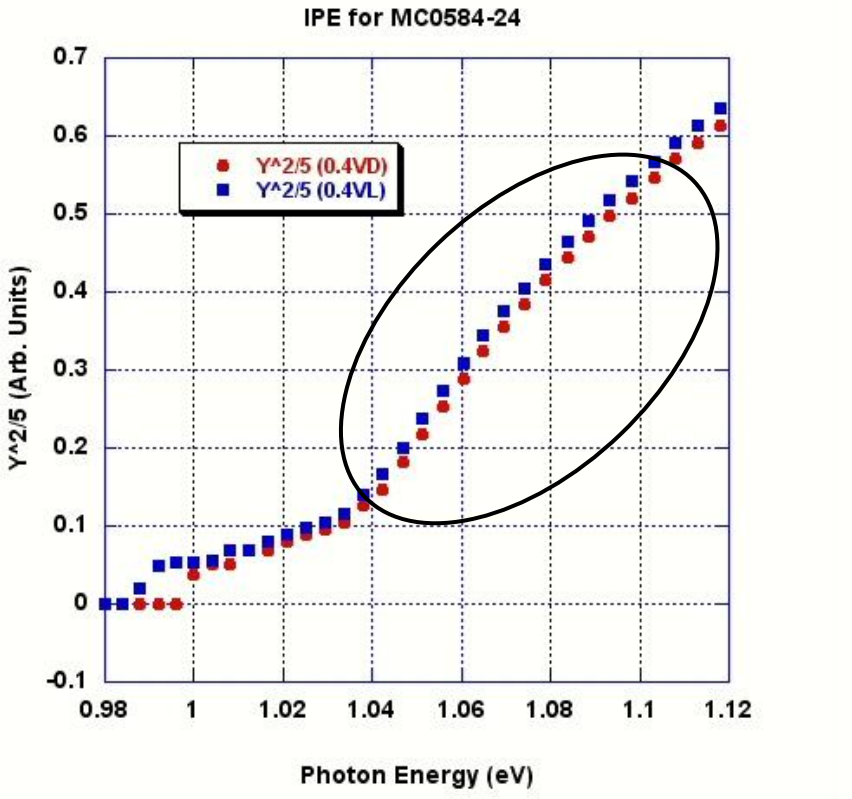

Fig. 8.2: Y^2/5 vs. photon energy plot is shown. The threshold energy is obtained by extrapolating the linear region to the x-intercept. The linear region is in the oval.

8.2 Obtaining the yield

The yield, Y, is numerically and physically the same as the Internal Quantum Efficiency (IQE). The reflectance and QE measurements must be taken on the samples to obtain the Internal Quantum Efficiency(IQE). The reflectance component is removed from the quantum efficiency data to obtain IQE (eq. 8.2). The QE was measured with light bias or in dark (referred to as light or dark). Measurements were performed in forward bias (0.4V arbitrarily chosen) to avoid tunneling effects at lower

biases and get a more accurate measurement. We analyzed data from a range of 900-1300nm (1.36-0.95eV) since this spans the range where indirect absorption might occur.

$$IQE = \frac{QE}{1-R} \tag{8.2}$$

8.3 Obtaining the valence and conduction band offsets

From the threshold energy and the band gaps of c-Si and a-Si, the valence and conduction band offsets can be calculated (Fig. 8.1).

$$\Delta E_V = E_t - E_{g1} \tag{8.3}$$

$$\Delta E_C = E_{g2} - E_{g1} - \Delta E_v \tag{8.4}$$

E_{g1}=1.12 eV and E_{g2} = 1.64 eV are approximately the band gap of c-Si and a-Si respectively [19,37,36].

8.4 IPE method results

IPE was measured on a series of devices from the same run. The cells have identical wafers and (p) a-Si layers but significant differences in cell performance depending on whether they had front or back i-layers of about 5nm, or if they had differences in heterojunction surface treatment. The device structures and cell performance are shown in table 8.1. The results for all of the MC0584 cells were the same $E_t = 1.01eV \pm 0.01eV$ (see table 8.1 and Fig.8.3) at 0.4V in the dark as well as

light. The measurements are performed at forward bias because tunneling through the discontinuity spike on the valence band side is minimized. However, high electric field at lower voltages (i.e. zero volts) results in tunneling effects [19]. The intrinsic layers apparently do not change the offsets at all. The samples 584-03 and 584-24 have low FF and poor performance. The open-circuit voltage also varies dramatically for the samples. However, we see no difference among the cells using this method. Therefore, this method is not suitable to understand the cell performance. The conduction and valence band offsets can be calculated from equations 8.2 and 8.3. The defects that were detected in C-V and J-V measurements were not detected in this method.

Sample	Conditions	E_t (eV)	ΔE_v (eV)	ΔE_C (eV)	V_{oc} (V)	FF (%)
MC0584-03	no piranha etch, low FF	1.01	-0.11	0.63	0.605	33.1
MC0584-06	piranha etch	1.01	-0.11	0.63	0.589	78.9
MC0584-10	Piranha, only front i-layer	1.01	-0.11	0.63	0.631	81.2
MC0584-18	Piranha, i-layer both sides	1.01	-0.11	0.63	0.67	78.5
MC0584-24	Piranha, i-layer both sides, low FF	1.02	-0.1	0.62	0.636	44.7

Table 8.1: The threshold energy is the same for all samples. Their basic structure is the same. The band offsets are obtained from the IPE method. The band-offsets have no effect on cell performance.

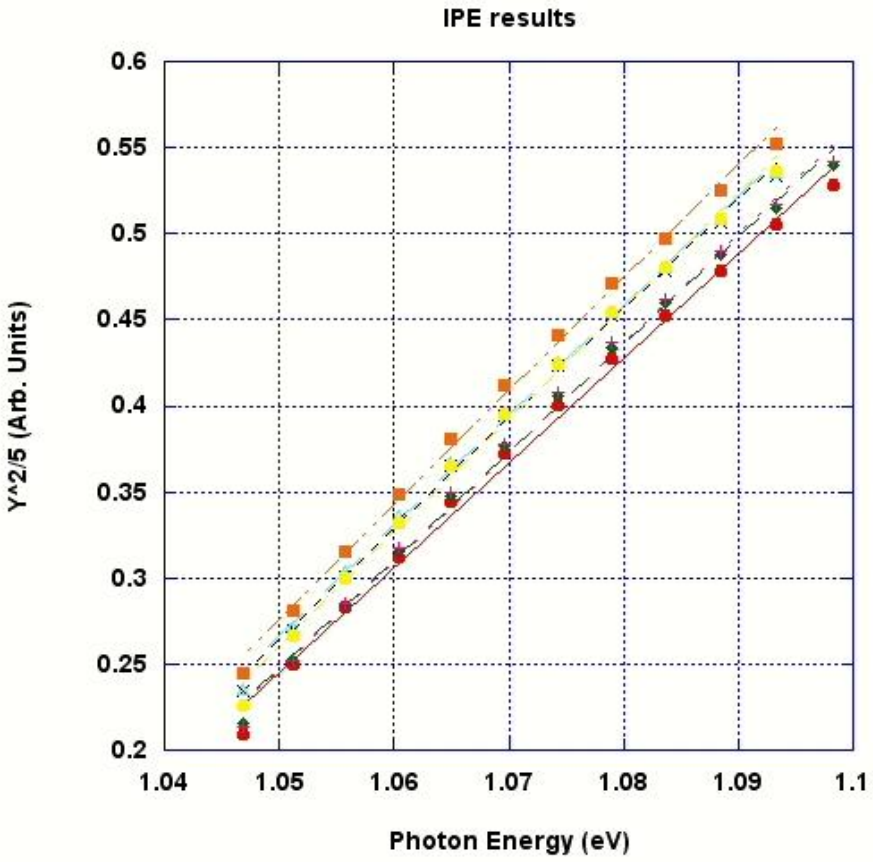

Fig. 8.3: Shown are IPE results for 584-03, 584-06, 584-10, and 584-18 at 0.4V in the dark and light.

The small value for the valence band offset is discussed by Sakata et al. [31] for a B-doped a-Si:H/ c-Si heterojunction structure. Our cells are also doped with diborane (for p-type layers) during processing, so the results can be compared. Moreover, their band offsets are $\Delta E_V = -0.06eV$ and $\Delta E_C = 0.24eV$. The valence band offset agrees well with our value, while the conduction band offsets vary. The

discrepancy can also be due to the variation in the band gap of amorphous silicon of different groups. From the IPE method, the hopping conduction can be detected. Therefore, while IPE is immune to defects, it can detect hopping conduction and tunneling of carriers. It measures the effective band discontinuity. Mimura et al. [30] reported $\Delta E_V = 0.71eV$ and $\Delta E_C = 0.09eV$ as their band-offsets. Our results are not similar. We had anticipated that IPE would be more valuable in identifying why certain device structures had s-curves and low open-circuit voltage to others since it has been used by others to characterize similar a-Si/c-Si heterojunction solar cells. Further work is required to understand the internal photoemission process.

Chapter 9

DISCUSSION

Various electrical measurements were used to characterize Si heterojunction solar cells to obtain parameters that are related to the basic device performance. Measurements included capacitance based (standard C-V, DLCP, impedance spectroscopy), internal photoemission, and temperature dependent J-V measurements. We examined solar cells with an i-layer, typically 5nm thick, either in the front, the back, both sides, or no i-layers. It is shown in the thesis that adding the i-layer either in the back or front improves the open-circuit voltage in general. The surface preparation was also evaluated by comparing samples with and without piranha etch.

In this thesis, electrical measurements and analysis focus primarily on the effect of the i-layer on V_{oc} and FF.

Doping concentration of c-Si wafer, excess defect density, and the free-carrier density in a cell can be obtained from C-V measurements using different methods as discussed in chapter 5. The doping concentration was obtained from the slope of $\frac{1}{C^2}$ vs. V plot. Excess defect density was obtained from the difference of carrier concentration at deep and shallow states (low frequency) and at deep states (high frequency). The free-carrier density does not include traps and defects in the cell, and it was obtained as a function of spatial position from DLCP method at different

frequencies. Excess defects seem to have an effect on V_{oc}. Specifically, when 5nm i-layer is added in the back, the excess defects decrease dramatically and improve V_{oc} at the same time.

Parallel capacitance, parallel resistance, and series resistance were derived from the frequency dependence of complex impedance at forward bias (Impedance Spectroscopy). A Nyquist plot was obtained assuming a simple parallel equivalent RC circuit model. The product of the parallel capacitance and resistance determine the minority carrier recombination lifetime. Open-circuit voltage of a cell is a function of this lifetime, so lifetime obtained from this method is indirectly a measurement of V_{oc}. A sample with high lifetime tends to have a higher open-circuit voltage as discussed in chapter 6. The lifetime obtained from IS method was compared to Sinton tester lifetime. Although they agree well for most of the part, they are not the same. This might be because Sinton lifetime was measured immediately after the deposition of layers while the IS measurements were made weeks or years for some of the samples in this thesis. It is possible that the cell's performance changed overtime as observed with IEC samples. In general, samples with higher lifetime by either method (with 5nm i-layer in the front or both sides) have higher V_{oc}.

Temperature dependent J-V give the A factor, series resistance, saturation current, and the barrier height of a solar cell. While the saturation current informs about the amount of recombination and is inversely proportional to V_{oc}, the A factor determines if the recombination is occurring in the bulk or at an interface. When the

samples have poor fill factor, it is reflected in the barrier height of the cell, and the barrier height is lower than the band gap of c-Si. Also, the A factor is greater than the theoretical upper limit of A = 2 when the samples have low fill factor (s-shaped curve). The i-layers, and therefore, V_{oc}, have no effect on the A factor, saturation current and the barrier height. Series resistance measured in SHJ solar cells is usually low, and it was observed here. Also, the series resistance from the IS method agrees well with this series resistance.

Internal photoemission (IPE) method looks at the photoresponse at the junction to photons with low energy. When the photon is absorbed and an electron-hole pair is formed, IPE determines the energy it takes for carriers to overcome the offset barrier to be collected. This energy is the threshold energy. The valence and conduction band-offsets were calculated from the threshold energy assuming the band gaps c-Si and a-Si are known. In chapter 8, IPE showed that a selected group of samples with and without i-layers and a wide range of open-circuit voltage and fill factor have the same valence and conduction band offset. Thus, band-offsets obtained from internal photoemission method appear to have no relation to cell performance, in contrast to simulation results from others. This method was not useful to understand the cell performance; however it can be used to estimate the band offsets in the SHJ solar cell with n-type c-Si wafer.

A major issue for capacitance measurements is that the IS measurements and C-V measurements were performed in the dark. J-V curves and quantum efficiency measurements were obtained in dark and light bias. There could be discrepancies

between measurements for samples with poor fill factor (s-shaped curves in light) that are not seen in the dark. By definition, it is assumed for capacitance and IPE measurements that the device is not limited by transport or collection of carriers, but rather by their frequency response or their energetic dependence. We may not be getting enough information about carrier transport in the device from the measurements investigated here. Capacitance measurements in light and forward bias could help reveal interesting information on the recombination.

Our ultimate goal is to understand front heterojunction Si solar cells in order to improve the cell performance of the back contact HIT devices because they have greater potential for high efficiency (>20%) [2]. The electrical measurements discussed in this thesis will help understand the heterojunction device physics. Currently, we are able to process front or back contact cells with 15% efficiency (table 9.1) where MC0625-10 is the IBC solar cell and MC0584-10 is the front junction solar cell that was analyzed in this thesis. The table shows the cell performance for each cell including the series resistance, saturation current, and the ideality factor. The diode parameters were obtained from dark curve for both cells. The IBC solar cell has high short-circuit current which is not generally seen in the front junction solar cells. This could be because all the area on the front is available to collect photons in an IBC cell. High efficiencies are possible if these devices are fabricated properly to get high open-circuit voltage and fill factor.

Parameters	MC0625-10	MC0584-10
Voc (V)	0.62	0.629
Jsc (mA/sqcm)	34.1	29.98
FF (%)	70.2	80.4
eff. (%)	14.8	15.2
R (ohm)	0.88	0.94
Jo (mA/sqcm)	2.48E-05	5.36E-09
A	1.595769	25.81

Table 9.1: Shown are cell parameters and diode analysis parameters obtained from dark curves. MC0625-10 is the IBC solar cell and 584-10 is the front junction solar cell. Both have about an efficiency of about 15%.

Future work

In this thesis, electrical measurements were applied only to front junction HIT solar cells to understand the cell performance. Samples with different wafers (n and p type) and different structures should be tested especially to understand IPE measurements. Once we have a better understanding of the electrical measurements and methods, we would like to apply some of these to characterize IBC HIT solar cells that are also processed at IEC.

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