A Physically-Based Model of Vertical TFET—Part II: Drain Current Model

Qi Cheng [ID], Sourabh Khandelwal [ID], *Senior Member, IEEE*, and Yuping Zeng [ID], *Member, IEEE*

Abstract—**A physically based model for the tunneling current of vertical tunneling field transistors (TFET) is proposed. In part I, the expression of $\varphi_{1D}(x)$ is derived from the multi-branch general solutions of Poisson's equation. The model's results are verified with TCAD simulation for transistors with different materials, device geometries, and biases. In this article, a surface potential model is validated at different device regions which include channel and drain. Based on the above two electric potential models, Kane's tunneling formula is utilized for the calculation of band-to-band tunneling current. The proposed current model is valid for all transistors' operating regions. The quantum effect on the band-structure parameters is taken into account in the modeling of InAs vertical TFET. It is shown that the channel thickness needs to be optimized to achieve the highest drive current.**

Index Terms—**Band-to-band tunneling, compact model, line tunneling, tunneling FET.**

I. INTRODUCTION

TUNNELING field transistors (TFET) have been viewed as a promising candidate for energy-efficiency application [1], [2]. Compared with MOSFET, TFET is more power-efficient because of its potential to achieve a steeper subthreshold slope (*SS*) and higher ON/OFF current ratio at room temperature [3], [4]. However, the existing TFET technology still has the drawback of the low ON current [5]. Enormous efforts have been made to alleviate this problem. The recent development of vertical TFET has drawn the attention of the research community [6]–[8]. Compared with the "point tunneling" of the lateral TFET, "line tunneling" is the main tunneling mechanism in the vertical TFET. The area of vertical TFET's active band-to-band tunneling region is larger than that of lateral TFET [9]. Thus, vertical TFET can achieve higher I_{ON} [10]–[12].

But the existing publications about the fabricated vertical TFET still show issues such as high subthreshold slope and

current non-saturated problem [6], [11]. Further studies are essential for the comprehensive understanding of device properties and performance dependence on device parameters [13]. A compact model derived based on the electric potential is still needed for a better understanding of device physics [14]. Several models have been proposed for TFET with "line tunneling" [8], [9], [15], [16]. But they assume that the inversion charge density of the channel can be ignored. Linear or parabolic potential distribution approximation is utilized, which severely reduces the model's accuracy in the inversion region [17].

In Part I, an analytical electric potential model is proposed for the source and region 1 based on the general solution of Poisson's equation. The effect of the inversion charge is taken into account. The results of the model are verified with TCAD and found to be accurately predicting the simulation results for different device and material parameters. In this article, in Section II, the electric potential model is extended to region 2 (channel) and drain. In Section III, utilizing Kane's tunneling theory and electric potential model from part I [18], the tunneling current model is developed. In Section IV, the model results are compared against those of TCAD simulation for different sets of parameters. It is well known that small-bandgap materials such as InAs are preferred for the fabrication of TFET. However, the band structure of InAs becomes thickness-dependent due to quantum confinement effects in the nanoscaled device and deviates remarkably from that of the bulk InAs. The quantum effect on the drive current of InAs vertical TFET is demonstrated.

II. SURFACE ELECTRIC POTENTIAL MODEL

A. Review of $\varphi_{1\text{-}D}(x)$ and $\varphi_s(x)$

The structure of the transistor used in the article is shown in Fig. 1. The source, channel, and drain regions are p$^+$ doped (N_s), undoped, and n$^+$ doped (N_d), respectively. The channel thickness is t_c, the HfO$_2$ gate oxide thickness is t_{ox}. The gate work function is 3.7 eV, N_d is 10^{19} cm^{-3}, the height of source region H_s is 30 nm, W_1 and W_2 are both 40 nm, and the length of drain region W_D is 10 nm in this article. Boltzmann statistics, Poisson's equation, and carrier's continuity equations are activated to simulate the electric potential, the non-local dynamical band-to-band tunneling model is included to compute the tunneling current [19], [20]. SRH recombination model is utilized for the leakage current. The default materials for the source, channel, and drain regions are Ge with parameters from [21] at 300 K. In Part I, the
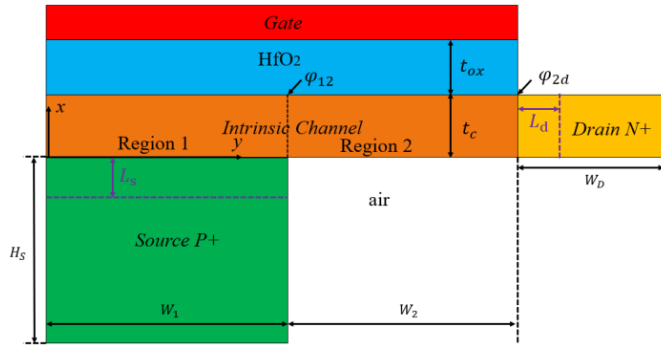
Fig. 1. Schematic of the vertical TFET. The coordinate system and the device's geometrical parameters are also depicted.

electric potential model has been derived for $\varphi_{1D}(x)$ as

$$\varphi_{1D}(x) = V - \frac{2kT}{q}\ln\left[\text{Sinh}\left(\frac{\beta}{t_c}x + \alpha\right)\right] + \frac{kT}{q}\ln\left(\frac{2\varepsilon_c kT\beta^2}{q^2 n_i t_c^2}\right) \quad (1)$$

where $V = V_{ds}$ is the applied drain voltage, ε_c and n_i are the relative dielectric constant and intrinsic carrier density of the channel material, respectively. t_c is the channel thickness. α and β are two parameters without any unit and can be determined from the boundary conditions.

As shown in Fig. 1, the source depletion region is within $-L_s \leq x < 0$, its electric potential is approximated as a parabolic function as

$$\varphi_s(x) = A_s(x + L_s)^2 + \varphi_{sl} \quad (2)$$

where L_s is the length of the source depletion region, $A_s = (\varphi_{s0} - \varphi_{sl})/L_s^2$. φ_{sl} is the electric potential in the source neutral region.

B. Channel Surface Electric Potential

The analysis starts with the surface electric potential $\varphi_{c.s}(y)$ at the interface between channel and gate oxide. In Fig. 1, $\varphi_{c.s}(y)$ can be separated into $\varphi_{c.s1}(y)$ and $\varphi_{c.s2}(y)$ for regions 1 and 2, respectively as follows:

In region 1 ($0 < y \leq W_1$), $\varphi_{c.s1}(y)$ is formulated as [22]

$$\varphi_{c.s1}(y) = \varphi_{1D}(t_c) + [\varphi_{12} - \varphi_{1D}(t_c)]e^{\frac{y-W_1}{\lambda_{1s}}} \quad (3)$$

where φ_{12} is an unknown channel surface potential at the interface of regions 1 and 2 as shown in Fig. 1, λ_{1s} is the characteristic length and expressed as [22]–[24]

$$\lambda_{1s} = \frac{1}{\sqrt{\frac{\varepsilon_{ox}}{\varepsilon_c t_c t_{ox}} - \frac{4q N_{inv1}}{\varepsilon_c t_c[\varphi_{1D}(t_c) - \varphi_{12}]}}} \quad (4)$$

where N_{inv1} is the inversion charge density per-gate length of region 1 and can be calculated by the Gaussian theory as

$$N_{inv1} = \frac{\varepsilon_c}{q}\left(\left.\frac{\partial \varphi_{1D}}{\partial x}\right|_{x=t_c} - \left.\frac{\partial \varphi_{1D}}{\partial x}\right|_{x=0}\right). \quad (5)$$

In region 2 ($W_1 < y \leq W_1 + W_2$), the surface electric potential is given by [24], [25] as

$$\varphi_{c.s2}(y) = \varphi_{2ls} + (\varphi_{12} - \varphi_{2ls})\frac{\text{Sinh}\left(\frac{W_1+W_2-y}{\lambda_{2s1}}\right)}{\text{Sinh}\left(\frac{W_2}{\lambda_{2s1}}\right)}$$
$$+ (\varphi_{2d} - \varphi_{2ls})\frac{\text{Sinh}\left(\frac{y-W_1}{\lambda_{2sd}}\right)}{\text{Sinh}\left(\frac{W_2}{\lambda_{2sd}}\right)} \quad (6)$$

where φ_{2ls} is the surface potential solution of the long channel model as [26]

$$\varphi_{2ls} = V_{ds} - \frac{2kT}{q}\ln\left[\frac{t_c}{\beta^*}\sqrt{\frac{q^2 n_i}{2\varepsilon_c kT}}\text{Cos}(\beta^*)\right]. \quad (7)$$

λ_{2s1} and λ_{2sd} are the characteristic lengths for the left and right terminals of region 2 respectively,

$$\lambda_{2s1} = \frac{1}{\sqrt{\frac{\eta\varepsilon_{ox}}{\varepsilon_c t_c t_{ox}} - \frac{4\eta q N_{inv2}}{\varepsilon_c t_c(\varphi_{12}-\varphi_{2ls})}}} \quad (8)$$

$$\lambda_{2sd} = \frac{1}{\sqrt{\frac{\varepsilon_{ox}}{\varepsilon_c t_c t_{ox}} + \frac{4q N_{inv2}}{\varepsilon_c t_c|\varphi_{2ls}-\varphi_{2d}|}}} \quad (9)$$

where $\eta = 0.3$ [25], φ_{2d} is an unknown channel surface potential at the interface between region 2 and drain as indicated in Fig. 1. N_{inv2} is the inversion charge density per-gate length of region 2 and expressed by

$$N_{inv2} = \frac{\varepsilon_{ox}}{q t_{ox}}(V_{gs} - V_{fb} - \varphi_{2ls}). \quad (10)$$

In the drain depletion region ($W_1 + W_2 < y \leq W_1 + W_2 + L_d$), the surface potential $\varphi_{d.s}(y)$ is expressed by a parabolic function

$$\varphi_{d.s}(y) = \pm\frac{q N_d}{2\varepsilon_c}(L_d + W_1 + W_2 - y)^2 + \varphi_{dl} + V_{ds} \quad (11)$$

where $\varphi_{dl} = kT/q\ln(N_d/n_i)$ is the drain built-in voltage, L_d is the length of drain depletion region and given by: $L_d = (2\varepsilon_d|\varphi_{dl} + V_{ds} - \varphi_{2d}|/q N_d)^{1/2}$. If $\varphi_{2ls} < \varphi_{dl} + V_{ds}$, the sign in (11) is "$-$"; If $\varphi_{2ls} > \varphi_{dl} + V_{ds}$, the sign is "$+$". φ_{12} and φ_{2d} are solved by the continuity of electric field between regions 1 and 2, and drain [24]. The surface electric potential calculated by the model is compared with the TCAD simulation in Fig. 2. In the previous publications [27], subthreshold approximation has been made in the derivation of surface electric potential. λ_{1s}, λ_{2s1}, and λ_{2sd} are $(\varepsilon_c t_c t_{ox}/\varepsilon_{ox})^{1/2}$, $(\varepsilon_c t_c t_{ox}/\eta\varepsilon_{ox})^{1/2}$, and $(\varepsilon_c t_c t_{ox}/\varepsilon_{ox})^{1/2}$, respectively. Substituting these simplified characteristic lengths into (3) and (6), another set of surface potential can be solved. The resulting surface electric potential is notified as a "subthreshold model." As shown in Fig. 2(b), it can be observed that our model's results show a close match with TCAD. The subthreshold model ignores the effect of inversion charge on the characteristic length, thus it induces error.
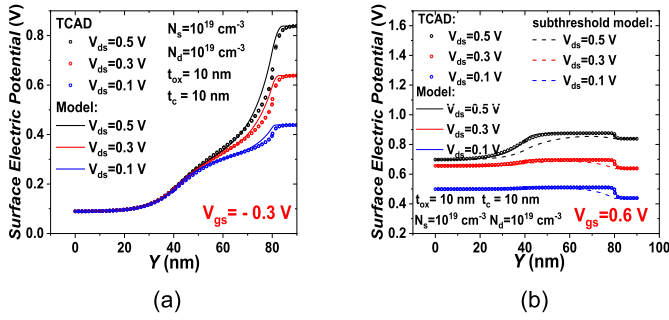
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Fig. 2. Comparison of surface electric potential solved by the model and TCAD simulation: (a) $V_{gs} = -0.3$ V and (b) $V_{gs} = 0.6$ V.

III. CURRENT MODEL

A. Tunneling Current in Region 1

The band-to-band tunneling process is modeled by Kane's tunneling [18], [19]. The BTBT generation rate (G_{b2b}) of the carriers per unit volume per unit time is given by

$$G_{b2b} = A\left(\frac{E}{E_p}\right)^P \text{Exp}\left(-\frac{B}{E}\right) \tag{12}$$

where $E_p = 1$ V/cm, $P = 2$ or 2.5 for the direct or indirect tunneling. A and B are material-dependent tunneling parameters depending on the bandgap and carrier effective mass [20]. The tunneling current can be derived by integrating (12) over the tunneling volume after a split up in E and E_{av} as [28]

$$I_{\text{BTBT}} = qW_1 \int_{x_1}^{t_c} A\frac{E_{\text{local}}}{E_p}\left(\frac{E_{av}}{E_p}\right)^{P-1}\text{Exp}\left(-\frac{B}{E_{av}}\right)(f_s - f_c)dx \tag{13}$$

where $E_{\text{local}} = \partial\varphi_{1D}/\partial x$ is the local electric field, E_{av} is the average electric field over the tunneling path ($E_{av} = E_g/ql_{\text{path}}$, with l_{path} being the length of the tunneling path). f_s and f_c are expressed as the Sentaurus device manual [19]

$$f_s = \frac{1}{1 + e^{\frac{\varepsilon}{kT}}} \tag{14}$$

$$f_c = \frac{1}{1 + e^{\frac{\varepsilon + qV_{ds}}{kT}}} \tag{15}$$

where ε is the carrier energy. As shown in Fig. 3, x_1 is the point at which the energy difference between the valence band of the source neutral region and the channel's valence band reaches E_g. At $x = x_2$, the valence band energy is lower than that at $x = 0$ by E_g. When $x_1 \leq x < x_2$, the band-to-band tunneling starts from the valence band of the source and ends at the conduction band of the channel; When $x_2 \leq x \leq t_c$,

the band-to-band tunneling occurs between the conduction and valence bands of the channel. x_1 and x_2 are solved by the following:

$$\varphi_{1D}(x_1) = \varphi_{sl} + \frac{E_g}{q} \tag{16}$$

$$\varphi_{1D}(x_2) = \varphi_{s0} + \frac{E_g}{q}. \tag{17}$$

Inserting (1) into (16) and (17), x_1 and x_2 can be formulated as

$$x_1 = \frac{t_c}{\beta}\text{Arcsinh}\left\{e^{\frac{q}{2kT}\left[V_{ds} + \frac{kT}{q}\ln\left(\frac{2\varepsilon_c kT\beta^2}{q^2 n_i t_c^2}\right) - \varphi_{sl} - \frac{E_g}{q}\right]}\right\} - \frac{t_c\alpha}{\beta} \tag{18}$$

$$x_2 = \frac{t_c}{\beta}\text{Arcsinh}\left\{e^{\frac{q}{2kT}\left[V_{ds} + \frac{kT}{q}\ln\left(\frac{2\varepsilon_c kT\beta^2}{q^2 n_i t_c^2}\right) - \varphi_{s0} - \frac{E_g}{q}\right]}\right\} - \frac{t_c\alpha}{\beta} \tag{19}$$

where $x_1 \leq t_c$ and $x_2 \leq t_c$. l_1 and l_2 are the l_{path} in the region $x_1 \leq x < x_2$ and $x_2 \leq x \leq t_c$ as shown in Fig. 3, respectively. They can be derived based on the following relationships [29]

$$\varphi_s(x - l_1) + \frac{E_g}{q} = \varphi_{1D}(x) \tag{20}$$

$$\varphi_{1D}(x - l_2) + \frac{E_g}{q} = \varphi_{1D}(x). \tag{21}$$

Then l_1 and l_2 are derived as (22) and (23), shown at the bottom of the page, and I_{BTBT} can be reformulated as

$$\begin{aligned}
I_{\text{BTBT}} &= I_{l1} + I_{l2}\\
&= qW_1\left[\int_{x_1}^{x_2} A\frac{E_{\text{local}}}{E_p}\left(\frac{E_{av1}}{E_p}\right)^{P-1}\text{Exp}\left(-\frac{B}{E_{av1}}\right)(f_s - f_c)dx\right.\\
&\quad\left. + \int_{x_2}^{t_c} A\frac{E_{\text{local}}}{E_p}\left(\frac{E_{av2}}{E_p}\right)^{P-1}\text{Exp}\left(-\frac{B}{E_{av2}}\right)(f_s - f_c)dx\right]
\end{aligned} \tag{24}$$

where I_{l1} and I_{l2} are the tunneling currents in the regions $x_1 \leq x < x_2$ and $x_2 \leq x \leq t_c$ as shown in Fig. 3, respectively. E_{av1} and E_{av2} are equal to E_g/ql_1 and E_g/ql_2.

As shown in Fig. 4, V_{gs} is swept from 0 to 1 V, it can be observed that the starting voltages for tunneling are 0.08 and 0.22 V for I_{l1} and I_{l2}, respectively. The reason for this phenomenon is as follows: when $V_{gs} < 0.08$ V, $x_1 = x_2 = t_c$. I_{l1} and I_{l2} are all equal to zero as indicated in (24); when 0.08 V $< V_{gs} < 0.22$ V, $x_1 < x_2 =_c$, I_{l1} is larger than zero and I_{l2} remains zero; when $V_{gs} \geq 0.22$ V, $x_1 < x_2 < t_c$, both of I_{l1} and I_{l2} are larger than zero.

Most of the studies on the TFET modeling derive the tunneling current model relying on the source-to-channel tunneling

$$l_1 = x - \left\{\sqrt{\frac{V_{ds} - \frac{2kT}{q}\ln\left[\sinh\left(\frac{\beta}{t_c}x + \alpha\right)\right] + \frac{kT}{q}\ln\left(\frac{2\varepsilon_c kT\beta^2}{q^2 n_i t_c^2}\right) - \left(\varphi_{sl} + \frac{E_g}{q}\right)}{A_s}} - L_s\right\} \tag{22}$$

$$l_2 = x - \frac{t_c}{\beta}\text{Arcsinh}\left[e^{\frac{E_g}{2kT}}\sinh\left(\frac{\beta}{t_c}x + \alpha\right)\right] + \frac{\alpha t_c}{\beta} \tag{23}$$

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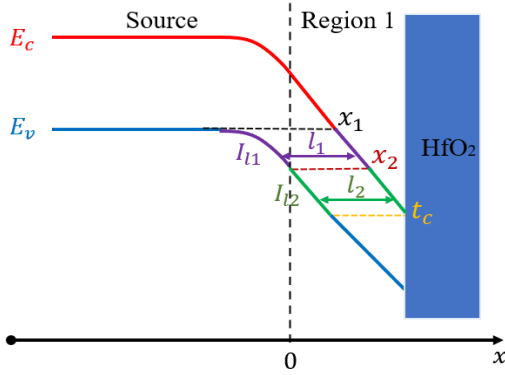
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Fig. 3. Energy band diagram along the source and region 1. l_1 and l_2 are the tunneling paths of source-to-channel tunneling and channel-to-channel tunneling, respectively.
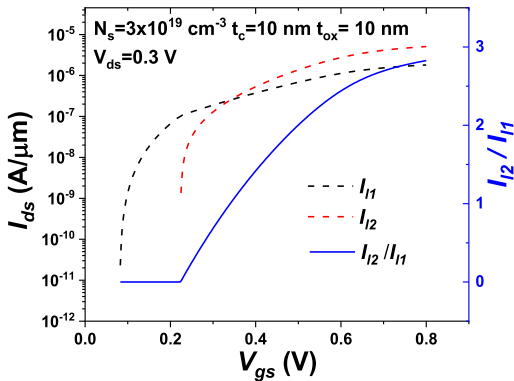

Fig. 4. I_{l1} and I_{l2} of a Ge vertical TFET with $N_s = 3 \times 10^{19}$ cm^{-3}, $t_c = 10$ nm, and $t_{ox} = 10$ nm.

current I_{l1} [29], [30]. Indeed, I_{l1} should dominate the tunneling current of lateral TFETs. However, as shown in Fig. 4, our model reveals that I_{l2} plays a more important role in the high V_{gs} region. The value of I_{l2}/I_{l1} reaches 2.5 when V_{gs} equals 0.6 V. The model predicted I_{l1} are larger than that of I_{l2} when $V_{gs} < 0.3$ V. It indicates that both I_{l1} and I_{l2} should be taken into account in the modeling of vertical TFET.

B. V_{gson}

The tunneling current calculated by (24) is compared with the TCAD simulation as shown in Fig. 5. It can be inferred from the figure that the model's results only fit the simulation in the high-V_{gs} region ($V_{gs} \geq V_{gson}$), where V_{gson} is the minimum value that (24) can agree with TCAD. For example, conducting the measurement of subthreshold slope (SS) between the current level 10^{-12} and 10^{-10} A/μm, SS of the model is 12.5 mV/dec, but SS of the simulated result is around 33 mV/dec. The physics behind this phenomenon can be explained as follows: as shown in Fig. 6(a), the electric potential allows for band-to-band tunneling in the channel, defined as

$$\varphi_t(y) = \varphi_{c.s}(y) - \varphi_{t.\min} \tag{25}$$

where $\varphi_{c.s}(y)$ is the channel surface electric potential model proposed in Section II-B, $\varphi_{t.\min} = \varphi_{sl} + E_g/q$ is the minimum channel electric potential that allows band-to-band tunneling.
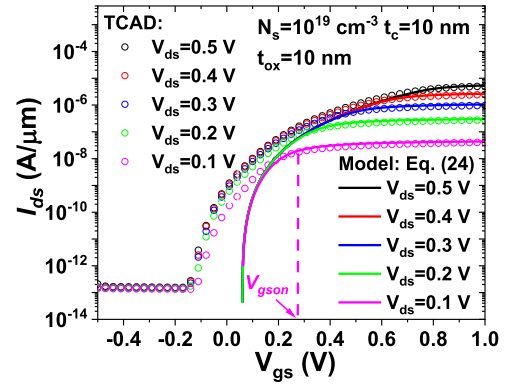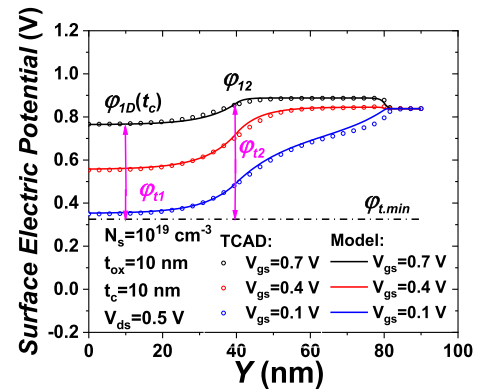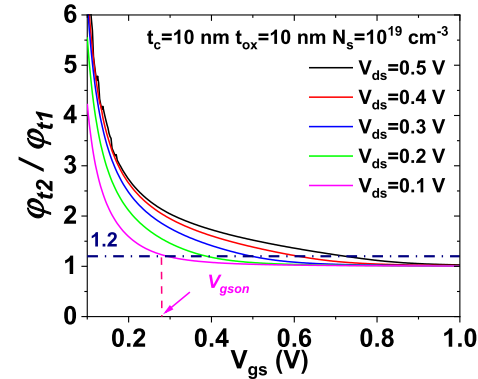

Fig. 5. Comparison of the tunneling current calculated by (24) and TCAD simulation. In both TCAD simulation and model calculation, $N_s = 10^{19}$ cm^{-3}, $t_c = 10$ nm, $t_{ox} = 10$ nm. The pink $I_{ds}-V_{gs}$ curve when $V_{ds} = 0.1$ V are adopted to demonstrate V_{gson} here.

(a)

(b)

Fig. 6. (a) Surface electric potentials predicted by TCAD and model, φ_{t1} and φ_{t2} are indicated by the pink arrows when $V_{gs} = 0.7$ V, $\varphi_{1D}(t_c)$ and φ_{12} are the channel surface electric potential in the 1-D tunneling region and at the interface of regions 1 and 2, respectively. (b) Values of $\varphi_{t2}/\varphi_{t1}$ versus different V_{ds} and V_{gs} when $\varphi_{t1} > 0$.

Thus, $q\varphi_t(y)$ is the tunneling window as a function of y. φ_{t1} and φ_{t2} are the $\varphi_t(y)$ at $y = 10$ nm and $y = 40$ nm, respectively. As the V_{gs} reduces from 0.7 to 0.1 V, φ_{t1} approaches zero and $\varphi_{t2} - \varphi_{t1}$ gets evidently larger. It indicates that the band-to-band tunneling near $y = 40$ nm plays a dominating role when the gate voltage becomes lower [16]. However, this effect is not taken into account in (24).

To find the value of V_{gson}, the model predicted $\varphi_{t2}/\varphi_{t1}$ under different biases, which is plotted in Fig. 6(b). It should be

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noted that $\varphi_{t2}/\varphi_{t1}$ increases rapidly as φ_{t1} approaches 0 V on the left part of the figure. As V_{gs} becomes larger, the value of $\varphi_{t2}/\varphi_{t1}$ decreases and approaches 1, the G_{b2b} at $y = 10$ nm and $y = 40$ nm are close to each other. Thus, (24) agrees with the TCAD simulated results. The intersection of 1.2 and the curve $\varphi_{t2}/\varphi_{t1}$ is defined as V_{gson} for this device. As indicated in Figs. 5 and 6(b), when $V_{ds} = 0.1$ V, V_{gson} is around 0.28 V.

C. V_{OFF}, I_{OFF}, and the Transit Region

The upper limit of the OFF-status region (V_{OFF}) is the gate voltage at which φ_{t2} is set to 0. When V_{gs} equals V_{OFF}, the band-to-band tunneling is completely turned off in region 1. The band-to-band tunneling between region 2 and the source region can be ignored because of the longer tunneling distance.

The OFF-status current (I_{OFF}) in the vertical TFET is p-i-n diode reverse diffusion current, the ambipolar effect is not considered here. For a Ge vertical TFET operating at room temperature, the diffusion coefficients for electron and hole are $D_n = 101$ cm^2/s and $D_p = 49$ cm^2/s, respectively [19]. The carrier lifetime for electron and hole are set to $\tau_n = 10^{-5}$ s and $\tau_p = 5 \times 10^{-5}$ s [31]. Thus, the corresponding diffusion lengths are $L_n = 317$ μm for the electron and $L_p = 495$ μm for the hole. Mohammadi and Khaveh [17], a drain voltage-independent expression for the OFF current density is proposed. However, both L_n and L_p are substantially larger than the lengths of p$^+$ and n$^+$ regions in the TFET. The "short" diode current approach works better in the modeling of TFET [32]. The OFF-status leakage current is expressed as

$$I_{OFF} = \frac{W_1 q D_n n_i^2}{N_s H_s} + \frac{t_c q D_p n_i^2}{N_D W_D} \quad (26)$$

where H_s is the height of source, W_D is the width of the drain region.

The transit region is defined as $V_{OFF} < V_{gs} < V_{gson}$. The current formula $I_{transit}$ of this transit region follows a mathematical approach [33]. $I_{transit}$ is equal to I_{OFF} when $V_{gs} = V_{OFF}$. $I_{transit}$ and its first-order derivative are continuous with I_{BTBT} when $V_{gs} = V_{gson}$ [34]

$$I_{transit}(V_{gs} = V_{OFF}) = I_{OFF} \quad (27)$$

$$I_{transit}(V_{gs} = V_{gson}) = I_{BTBT}(V_{gs} = V_{gson}) \quad (28)$$

$$\left. \frac{\partial I_{transit}}{\partial V_{gs}} \right|_{V_{gs} = V_{gson}} = \left. \frac{\partial I_{BTBT}}{\partial V_{gs}} \right|_{V_{gs} = V_{gson}}. \quad (29)$$

The model's results are compared with those of TCAD simulation in Fig. 7 in the following three regions.

1) When $V_{gson} \leq V_{gs}$, I_{ds} is equal to I_{BTBT} of (24).
2) When $V_{OFF} < V_{gs} < V_{gson}$, transit current model $I_{transit}$ is adopted to calculate I_{ds}.
3) When $V_{gs} \leq V_{OFF}$, the leakage current is derived by (26). The good agreement indicates that our model works for all operating regions.

The band-tail effects can be detrimental to the TFET performance [35]–[38], especially, the performances in the subthreshold region are severely degraded by these density-of-state tails in the bandgap. As indicated in Fig. 8, the valence band tail Δv can generate leakage current between the source
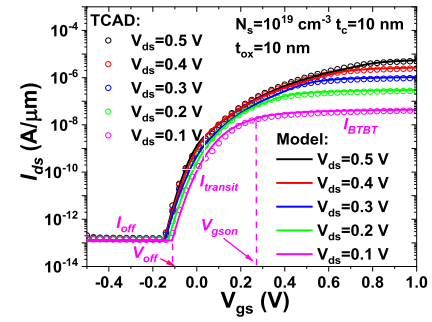

Fig. 7. Comparison of model-predicted I_{ds}–V_{gs} with TCAD simulation, the three operating regions are indicated for transistor with $V_{ds} = 0.1$ V.
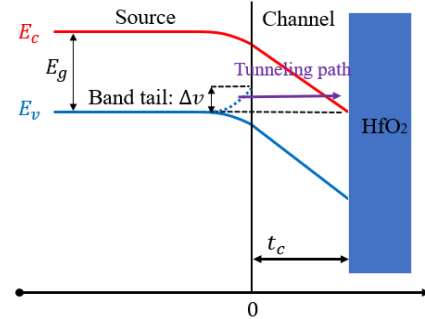

Fig. 8. Band diagram of a vertical TFET in the subthreshold region. The dash blue curve indicates the valence band tail that generates the leakage current.
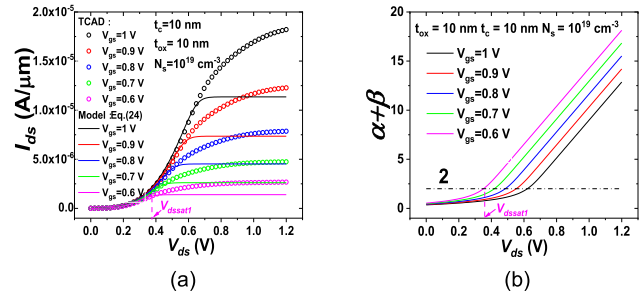

Fig. 9. (a) Verification of (24)'s results with TCAD simulation: I_{ds}–V_{ds} characteristics and (b) $\alpha + \beta$ calculated by model. The transistor with $V_{gs} = 0.6$ V is adopted to demonstrate V_{dssat1}.

and channel [39], inducing a larger SS and an earlier onset voltage of tunneling. The modified V_{OFF} due to the band-tail effects is the gate voltage at which the following holds:

$$\varphi_{12} = \varphi_{sl} + \frac{E_g - \Delta v}{q}. \quad (30)$$

Thus, V_{OFF} reduces when the band-tail effects are taken into account [35]. For the $I_{transit}$, a larger value of SS is needed for the smooth transition between the OFF- and ON-status.

D. I_{ds}–V_{ds} Model

As shown in Fig. 9(a), the I_{ds}–V_{ds} characteristics calculated by (24) are compared with TCAD simulation. It indicates that (24) predicts lower results than TCAD in the high V_{ds} region ($V_{ds} > V_{dssat1}$). Because φ_{12} increases with the enhancement of V_{ds}, but this effect is not taken into account in (24).

In part I, the condition $\alpha + \beta > 2$ is used as the judgment to determine whether the linear approximation of $\varphi_{1D}(x)$ holds or
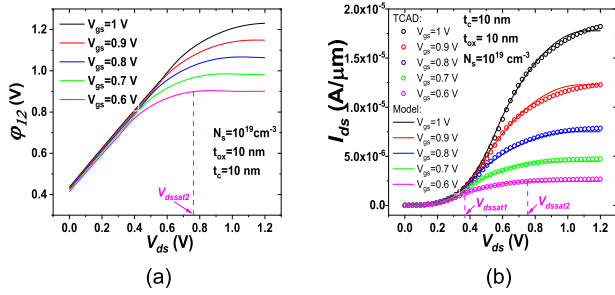
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Fig. 10. (a) φ_{12} calculated by the model, the transistor with $V_{gs} = 0.6$ V is adopted to demonstrate V_{dssat2} and (b) verification of model-predicted results with TCAD simulation.

not. When $\alpha + \beta > 2$ is valid, $\varphi_{1D}(x)$ can be treated as a linear function of x, and $\varphi_{1D}(x)$ is independent of V_{ds}. Thus, the tunneling current calculated by (24) is saturated with V_{ds} and smaller than the results from TCAD as indicated in Fig. 9(a). In Fig. 9(b), the intersection of the line "2" and $\alpha + \beta$ is notified as V_{dssat1}, the corresponding drain current I_{dssat1} can be calculated by inserting $V_{ds} = V_{\mathrm{dssat1}}$ into (24).

As shown in Fig. 10(a), the model predicted φ_{12} will be saturated with the increasing of V_{ds}, which is consistent with the conclusion drawn by TCAD simulation [40]. The saturated drain voltage is notified as V_{dssat2}. The model for the $I_{ds}-V_{ds}$ characteristic can be divided into three regions as below.

When $V_{ds} < V_{\mathrm{dssat1}}$, $\alpha + \beta < 2$ holds. Equation (24) accurately agrees with the TCAD. The drain current expression is (24)

$$I_{ds} = I_{\mathrm{BTBT}} \tag{31}$$

and g_{dssat1} is the output transconductance (g_{ds}) derived by (24) when V_{ds} is equal to V_{dssat1}.

When $V_{\mathrm{dssat1}} \leq V_{ds} < V_{\mathrm{dssat2}}$, g_{ds} can be approximated as a linear function that reaches the maximum value of g_{dssat1} at $V_{ds} = V_{\mathrm{dssat1}}$ and the minimum value of 0 at $V_{ds} = V_{\mathrm{dssat2}}$ [32]

$$g_{ds} = \frac{dI_{ds}}{dV_{ds}} = \frac{g_{\mathrm{dssat1}}(V_{\mathrm{dssat2}} - V_{ds})}{V_{\mathrm{dssat2}} - V_{\mathrm{dssat1}}}. \tag{32}$$

Performing an integration from $V_{ds} = V_{\mathrm{dssat1}}$ based on (32), the current formula is formed as

$$I_{ds}(V_{ds}) = I_{\mathrm{dssat1}} + \frac{g_{\mathrm{dssat1}}\left(V_{\mathrm{dssat2}}V_{ds} - \frac{V_{ds}^2}{2}\right)}{V_{\mathrm{dssat2}} - V_{\mathrm{dssat1}}} - \frac{g_{\mathrm{dssat1}}\left(V_{\mathrm{dssat2}}V_{\mathrm{dssat1}} - \frac{V_{\mathrm{dssat1}}^2}{2}\right)}{V_{\mathrm{dssat2}} - V_{\mathrm{dssat1}}}. \tag{33}$$

When $V_{ds} \geq V_{\mathrm{dssat2}}$, the expression of saturated drain current is derived by inserting $V_{ds} = V_{\mathrm{dssat2}}$ into (33)

$$I_{\mathrm{dssat}} = I_{\mathrm{dssat1}} + \frac{g_{\mathrm{dssat1}}V_{\mathrm{dssat2}}^2}{2(V_{\mathrm{dssat2}} - V_{\mathrm{dssat1}})} - \frac{g_{\mathrm{dssat1}}\left(V_{\mathrm{dssat2}}V_{\mathrm{dssat1}} - \frac{V_{\mathrm{dssat1}}^2}{2}\right)}{V_{\mathrm{dssat2}} - V_{\mathrm{dssat1}}}. \tag{34}$$

As indicated in Fig. 10(b), the model can agree with the TCAD well by substituting (31)–(34) into each operating region.

As for the heterojunction structure such as Si/SiGe, according to the deformation theory [41], [42], the band diagram
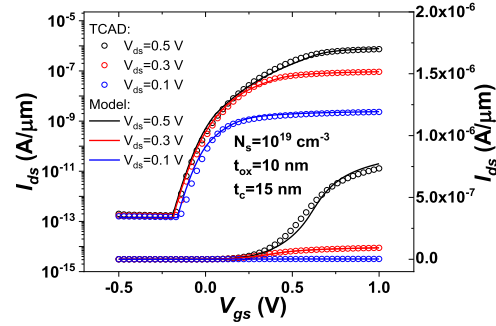
of both carriers' subvalleys is modified due to the strain. Substituting the resulting bandgap and effective mass of carrier into Kane's tunneling theory [18], a revised set of A and B in (12) can be obtained to model the strain effect.

IV. RESULTS AND DISCUSSION

A. Verification of Model on Ge Vertical TFET

In order to validate our model predictions for vertical Ge TFET with different channel thicknesses and V_{ds} biases, the $I_{ds}-V_{gs}$ curves calculated by our model are compared with TCAD simulation as shown in Fig. 11. The V_{ds} is used as the running parameter. The channel thickness is 15 nm. The good agreement between the model and TCAD can be easily observed. Higher values of V_{ds} can reduce the V_{OFF}, because larger V_{ds} induces higher φ_{12}. It should be noted that transistors with thinner channel thickness have higher ON current. For example, when $V_{gs} = 1$ V, $V_{ds} = 0.5$ V, the drain currents predicted by our model are 5.4×10^{-6} A/μm and 7.5×10^{-7} A/μm for transistors with t_c equals to 10 and 15 nm, respectively. The reason is that the channel electric field in the x-direction for the vertical TFET with a thinner channel is larger under the same V_{gs}. Thus, the band-to-band tunneling generation rate is more significant according to (12).

As shown in Fig. 12, the precision of our model is verified with TCAD for transistors with different t_{ox} and different N_s. In Fig. 12(a), Ge vertical TFET with $t_{ox} = 5$ nm has the smallest V_{OFF} and SS, because it has the best gate control ability on the channel electric potential. Fig. 12(b) indicates that transistors with higher source doping concentration have a larger $I_{\mathrm{ON}}/I_{\mathrm{OFF}}$ ratio. The reason can be explained as follows: (26) indicates that larger source doping concentration results in smaller I_{OFF}; φ_{sl} decreases with the increase of N_s. The channel electric field along the x-direction will be larger for transistors with higher N_s. A larger tunneling window is expected as well. Thus, I_{ON} is higher and a larger $I_{\mathrm{ON}}/I_{\mathrm{OFF}}$ ratio can be achieved.

B. InAs Vertical TFET

With a small bandgap of 0.356 eV at room temperature, InAs is widely viewed as a promising material to fabricate TFET to improve the tunneling current. However, the bandgap and the effective mass of the conduction band increase with the reduction of channel thickness due to the quantum effect [13],

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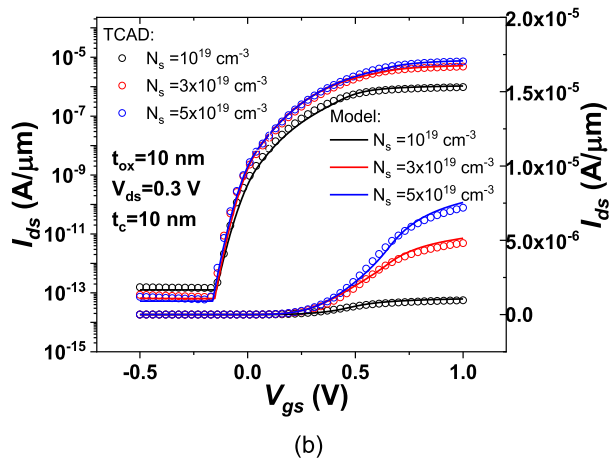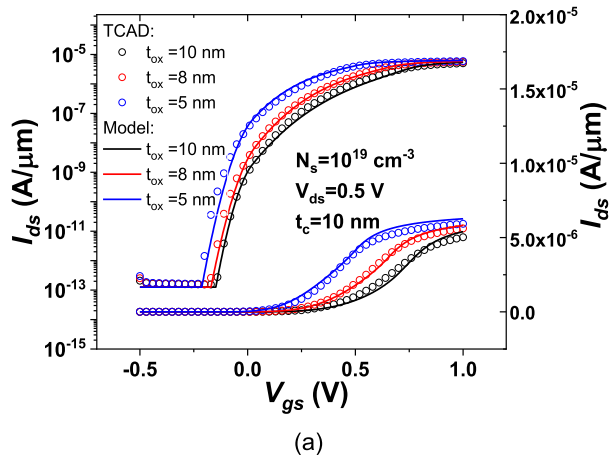CHENG *et al.*: PHYSICALLY-BASED MODEL OF VERTICAL TFET—II

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Fig. 12. Verification of model's results with TCAD simulation in both linear and log scales: (a) different t_{ox} and $V_{ds} = 0.5$ V and (b) different N_s and $V_{ds} = 0.3$ V.

Fig. 13. Verification of model predicted current with TCAD for InAs vertical TFET: (a) $I_{ds}-V_{ds}$ and (b) saturation current I_{dssat}.

which limits the increase of tunneling current. The relationships between channel thickness, the effective mass of conduction band, and bandgap are expressed as [43]

$$m_e^* = a t_c^b + c \qquad (35)$$

$$E_{g.\text{InAs}} = \alpha t_c^\beta + \gamma \qquad (36)$$

where m_e^* is the effective mass of the InAs conduction band, $E_{g.\text{InAs}}$ is the bandgap of InAs, a, b, and c are equal to 0.1944, -1.101, and 0.0205, and α, β, and γ are equal to 1.567, -1.057, and 0.296. The model's results are verified with TCAD simulation for InAs vertical TFET with $t_c = 8$ nm, $t_{ox} = 10$ nm in Fig. 13(a) and good agreement can be observed from the linear to saturation region.

When a transistor is used in the amplifier, a larger saturation current I_{dssat} is preferred. As indicated in Fig. 13(b), the I_{dssat} is extracted from both (34) and TCAD simulation for InAs vertical TFET with different channel thicknesses. It shows that I_{dssat} is the smallest when t_c is equal to 4 nm due to the largest m_e^* and $E_{g.\text{InAs}}$. However, when t_c is larger than 12 nm, the I_{dssat} will decrease with t_c, because the channel electric field along the x-direction becomes smaller. Fig. 13(b) shows that the transistor with $t_c = 12$ nm has the highest I_{dssat}, which is a trade-off between the quantum effect and channel electric field.
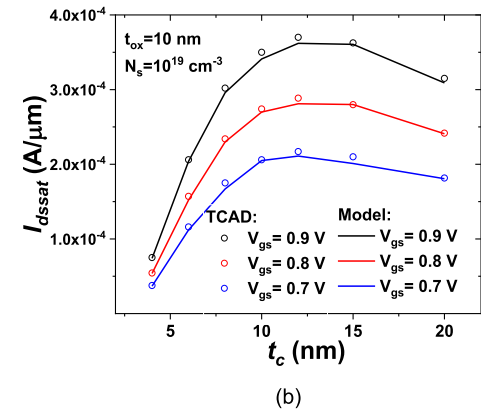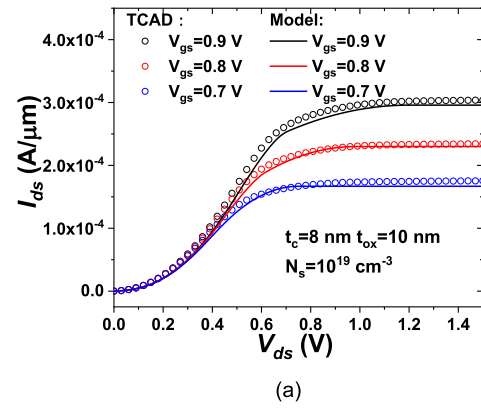
C. Analytical Current Formula

According to (1), the electric field in region 1 along the x-direction is

$$E_{\text{local}} = \frac{\partial \varphi_{1D}}{\partial x} = -\frac{2kT}{q} \frac{\beta}{t_c} \coth\left(\frac{\beta}{t_c} x + \alpha\right). \qquad (37)$$

As stated in Najam and Yu [15], a constant electric field along the x-direction is assumed in the channel

$$E_{\text{locals}} \approx -\frac{2kT}{q} \frac{\beta}{t_c}. \qquad (38)$$

Thus, the simplified expression of the channel electric potential is

$$\varphi_{1Ds}(x) \approx -\frac{2kT}{q} \frac{\beta}{t_c} x + \varphi_{s0} \qquad (39)$$

where $\varphi_{s0} = \varphi_{1D}(x = 0)$. Please note that the β in (39) is calculated by inserting (1) into boundary conditions, which is different from the channel fully depleted approximation discussed in Part I. x_t is defined as the starting point of tunneling as shown in Fig. 14. x_t can be solved based on the following:

$$\varphi_{1D}(x_t) = \varphi_{sl} + \frac{E_g + \Delta E_{vh.s}}{q} \qquad (40)$$

where $\Delta E_{vh.s} = E_v - E_{v.f}$ is the energy difference between the bottom of the valence band and the hole Fermi level in

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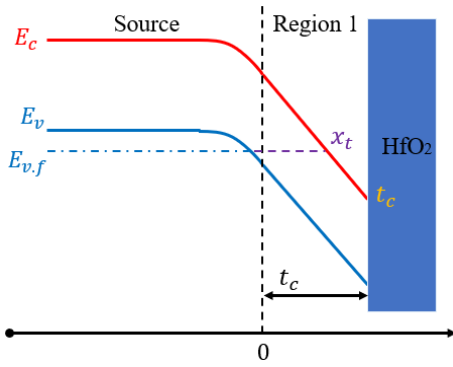
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Fig. 14. Energy band diagram along the source and region 1. x_t is the start point of tunneling in the analytical current model.
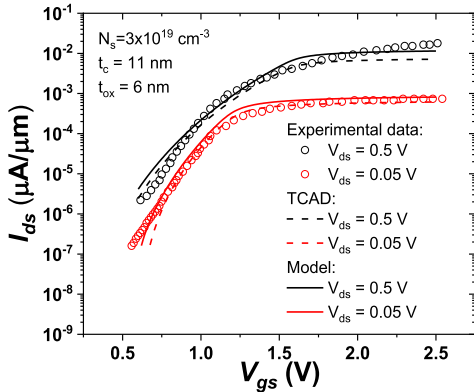

Fig. 15. Comparison between the results of (43), TCAD simulation, and experimental data from Kim *et al.* [11] for the Si TFET.

the source. Thus, x_t is expressed as

$$x_t = \frac{t_c}{\beta}\text{Arcsinh}\left\{e^{\frac{q}{2kT}\left[V_{ds}+\frac{kT}{q}\ln\left(\frac{2\varepsilon_c kT\beta^2}{q^2 n_i t_c^2}\right)-\varphi_{sl}-\frac{\Delta E_{vh,s}}{q}-\frac{E_g}{q}\right]}\right\} - \frac{t_c\alpha}{\beta}.$$

(41)

To simplify the expression of tunneling current, f_s and f_c are deleted from (24). It is assumed that the average electric field E_{av} in the region of $x_t \leq x \leq t_c$ is equal to the constant local electric field E_{locals}. Thus, (24) can be approximated as

$$I_{\text{BTBT}} = qW_1 \int_{x_t}^{t_c} A\left(\frac{E_{\text{locals}}}{E_p}\right)^P \text{Exp}\left(-\frac{B}{E_{\text{locals}}}\right)dx. \quad (42)$$

Substituting (38) into (42) can be analytically integrated as

$$I_{\text{BTBT.}s} = qW_1 A\left(-\frac{2kT}{qE_p}\frac{\beta}{t_c}\right)^P \text{Exp}\left(\frac{Bqt_c}{2kT\beta}\right)(t_c - x_t). \quad (43)$$

As shown in Fig. 15, the results from the simplified current formula are verified with TCAD simulation and experimental data. The model of (43) predicts slightly higher values than TCAD simulation because the average electric field E_{av} is replaced by E_{locals}. This approach underestimates the length of the tunneling path. The calibrated Si tunneling parameters: $A = 4 \times 10^{14}$ cm^{-3} s^{-1} and $B = 1.7 \times 10^7$ V/cm are adopted in the TCAD simulation and model calculation [10]. It should be noted that the ambipolar current dominates the leakage current of line-tunneling TFET [11]. Thus, the off region is not taken into account in Fig. 15.

V. CONCLUSION

In this article, an analytical current model of vertical TFET is proposed based on the previous electric potential model. The model's results are verified with TCAD for transistors with different materials, device geometries, and biases. Good agreements have been observed. The quantum effect on the band structure parameters of InAs in the modeling of vertical TFET is taken into account in this article. It shows that the InAs vertical TFET can achieve the highest drive current with a channel thickness of 12 nm.

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