LASER PROCESSING IN FABRICATION OF INTERDIGITATED BACK CONTACT SILICON HETERO-JUNCTION (IBC-SHJ) SOLAR CELL

by

Jianbo He

A dissertation submitted to the Faculty of the University of Delaware in partial fulfillment of the requirements for the degree of Doctor of Philosophy in Materials Science and Engineering

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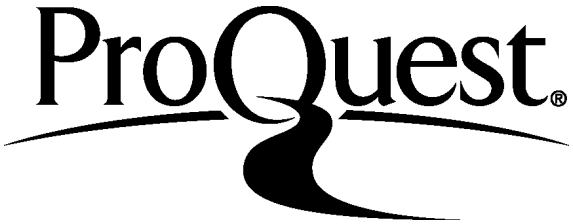

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ABSTRACT

The Interdigitated Back Contact Silicon Hetero-Junction (IBC-SHJ) solar cell combines the advantages of high open-circuit voltage of SHJ device and no front electrical shading of IBC device to achieve the very high efficiency potential. Most recently 25.6% IBC-SHJ device has been announced by Panasonic (formerly Sanyo) which is the highest efficiency of single junction photovoltaic device under one sun condition. However, the p and n regions on the rear side of the IBC-SHJ device usually require multi-steps of photolithography process and/or fine photolithography masks, which is very elaborate and not suitable for large scale industrial production. In order to eliminate or reduce the complexity of IBC-SHJ solar cell fabrication, the application of two laser-based patterning processes, namely laser fired contact (LFC) and laser isolation, are being studied in this thesis.

Laser fired contacts to n-type crystalline silicon were developed by investigating novel metal stacks containing Antimony (Sb). Lasing conditions and the structure of metals stacks were optimized for lowest contact resistance and minimum surface damage. Specific contact resistance for firing different metal stacks through either silicon nitride or p-type amorphous silicon was determined using two different models and test structures. Specific contact resistance values of 2-7 $m\Omega\ cm^2$ have been achieved. Recombination loss due to laser damage was consistent with an extracted local surface recombination velocity (SRV) of ~20,000 cm/s that is similar to values for laser fired base contact for p-type crystalline silicon.

Both direct laser isolation and laser-chemical isolation were studied as rear side patterning technique for IBC-SHJ cells. Shunt resistance > 5,600Ω cm was obtained by direct laser isolation at the cost of significant surface passivation loss and bulk wafer damage. Shunt resistance > 16,000Ω cm was achieved with laser chemical isolation while lifetime of test structure sample still maintain above 1700 us.

The LFC technique together with laser patterning technique has been applied into IBC-SHJ device application. 16.9% IBC-SHJ device has been fabricated and steps of etching steps in photolithography have been reduced and replaced by LFC during process. With mask deposition and LFC technique, 15.2% IBC-SHJ device has been fabricated with no photolithography steps. Finally, p a-Si back IBC-SHJ solar cell was fabricated with laser chemical isolation and LFC. The proof-of-concept device achieved efficiency of 8.8%. The localized base contact technique together with laser patterning technique will enable low cost back contact patterning and innovative designs for n-type crystalline silicon solar cell.

Chapter 1

INTRODUCTION

1.1 An Overview of Solar Cells

Solar Cells are the device that converts the radiation energy, usually from the sun light, into the electrical energy. This phenomenon is called photovoltaic effect which was discovered by Alexander-Edmund Becquerel in 1839 [1]. The first modern silicon solar cell with 6% efficiency was announced by Charpin, Fuller and Pearson in 1954 [2]. The in-depth understanding of p-n junction operation was revealed by Prince, Loferski , Rappaport and Wysocki, Shockley and Queisser [3] [4] [5] [6].

The significance of solar cell was not recognized until recent decades by the increasing concern over the impact on global warming from greenhouse gas primarily CO2. As the human population expands, the need for energy has been unprecedented. To meet the tremendous requirement of energy production, extracting the traditional fossil fuel, including coal, natural gas and oil, is our dominating source of energy for decades, which is accounted for 87% of global energy supply in 2012 [7]. However, the consumption of fossil fuel will inevitably cause emission of greenhouse gas. The accumulation of greenhouse gas emission is predicted to lead to natural disasters such as droughts, floods, sea level rise, glacier melting, and serious disruptions to agriculture and natural ecosystems. Also, the fossil fuel does not have infinite reserves, which take millions of years to develop.

On the other hand, the instance source of solar radiation intercepted by the earth from sun is at the level of 1.8×10^{11} MW [8], which is significantly higher than the current energy consumption level. Also importantly, the manufacturing and operation of solar cell produce little greenhouse gas. Therefore, solar cell has been considered one of the most promising energy sources to eventually replace the conventional fossil fuel.

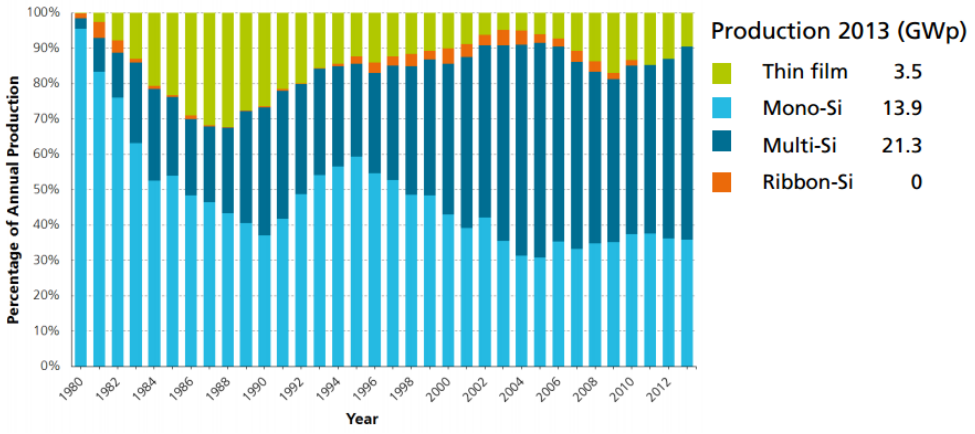

Figure 1.1 PV Production Development by Technology in 2013

Currently, there are two types of commercial available solar cells. One is crystalline silicon based solar cell and the other type is thin-film based solar cell. Figure 1.1 shows the PV production development by technology in 2013 [9]. Crystalline silicon (c-Si) based solar cell contributed 90% of worldwide PV production. The fact that crystalline silicon solar cells are prevailing at both research and production level is as follow: Firstly, c-Si solar cell industry and researchers can inherit knowledge and equipment from the mature microelectronics industry; Secondly, from element point of view, Si is the second most abundant in the earth's

crust and is nontoxic, which are two major concern of $CuInSe_2$ and CdTe thin film based solar cells; Thirdly, the silicon has a suitable band gap of 1.1eV and a reasonable absorption coefficient although it is an indirect bandgap semiconductor. Together with the knowledge from microelectronics industry, the most efficient single junction solar cell is made using single crystal silicon wafer. The combination of the three factors makes crystalline silicon solar cells currently the most suitable technology for large-scale PV systems.

1.2 Advanced Crystalline Silicon Solar Cell Structures

The traditional solar silicon solar cell has suffered several disadvantages: The open-circuit voltage is limited mainly by the passivation on the rear side, where the metal-silicon ohmic contact is formed; it also has to go through several high temperature, > 700 C, processing to form the p-n junction. To solve the above two major concerns, an a-Si:H/c-Si hetero-structure (SHJ) was first suggested in 1974 by Fuhs. [10] The SHJ solar cell is based on an emitter and back surface field (BSF) that are deposited by low temperature growth, usually below 250 C. Intrinsic passivation layers are inserted between doped layers and wafer both on front side and rear side [11]. The first solar cell device based on this hetero structure was reported by Hamakawa in 1983 [12]. The thin layer of hydrogenated amorphous silicon (a-Si:H) could significantly lower the defect density on the crystalline surface by passivating the dangling bonds. The excellent passivation on both sides of the device results in open-circuit voltages over 700 mV. At the same time, the low deposition temperature in SHJ processing reduces the cost and enables potential application of thin wafer in this device structure. Since the late 1980s, Sanyo Inc. of Japan started to incorporate

hetero-junctions into c-Si wafer-based solar cells. [13] Sanyo which was recently acquired by Panasonic, has been the forerunner in SHJ solar cell research field, and presently holds the efficiency record for a hetero-junction device of very impressive value of 24.7% in 2014 [14], compared to the best diffused junction device with 24.7% efficiency [15].

The architecture of SHJ solar cell is as follow. Starting from an n-type c-Si wafer, an intrinsic a-Si:H is deposited by plasma enhanced chemical vapor deposition (PECVD) on both sides of the wafer to passive the free Si surfaces. This is followed by depositing a p-type a-Si:H emitter on the front illumination surface followed by an anti-reflective (AR) transparent conductive oxide (TCO). On the back side, an n-type a-Si:H is deposited on the intrinsic layer serving which serves as back surface field (BSF) followed by TCO/metal layers as back contact. A sketch of an a-Si:H/c-Si hetero-junction solar cell with front and back buffer layers, as developed by Sanyo, is shown in Figure 1.2.

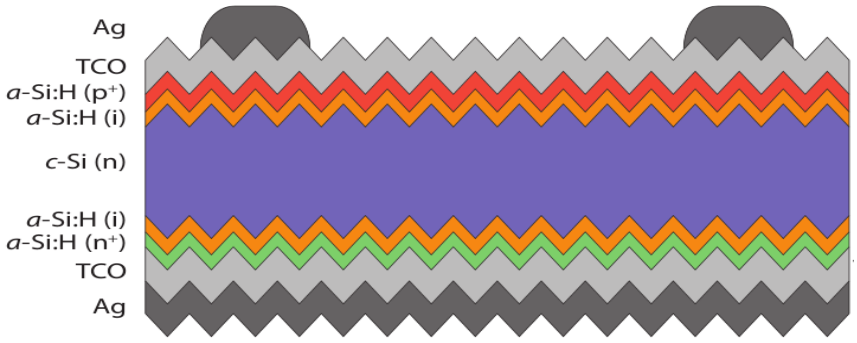

Figure 1.2 Sketch of a HIT solar cell as first developed by *Sanyo Inc.*, Japan. The wafer is n-type. Structure is not drawn to scale. [16]

Compared with traditional crystalline silicon solar cell, the major innovation of SHJ solar cell is in the material part with minimal change in the architecture. The open-circuit voltage for the device is significantly enhanced due to the excellent passivation of intrinsic a-Si:H layer. However, another major drawback of traditional crystalline silicon solar cell is the shadowing loss caused by the electrical grid on the front side of the cell, which was not addressed in SHJ solar cell research. The loss becomes more severe if many cells are interconnected to form a solar module by soldering highly conductive tabs to the front and back of neighboring cells. Moreover, the optimization of front layer of the tradition c-Si solar is often difficult since both the electrical property for front contact formation and optical property for anti-reflection purpose must be considered. To reduce the front shading loss and enhance the short-circuit current, an innovation on the structure of traditional crystalline solar cell was proposed. Interdigitated back contact (IBC) solar cell was first suggested by Schwartz and Lammert in [17] 1975 where, there is no metal grid on the front surface to shadow the sunlight. The junction and the front contact are moved to the rear side of the cell, forming an interdigitated p and n strip pattern, as shown in Figure 1.3, a structure commercialized by SunPower [18]. The front surface of the Si is passivated by forming n+ diffused junction to create a front surface field (FSF), followed by a double-layer of silicon oxide and silicon nitride.. Since there is no electrical grid on front, the optimization of the top silicon oxide and silicon nitride can be optimized as an anti-reflection structure. On the rear side, p+ and n+ regions are patterned by photolithography to form the interdigitated strips. A silicon oxide layer is created on top of both p+ and n+ regions for passivation purpose. Both p and n contacts are formed through the rear passivation layer by array of small openings to minimize the

recombination active areas at the contact. The current efficiency record of IBC cell was held by SunPower, at 24.2% [19]. This was the highest efficiency for commercially available crystalline silicon solar cell until 2014, and is now still the second highest efficient in the world.

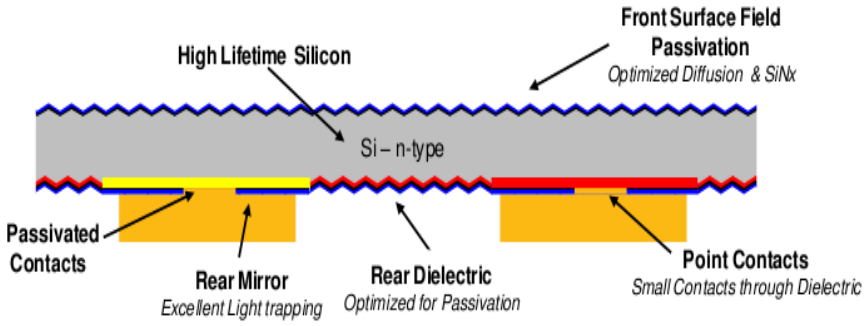

Figure 1.3: Sketch of IBC solar cell developed by *SunPower Corp.*, USA. The wafer is n-type. [18]

In 2007, a new advanced crystalline silicon cell structure was proposed by M. Lu et al [20], combining the benefits of both the SHJ and IBC structures which utilizes all low temperature processing. Figure 1.4 shows the initial IBC-SHJ device structure where the cells were fabricated on 300μm thick n-type polished float-zone (FZ) wafer. Both side surfaces were passivated by intrinsic a-Si:H layer which was deposited by PECVD and an AR stack coating consisting of a indium-tin-oxide (ITO) layer and MgF_2 was deposited on the front side. On the back surface of the wafer, the a-Si:H p-type emitter and n-type base strips were deposited by PECVD where the interdigitated pattern was created by photolithography processing. The proof of concept cell achieved a 602mV V_{oc} and a 26.7mA/cm^2 J_{sc} and a total efficiency of 11.8%. Within a decade the efficiency was increased to over 20% by several research groups [21][22], a Panasonic Electronics which is currently holding the 25.6% record [23].

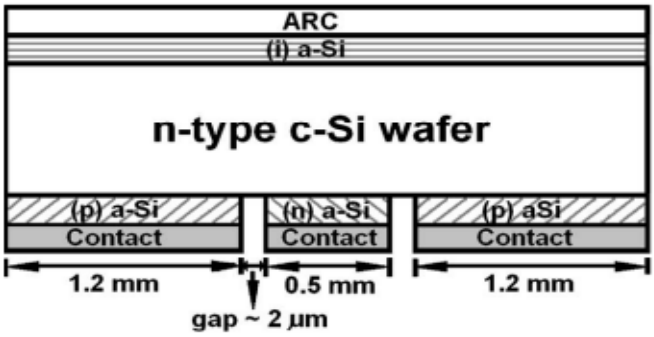

Figure 1.4: Sketch of the 1st IBC-SHJ solar cell fabricated at IEC in 2007 [21]

1.3 Research Motivation of Dissertation

Besides the high efficiency and potential of The c-Si IBC-SHJ cell is the highest efficiency Si device and is the p- and n- regions are deposited by an all low temperature process. However, the rear-side pattern of the p and n regions usually requires multi-steps of photolithography process and/or fine photolithography masks, which is very elaborate and not suitable for large scale industrial production [19][24].

In order to eliminate or reduce the complexity of IBC-SHJ solar cell fabrication, the application of a laser based patterning process is proposed. . The goal of this research is to develop a robust device fabrication process for IBC-SHJ structures using laser processing for base contact formation and base-emitter isolation, as shown in Figure 1.5 This process has fewer fabrication steps and will thus reduce the complexity and cost of IBC-SHJ production. Also, since some manual fabrication steps will be replaced by laser processing steps, the process will be suitable with thin (50 um) Kerfless wafer which can further reduce the cost in material point of view.

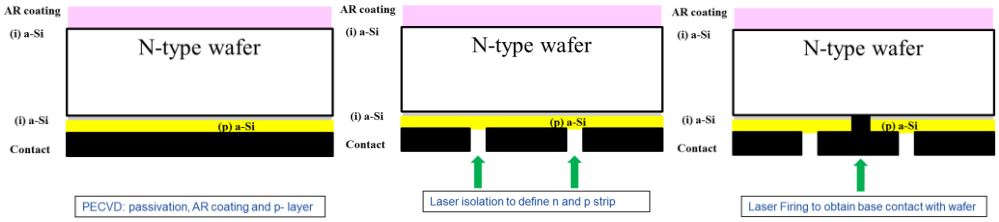

Figure 1.5: Sketch of the IBC-SHJ solar cell with rear side patterning developed by laser processing.

To achieve the goal of this research, two most important objectives are:

1. Rear p-n strip pattern development using laser application instead of photolithography. This step will also serve as an isolation of metal p and n contact. The electrically isolation of the p strip and n strip should not be at the expense of degrading the effective lifetime of the wafer.
2. Laser fired n type base contact. This objective is to obtain base contact on n strip using laser process, namely Laser Fired Contact, where the metal contact on n strip is directly deposited on p type amorphous silicon. The challenge is to get ohmic contact between the metal and n type silicon wafer base while there is p type dopant in the amorphous silicon layer between them. Also, this step has strong potential to create damage on the wafer, so there might a tradeoff between the contact resistance and the area fraction of the laser fired point contact. A unique aspect of this research is the development and application of custom-designed multi-layer metal stacks to replace the typical single metal layer.

The success of this research will reduce the cost and increase the throughout output of IBC-SHJ fabrication in both laboratory and industrial scale.

1.4 Thesis Outline

In this thesis, the focus is the research of laser processing, mainly laser fired contact (LFC) and laser isolation and patterning, and their application in IBC-SHJ as well as in standard SHJ solar cells. In **Chapter 2**, the fundamental physics background of solar cells is presented and discussed with respect to crystalline silicon solar cells along with the basic laser-material interaction principal. In **Chapter 3**, the experimental techniques, including film fabrication, laser processing, material and electrical characterization, are discussed. **Chapter 4** will start with brief introduction of LFC background and history, followed by the development of metal stack for LFC on n-type crystalline silicon. The relationship between laser parameters and LFC yield will be discussed as well by characterizing the electrical and material properties with various test structures. In **Chapter 5**, the trade-off between LFC and passivation loss will be discussed, both by characterizing test structures and applying LFC into standard SHJ solar cells. The device results will also be compared between different blocking layers which lie between the LFC metal stack and passivation layer. In this case the standard SHJ solar cell will serve as a test structure for more complicated IBC-SHJ solar cell. In **Chapter 6** the IBC-SHJ device results will be discussed when LFC was incorporated for the base contact. The rear side pattern will be re-designed and optimized for LFC process. Chapter 7 will discuss laser isolation and patterning, both the direct processing and the laser-assisted chemical etching. The shunt resistance and passivation loss are discussed. The IBC-SHJ solar cell device results will finally be discussed when two laser processing steps, LFC and laser isolation, are both applied in the photolithography-free fabrication. The final **Chapter 8** will summarize the current status of both LFC and laser isolation and evaluate the advantages and

disadvantages of them. The suitability of applying these laser techniques in crystalline solar cells, especially IBC-SHJ will also be discussed. Future work on the laser processing techniques is also outlined.

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Chapter 2

BACKGROUND INFORMATION

2.1 Solar Cell Basics

A solar cell is a device which converts energy from sunlight into electricity [1]. The core part of the device is a p-n junction which can be either a homo-junction or hetero-junction. When the light is absorbed by the bulk of solar cells, the photon with energy higher than bandgap of the material will generate electron-hole pair, which can be separated and collected before recombination by the junction and then dissipate the energy from the contacts into the external load. In practice, most of the p-n junctions in solar cell use semiconductor materials, especially crystalline silicon as the base absorption material.

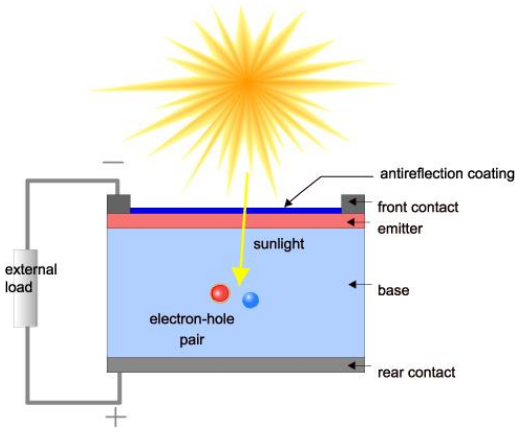

Figure 2.1 Cross section of a solar cell. [1]

2.1.1 Band Gap and p-n junction

The most widely used semiconductor in solar cell is Si which is a group IV element with an indirect bandgap of 1.1 eV in its crystal form. One of the most important properties related with crystalline nature of semiconductor is its energy band structure. The semiconductor bandgap is the smallest amount of energy needed to excite an electron that is bounded to its ground state at valance band into a free state in conduction band where it becomes a free carrier. Band diagram is used to describe the band semiconductor band structure. There are two energy bands in a typical semiconductor the band with higher energy level where free electron resides is called conduction band (E_C) where the band with lower energy level where the electron is bounded is called valence band (E_V). The band gap (E_G) is the energy difference between the valence band and conduction band.

The excitation of the bounded electron from E_V through E_G to E_C will also leave a hole in valence band. A hole is analogous to an electron with opposite charge which moves in the opposite direction in the valence band. Both the electron in the conduction band and the hole in the valence band are equal when considering the conduction in semiconductor and therefore are called free carriers.

Thermal excitation is the dominating electron-hole free carrier pair generation mechanism in intrinsic semiconductor. In this case we have $n_0=p_0=n_i$, [2] and the Fermi level is positioned in the center of E_G. n_0 is the free electrons concentration, p_0 is the free holes concentration. The product of n_0 and p_0 is independent on Fermi level and are given by:

$$n_0 p_0 = {n_i}^2 \quad (2.1)$$

Where n_i is the intrinsic carrier concentration.

Crystalline silicon can be intentionally doped by group-V elements for n-type doping or group-III elements for p-type doping. The additional electrons or holes can be present in the conduction band or valance band because of ionized donor or acceptor impurities, respectively. Figure 2.2 shows the band diagram of n-type doped crystalline silicon where excessive electrons were present in the conduction band. Under thermal equilibrium state, free electrons and holes densities n_0 and p_0 in a semiconductor can be derived using Fermi-Dirac statistics by introducing the Fermi level E_f.

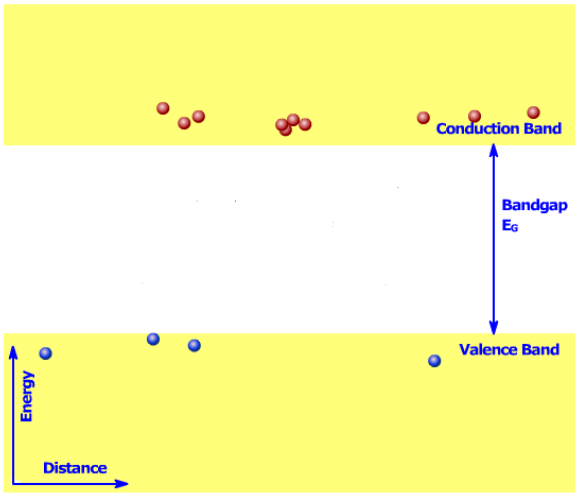

Figure 2.2 Band Diagram of n-type doped crystalline silicon [1]

P-n junction is formed when n-type and p-type semiconductor material are contacted intimately, as shown below in Figure 2.3. The n-type region has a higher electron concentration, while as the p-type region has a higher hole concentration. As a result electrons and holes will diffuse towards the less concentrated region. The diffusion of charged electrons and holes will leave the opposite-charged dopant atom sites behind, which are fixed in the lattice. After the diffusion, positive and negative ion cores are exposed in n and p regions respectively. The positively charged ion in

the n-type region and negatively charged ion in the p-type region will create an electrical field which is called the 'built-in potential' V_{bi}. The region of this potential is called the "depletion region" where the electric field very quickly drives out carriers that diffuse into this region.

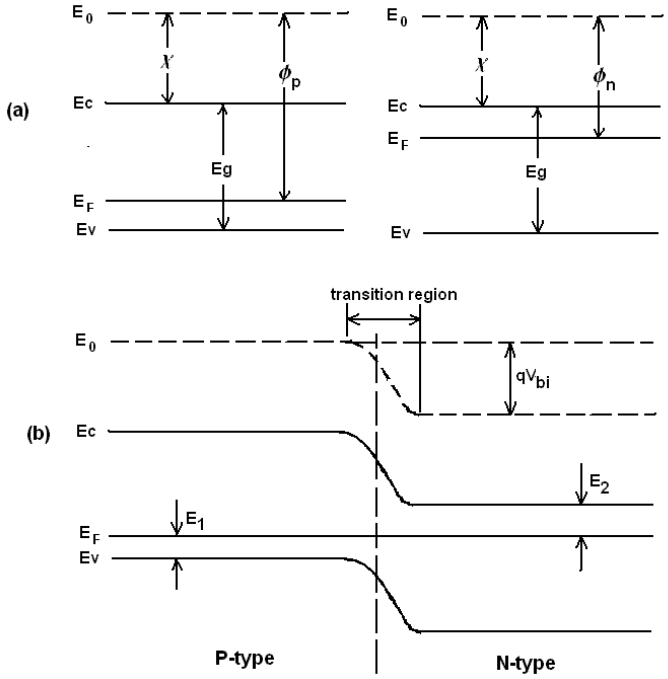

Figure 2.3 (a) Band Diagram of p-type semiconductor (left) and n-type semiconductor (right), (b) junction formation when contacting p and n type semiconductor.

2.1.2 Solar Cell Characteristics

The operation of solar cells can be described by three basic equations which describe the static and dynamic behavior of carriers in semiconductor under external influences which are external electrical field and illumination in the case of solar cell. [3]

The first equation is Poisson equation:

$$\frac{d^2\Psi(x)}{dx^2} = \frac{dE(x)}{dx} = -\frac{\rho(x)}{\varepsilon_s} = \frac{q(n-p+N_A-N_D)}{\varepsilon_s} \quad (2.2)$$

Where $\Psi(x)$ is electrical potential in the depletion region, $E(x)$ is the electrical distribution in the depletion region, $\rho(x)$ is the charge density, ε_s is the dielectric constant. The Poisson equation is used to determine the distribution of electrical potential field within the depletion region.

The second equation is current-density equations: [3]

$$J_n(x) = qn(x)\mu_n E(x) + qD_n \frac{dn(x)}{dx} \quad (2.3)$$

$$J_p(x) = qp(x)\mu_p E(x) - qD_p \frac{dp(x)}{dx} \quad (2.4)$$

Where D_n and D_p are diffusion coefficient for electron and hole, respectively. The current-density equations give the electron and hole current densities, which are the sums of the diffusion current and drift current, under steady-state condition where the external illumination and/ or electrical field is applied.

The third equation is called continuity equations in which the current and carrier density are no longer time-independent: [3]

$$\frac{\partial n(x,t)}{\partial t} = G_n(x,t) - R_n(x,t) + \frac{1}{q}\frac{\partial J_n(x,t)}{\partial x} \quad (2.5)$$

$$\frac{\partial p(x,t)}{\partial t} = G_p(x,t) - R_p(x,t) + \frac{1}{q}\frac{\partial J_p(x,t)}{\partial x} \quad (2.6)$$

$G_n$and G_P are electron and hole generation rate, and $R_n$and R_P are electron and hole recombination rate, respectively. The continuity equations take the time-dependent carrier behaviors which are carrier generation rate and carrier recombination rate into consideration. This set of equations are used to deal with phenomena such as low-level injection, carrier generation and carrier recombination in solar cell device [4].

In reality, it is impossible to analytically solve the three equations for solar cell operation analysis. The practical solution for these equations with more insight into the fundamental physics can be found in [5] [6]. The relationships of current density and external voltage through a solar cell, can be described by the following in a simplified case:

$$J = J_0(e^{\frac{qV}{nkT}} - 1) \quad (2.7)$$

The equation is the well-known ideal diode law. J_0 is the dark saturation current density which is related to the material property, k is the Boltzmann's constant, n is the ideal factor describing how closely the actual solar cell is operating to the ideal diode which is between 1 and 2. When under illumination which is necessary for a working solar cell, the new J-V relationship is simply a superposition of the dark J-V curve together with the light generated current density J_L. With light generated current, the dark J-V curve will be shifted down into the fourth quadrant of J-V plot. The electrical power will then dissipate from the solar cell diode to external load, as shown in Figure 2.4. A working solar cell under illumination will have diode law to become:

$$J = J_0\left(e^{\frac{qV}{nkT}} - 1\right) - J_L \quad (2.8)$$

Where J_L is the light-generated current density.

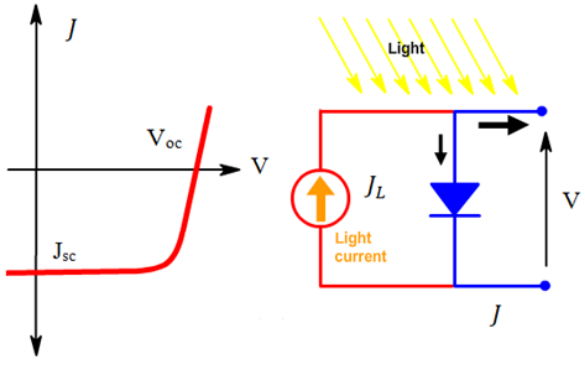

Figure 2.4 J-V curve characteristics of solar cell under external voltage and illumination.

The short circuit current density J_{SC} is the current density flowing across the photovoltaic device when the voltage measured from the device is zero. It is due to the generation and collection of light-generated carriers. Ideally J_{SC} is equal to J_L, which is the largest current density possibly being drawn from the photovoltaic device. The definition of open circuit voltage V_{OC} is the maximum voltage across the device when the current density across the solar cell is zero. Since the output equals to the product of current and voltage, it is obvious that at either open-circuit or short-circuit, the output power is zero. The maximum output power is obtained under the operation condition between the V_{OC} and J_{SC}. The voltage and current density of the solar cell when it is giving maximum output is call V_{mp} and J_{mp}, respectively. The ratio of the product of V_{mp} and J_{mp} over V_{OC} and J_{SC} gives another important parameter called Fill factor (FF), which is defined as:

$$FF = \frac{V_{mp}J_{mp}}{V_{OC}J_{SC}} \quad (2.9)$$

With V_{OC}, J_{SC} and FF, the conversion efficiency of solar cell η is usually expressed as follow:

$$\eta = \frac{FFV_{OC}J_{SC}A}{P_{in}} \quad (2.10)$$

Where A is the area of the solar cell, P_{in} is the input power from illumination.

2.1.3 IBC-SHJ Solar Cells

Silicon heterojunction (SHJ) solar cell exhibits the potential of achieving the same or even higher conversion efficiency than traditional diffused homojunction solar cell without the high temperature process and high recombination area at the contact. The SHJ solar cell is based on an emitter and back surface field (BSF) that are

produced by low temperature growth of ultra-thin layers of hydrogenated amorphous silicon (a-Si:H) on both sides of a c-Si wafer, where electrons and holes are photo-generated. With the wider band gap of ~1.7eV and the hydrogen, a-Si:H is able to passivate the crystalline surface thus achieve high open-circuit voltage.

Besides the benefit of passivation brought by heterojunction, the difference of bandgap, electron affinity and work function of the two different materials can also play important role in solar cell operation. When the system is in equilibrium state after p and n-type materials contacting, discontinuities on both valence band and conduction band edge arise due to the difference in electron affinity χ and bandgap E_g, as shown in Figure 2.5. At the valence band edges, the spike shaped band offset will hinder the hole transport. In n-type SHJ solar cells valence band offset is undesirable since holes are minority carriers. This detrimental effect could be relieved or solved when the buffering layer is properly tuned with thickness and band gap so that minority carrier could tunnel through [7].

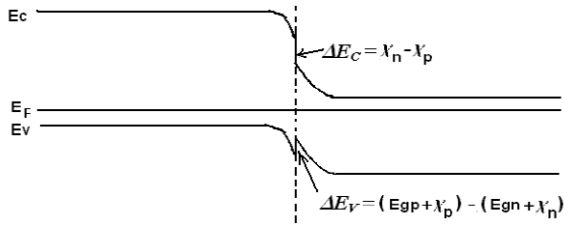

Figure 2.5 Band diagrams of a heterojunction [7]

As for Interdigitated Back Contact (IBC) solar cell, its architecture is quite unique since both p^+ and n^+ region and their contacts are on the rear surface, leaving the front surface free of any metal grids. Without any optical shading from grids, and the need to balance the front layer optimization between anti-reflection and ohmic-

contact, the short-circuit current can be greatly improved. On the rear side, both positive and negative contacts coverage will be increased. As the result, the standard trade-off between reflection loss and series resistance loss in front contact case can be avoided. At the module level, with both contacts on the same side, IBC solar cell will simplify interconnecting of cells and reduce the material cost in module packaging process. [8]

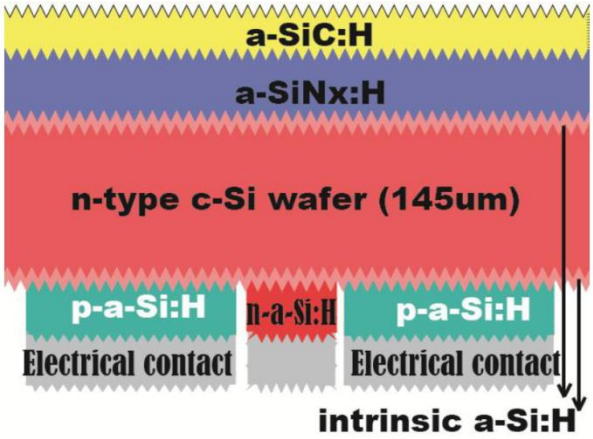

Figure 2.6 Schematic of a practical IBC-SHJ fabricated at IEC.

However, similar as the conventional front junction diffusion solar cell, IBC solar cell junctions and back surface field are formed in high temperature diffusion process, and the recombination at the contact area is inevitable. To address the disadvantage the SHJ concept was merged into IBC solar cell, and IBC-SHJ solar cell concept is proposed. The IBC-SHJ solar cell has similar architecture with the traditional IBC solar cell, but all the diffusion layers are replaced by a-Si:H based thin layers which are deposited under low temperature (<300 C). Both front and rear surfaces are passivated with intrinsic a-Si:H layers. An anti-reflection stack layer of a-SiN_x:H and a-SiC_x:H are deposited on top of the i-a-Si:H layer to enhance light

absorption together with the texturing of silicon wafer. The positive fixed charge in a-SiN_x:H will also create a front surface field to enhance the front surface passivation. On the rear side, the interdigitated emitters and back surface fields are formed by p-a-Si:H and n-a-Si:H thin film, respectively. Finally both p and n contact strips are deposited on top of p-a-Si:H and n-a-Si:H layers, respectively.

2.2 Laser Processing in Solar Cells

Advanced laser processing is being used at the forefront of IC manufacturing to enable fabrication of devices that go beyond the physical limits set by traditional processing. The techniques used are accurate, fast and cover a wide range of processes. Laser processing is used in all aspects of fabrication including: photomask writing, photomask inspection, bare wafer inspection, metrology, wafer dicing, marking, trimming, micro-via drilling and fabricating flat panel displays [9]. The success of laser processing applications in the IC industry suggests that such techniques should be considered in the effort to reduce manufacturing costs and to improve electrical efficiency of solar cells.

The laser processes currently used in solar cell fabrication can be classified in five basic categories; (1) cutting, (2) scribing, (3) drilling, (4) alloying and, (5) doping. Most of the laser processing used in solar cell fabrication to date has been achieved using pulsed lasers rather than the continued wavelength laser [9].

2.2.1 Laser Basics and Laser Optics

The word laser is an acronym for Light Amplification by Stimulated Emission of Radiation. A laser is a device that amplifies light and produces a highly intensified

and collimated beam with very narrow wavelength distribution. As shown in Figure 2.7, a laser typically has an optical resonator which is consists of an amplifying medium and two mirrors on both ends. The stimulated emission occurs within the medium, and is then fed back into the medium by the two mirrors for continued growth [10]. According to the type of medium material, there are several types of laser, such as gas laser, chemical laser, dye laser, semiconductor laser and solid state laser. Laser can also be classified by its operation mode, either in continuous mode or pulsed mode. A continuous wave laser delivers beam with constant power over time, while pulsed laser delivers beam with a time-dependent power profile.

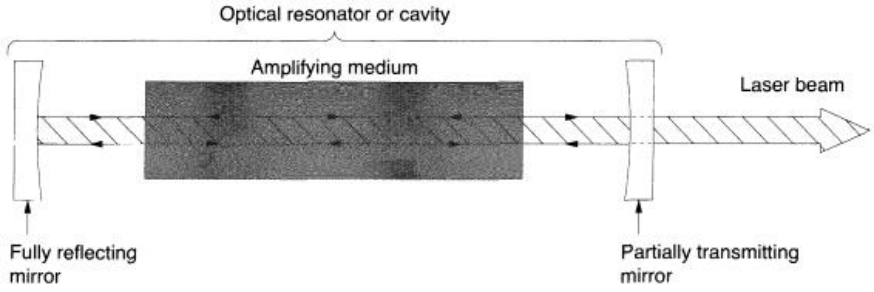

Figure 2.7 Schematic of a typical laser

Solid state lasers with pulsed operation mode are the mainstream in the semiconductor and photovoltaic industry because of its low cost, ease of construction and wide range of output power, from 0.04 watts to 600 watts [11]. Most solid state lasers use neodymium-doped yttrium aluminum garnet (Nd:YAG) as laser active medium which feature pulse repetition frequencies range from several Hz up to 100 kHz. The laser pulse energies Ep usually range from the μJ to the mJ regime and the pulse durations from the low ns to the μs regime.

In the ideal case, a laser source operating in TEM00 mode, has a beam profile of Gaussian distribution [11]. Thus, the Intensity distribution I(r) could be described as follow:

$$I(r) = I_0 e^{-2r^2/w^2} \quad (2.11)$$

Where I_0 is the maximum intensity related to laser power P and w is the laser beam radius.

I_0 could be expressed as follow:

$$I_0 = \frac{2P}{w_0^2} \quad (2.12)$$

Where w_0 is the minimum beam radius at the beam waist.

Another important parameter is the divergence θ which describes how fast the beam radius expands along its pathway:

$$\theta = \frac{w_0}{z_0} \quad (2.13)$$

Where z_0 is called Raleigh length. The Raleigh length is the length from the beam waist to where the beam radius expands to $\sqrt{2}w_0$. The schematic of the propagation of a Gaussian laser beam is shown in Figure 2.8.

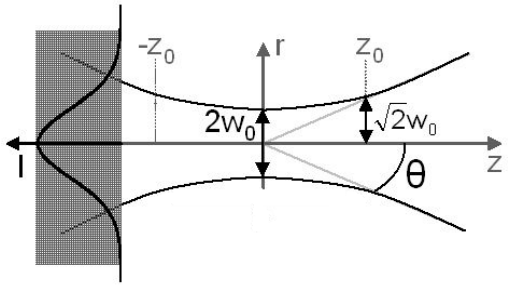

Figure 2.8. Propagation of laser beam with Gaussian distribution.

2.2.2 Laser Absorption in Materials and Materials Response

When laser hits the material surface, the reflection and absorption take place simultaneously, just like any type of light illumination. The reflection R at the material surface and laser intensity, I, can be described by the familiar equation [10]:

$$P = \frac{(n_1 - n_2)^2}{(n_1 + n_2)^2} \quad (2.14)$$

Where n_1 and n_1 are index of refraction of air and material, respectively;

$$I(z) = I_o e^{-\alpha z} \quad (2.15)$$

Where α is the material's absorption coefficient at certain wavelength and temperature.

The mechanism of laser absorption could vary from materials. In general, a photon will couple either with an electronic state or a vibrational state in the material depending on the wavelength of the laser. In insulators and semiconductors, the absorption of laser photon mostly associates with inter band transitions (electron from E_V to E_C) or inter sub band transitions (electron from E_V to E_V or E_C to E_C). In the case of metal where are mostly interested, the photons will be absorbed by electron gas [10]. These excited electronic states can then transfer energy to lattice phonons if the pulse width is long enough. The time for the excited electronic states to transfer energy to nearby lattice depends on the material type, and is defined as thermalization time. In the case of metal, the thermalization is done by electron scattering. Therefore the thermalization takes place by electron scattering. The lifetime of the excited electron τ_{ee} could be expressed by Fermi liquid theory [10]:

$$\tau_{ee} = \tau_0 \left(\frac{\varepsilon_F}{\varepsilon - \varepsilon_F}\right)^2 \quad (2.16)$$

Where τ_0 is at the order of fs and is determined experimentally by time-resolved photoemission. ε_F is the Fermi Energy and ε is the energy of the excited

electron. The lifetime of excited electron is a very important parameter in choosing the pulse duration of laser for particular type of laser processing, as different pulse duration could result in completely different material response.

If a laser pulse is shorter than the lifetime of an excited electron, the lattice temperature is completely de-coupled from the electron temperature. If sufficient energy is given in a short pulse, the electron gas could be heated up and bonding is loosened enough for the material to vaporize, without having enough time to heat up the adjacent lattice.

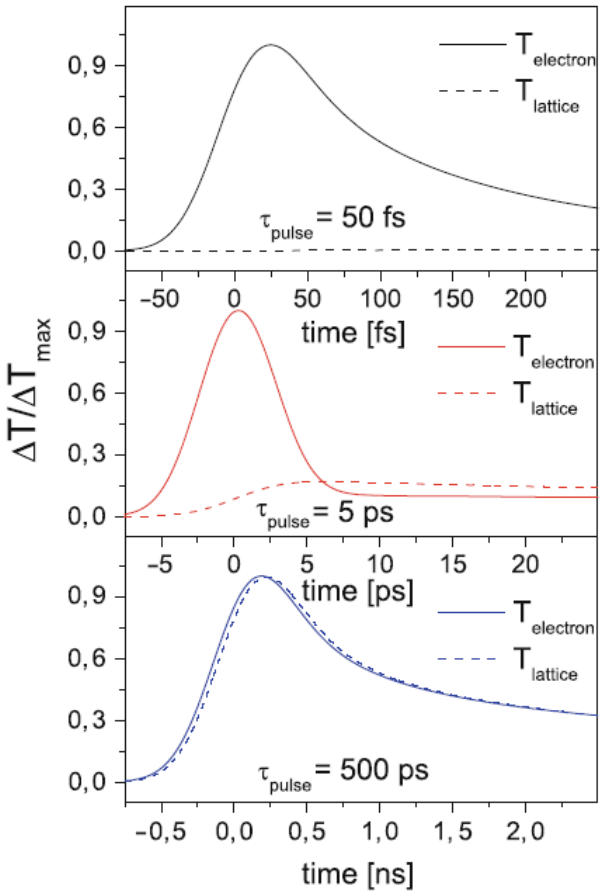

Figure 2.9 Electronic and lattice temperature profile of copper irradiation by laser with different pulse duration. [10]

When the laser-induced excitation rate is lower than or similar with thermalization rate, which means the pulse duration is comparable or longer than the thermalization rate, the details of the transition of thermalization of the excited states is not important. The excited electron has sufficient time to transfer the energy to the adjacent lattice. Therefore, the absorbed laser energy can be considered as being directly transformed into heat energy. Such processes are photo-thermal and the material response can be treated with a thermal only method. Laser processing of metals with laser pulse duration larger than nanosecond is typically characterized by photo-thermal mechanisms.

In figure 2.9, the electronic and lattice temperature of copper are plotted under different pulsed laser radiation. It is obvious that laser pulse duration comparable or shorter than τ_{ee} is desirable during laser isolation process which requires precise removal of top metal layer without a significant heat affected zone (HAZ). On the other hand, an optimized LFC require minimum surface passivation loss or wafer damage while dope the silicon surface preferably by dopant diffusion. Therefore, a longer pulse laser compared to laser isolation is desired for LFC work. The details of laser isolation and LFC will be discussed in later chapters.

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Chapter 3

EXPERIMENTAL TECHNIQUES

Experimental techniques and facilities used in the study of this thesis will be introduced in this chapter, including the fabrication techniques for preparing solar cells; the material and electrical characterization methods used to characterize related test structures; and the testing and analysis tools to investigate device performances.

3.1 Fabrication

Various techniques can be used to fabricate a-Si/c-Si heterojunction solar cells. In IEC, plasma enhanced chemical vapor deposition system (PECVD) is used for growing all a-Si and other Si based amorphous films (a-SiN_x and a-SiC). Electron-beam deposition system is used for deposition of metal contact for solar cells, and metal stack layers for LFC studies, and sputtering is used for the deposition of ITO film on HIT solar cells. [2] Laser processing, including laser firing and laser isolation, is performed using Nd-YAG solid-state pulse laser system.

3.1.1 Plasma Enhanced Chemical Vapor Deposition (PECVD)

PECVD is a process used to deposit thin films from a gas phase to solid phase on substrates. Typically, the plasma is generated by Radio Frequency (RF, 13.56MHz) or direct circuit (DC) glow discharge between two electrodes, the spacing between which is filled with processing gas mixture [1]. The processing gas mixture is converted by the plasma into reactive radicals, ions, neutral atoms and molecules, and

other highly excited species. These ionic, atomic and molecular fragments are accelerated by the potential between the electrodes and interact with substrate surface. After the plasma of the processing gases strikes, chemical reactions are triggered. The system has multiple chambers to prevent cross contamination of films deposited under different conditions and 'flipper' that permits deposition on both sides of a wafer without breaking vacuum during the depositions. PECVD serves as one of the most important fabrication tools in this thesis. Amorphous silicon (a-Si) layers doped p or n type serve as emitter or contact layers and are deposited on silicon wafer by PECVD. Un-doped intrinsic a-Si layers serve as buffer and passivation layers along with a-SiN_x as passivation/anti-reflection layer. [2]

Figure 3.1 illustrates the design of PECVD reactor used in this thesis [2]. Processing gas mixture comes into the chamber from the bottom and pumped out through a turbo pump backed by a mechanical process pump [2]. The substrate carrier and chamber walls are grounded which means electric field is formed in the region between the powered electrode and substrate carrier. The dissociated reactive species from the gas mixture will be accelerated by electrical field or diffuse onto the bottom surface of substrate, for charged species and for neutral species, respectively. The flow rate of each processing gas is controlled by a mass flow controller (MFC), and the chamber pressure is monitored by pressure gauges and adjusted by the throttle valve. Two heaters which are on the top and the bottom of substrate carrier control the substrate temperature up to about 400^oC for our system.

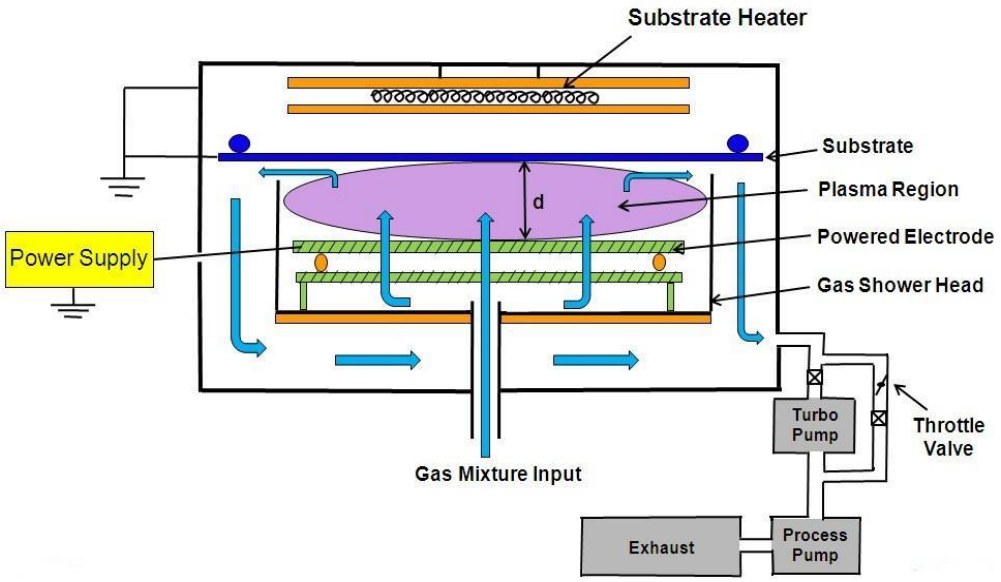

Figure 3.1 Schematic cross-section of a PECVD reactor in IEC. [2]

The PECVD system is a multi-chamber (MC) in-line system at IEC, with four reaction chambers and two load locks. Each of the four reaction chambers has the similar structure as shown in Figure 3.1, and a picture of MC system is shown in Figure 3.2. Intrinsic, p-type, and n-type materials are deposited in different chambers of the MC system to prevent cross contaminations. It is also equipped with a sample flipper in one of the load locks, which enables continuous depositions on both sides of substrate without unloading the samples and breaking the vacuum. This will prevent surface contamination during the vacuum break. [2]

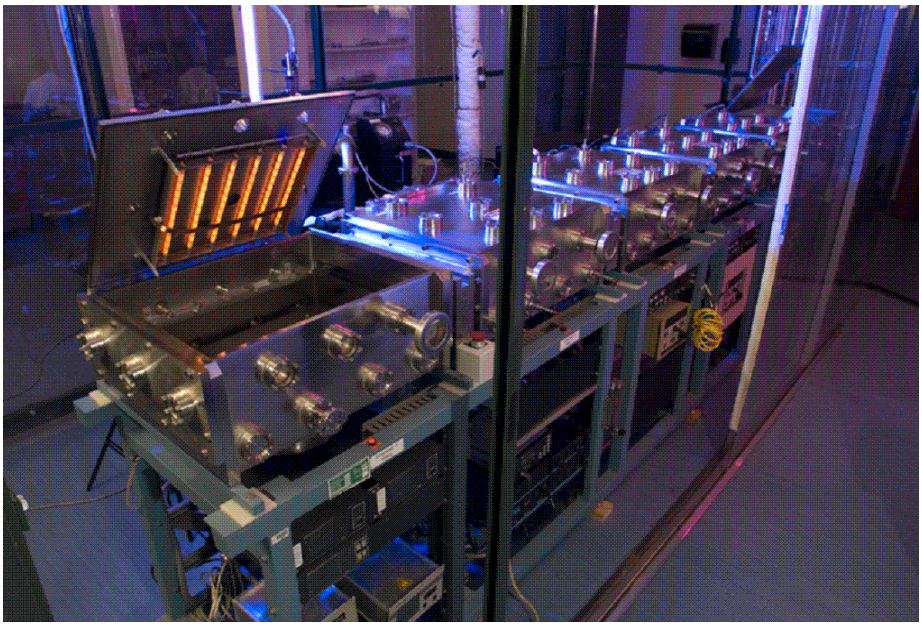

Figure 3.2 Multi-chamber (MC) in line PECVD system at IEC [2]

3.1.2 Physical Vapor Deposition (PVD)

Physical Vapor Deposition (PVD) is a variety of vacuum methods used to deposit thin films by the condensation of vaporized form of the desired film materials onto the substrate. Rather than the involving of chemical reaction in PECVD, PVD involves only physical processes such as high temperature vacuum evaporation or plasma-assisted sputtering in this research. [2]

Electron-Beam (E-Beam) Evaporation

Electron Beam Evaporation is a type of high vacuum PVD in which a target anode is bombarded by an electron beam produced by an electron gun. The e-beam heats the ingot material up to its melting point. The atoms from the target ingot will then transform into a gas status and then precipitate into solid form on the surface of substrate [3]. The deposition rate of E-beam evaporation can vary widely from 0.1 μm

/min to 100 μm/min. In the e-beam system at IEC, the electron beam is created by a filament, and directed and focused onto the target ingot by a permanent magnet. Sample holder can accommodate up to 9 pieces of 1 inch by 1 inch substrates and the thickness of the film is monitored by a crystal monitor during the deposition. This system is used for the deposition of aluminum (Al), silver (Ag) and nickel (Ni) contacts for solar cells, as well as the deposition of titanium (Ti) and antimony (Sb) for LFC studies. Metal masks are used to cover the substrate surface during e-beam depositions to define the contact grids for front heterojunction (F-SHJ) solar cells and the LFC test structures.

Sputtering Deposition

Sputtering deposition is a widely used method in semiconductor industry to deposit thin films. The advantage of sputtering over Ebeam is it usually will introduce less radiation damage since the target will not be heated up significantly. The sputtering system consists of an evacuated chamber, a target and a substrate holder. The inert gas Argon filled in the chamber is struck with RF electrical field and ions are formed. The electric field inside the chamber accelerates ions accelerated towards the target, scattering the target atoms in all directions. The sputtered species will travel through space until it strikes and condenses on the surface of substrate. In this work, a RF sputtering system is used to deposit ITO coating on the front surface of F-SHJ solar cell for anti-reflection.

3.1.3 Photolithography

Although one of the major motivations of this Thesis is to reduce or eliminate the photolithography process in IBC-SHJ solar cell fabrication, it is still a process

extensively used in the rear side patterning in this research. As ultra-violet (UV) light shines on a photo mask with a desired pattern, it transfers the pattern to a light-sensitive chemical photoresist on the substrate. After a series of chemical etching, the material under the PR will be engraved with the exactly same pattern. There are two types of photoresist: positive and negative. For positive PR, the exposure process changes the chemical structure of the PR so it becomes soluble in the PR development step. The exposed positive photoresist is then lifted off by a developer solution. After lift of step the underlying material will be exposed without PR covering. On the other hand, the negative PR remains on the surface after exposure process since the exposure makes negative photoresist difficult to dissolve. After developing, The unexposed area will be removed and leaving the underlying material exposed. [2]

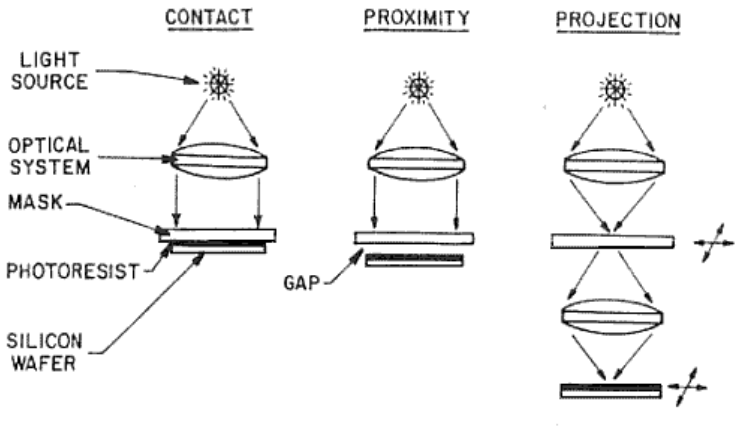

Figure 3.3 Contact, proximity and projection methods of photolithography [2].

Figure 3.4 Karl Suss MJB Standard 3 mask aligner used in this thesis.

3.1.4 Laser System for LFC and Laser Isolation

A laser is a device that amplifies light and produces a highly intensified and collimated beam with very narrow wavelength distribution. A solid state Nd-YAG pulse laser scribing system is used at IEC to perform all laser related work, including laser fired contact and laser isolation. The maximum output power of the system is 2 W, with a transverse magnetic 00 (TM00) Gaussian distribution of pulse profile. The system features 7 ns/ 5 ns pulse duration for 532 nm/ 1064 nm laser wavelength respectively. The spot size is set to be 30 um and frequency could be varied from 1 kHz to 20 kHz. Also we have an external collaborator, IPG Phonics (former JPSA), who has extensive selection of laser systems regarding pulse duration, laser wavelength, frequency and spot size, etc. A wide range of lasing conditions for LFC and laser patterning has been investigated at IPG for optimization.

3.2 Optical and Material Characterization

3.2.1 Optical Microscope (OM)

Optical Microscope is a type of microscope uses light visible to human eyes and a set of optical lenses to magnify images of sample area with interest. It is the oldest design of microscope, but the simplicity of use make OM a very helpful to surface morphology characterization where the image is captured using a digital camer couple to a computer. The OM used in this thesis is Olympus Vanox Microscope with Digital Camera for initial examination of the morphology of LFC and laser isolation.

3.2.2 Scanning Electron Microscopy (SEM)

Unlike traditional OM, the SEM utilizes high energy electrons to form sample image. A beam of electrons is produced inside the chamber of the microscope by heating a metal filament usually made from Tungsten or Lanthanum Hexaboride. This beam is attracted through the anode, condensed and then passing through the scanning coils and finally focused as a very small point on the sample of interest by the magnetic objective lens. The scan coils are energized by high voltage and creates a magnetic field, which will bend the beam at operator's will in a controlled pattern. Image arises from secondary electrons emitted from specimen surface by collision of primary beam electrons with specimen matrix. A positively charged wire cage is used to enhance the number of secondary electrons reaching the scintillator. [4]

Usually, the magnification of SEM is determined by the acceleration voltage, the size of electron spot and the interaction volume. Under optimum conditions, resolution of ~ 1 *nm* is attainable, which corresponds to the magnification of 300,000 times. In this thesis, SEM is used to study the surface morphology of LFC and laser isolation.

3.2.3 Focused Ion Beam (FIB)

Focused ion beam, (FIB) is a technique mostly used in semiconductor industry and materials science for fine sample analysis, material deposition, and most importantly, ablation of materials. An FIB setup is usually bundled with a SEM. Unlike the SEM which uses a focused beam of electrons, an FIB setup uses a focused beam of ions to image the sample. FIB system can equip with both electron and ion beam columns which allows the same area being examined by both SEM and EDS

In this study the Zeiss Auriga 60 dual beam FIB-SEM has been used. The facility provides high resolution solutions for nano-tomography, 3-D imaging and analysis, lamellar and thin foil preparation, and nano-patterning. Additionally, the view-and-slicing capability of the FIB-SEM extends the opportunities to correlative tomography. The cross-section SEM image of LFC spot taken with FIB-SEM for bulk wafer defect analysis will be presented in later chapter.

3.3 Electrical Characterization

3.3.1 Energy Dispersive X-Ray Spectroscopic Analysis (EDX)

Energy-dispersive X-ray spectroscopy is also called energy dispersive X-ray analysis or energy dispersive X-ray microanalysis. It is an analytical tool to characterize the elemental distribution within sample. A high-energy beam of charged particles (electrons and protons) or X-rays is striking onto the sample of interest to excite the characteristic X-ray from the element to be tested. The incident particles or X-ray is able to eject an electron from an inner shell leaving electron hole behind. An electron from high energy orbital then falls back into the electron hole. The energy emitted during the fall back equals to the difference between higher-energy and the lower energy orbital, which is called characteristic X-Ray. The quantity and energy of

the characteristic X-rays radiating from the sample will be measured by an energy-dispersive spectrometer. [5] As the energy of the X-rays which equals to the difference between two orbitals is uniquely linked to the atomic structure, the measured quantity and number of X-Ray will reveal the elemental composition of the sample of interest. to be measured [5].

In this Thesis, the EDX is mainly used to characterize the compositional property of LFC spot with different metal stack design under different lasing condition. The the compositional distribution within laser isolation trench is also studied by EDX.

3.3.2 Effective Minority Carrier Lifetime Measurement

Minority carrier lifetime is a measure of how long a carrier will stay active before recombination. The lifetime determines the steady state populations of electrons and holes, i.e. the separation of quasi-Fermi levels and hence V_{oc} of the solar cell [6]. In this study, high quality Float Zone (FZ) wafers with bulk lifetime exceeding 5 ms are used and therefore the measured effective lifetime is mainly determined by quality of its surface passivation. Therefore, lifetime measurement is crucial in this Thesis in studying the surface passivation, the surface damage caused by laser processing and performance of a solar cell. The measured lifetime is usually called effective lifetime, $\tau_{eff,}$ which can be decomposed to bulk (τ_b) and surface (τ_s):

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_b} + \frac{1}{\tau_s} \qquad (3.1)$$

Two basic methods to test effective lifetime are: transient decay method, also called photo-conductance decay (PCD); and the quasi-steady-state photo-conductance method (QSSPC). For PCD method, the photo-generation is terminated abruptly.

There will be no current flowing from the device. Therefore the rate of carrier density change is equal to the recombination rate:

$$\frac{d(\Delta n)}{dt} = -\frac{\Delta n}{\tau_{eff}} \qquad (3.2)$$

If *dn/dt* and the excess carrier concentration Δn are measured, the effective lifetime τ_{eff} can be determined by equation (3.2). For QSSPC method, the illumination terminates slowly which is a quasi-steady process, so the QSS conditions prevail within the semiconductor, and effective lifetime is:

$$\tau_{eff} = \frac{\Delta n(t)}{G(t) - \frac{\partial n}{\partial t}} \qquad (3.3)$$

where *G(t)* is the generation rate, which is measured using a photo-detector.

For both the above testing methods, the excess electron concentration Δn is determined by measuring the conductance change of the c-Si wafer with illumination and time. The excess photo-conductance for a wafer of thickness *W* can be measured in a contactless fashion by using an inductor and expressed in terms of *Δn*:

$$\Delta\sigma_L = qW(\mu_n + \mu_p)\Delta n \qquad (3.4)$$

where μ_n and μ_p are electron and hole mobility respectively.

The range of Δn can be from 10^{13}cm^{-3} (low injection level) to up to 10^{17}cm^{-3} (high injection level). The specific Δn of 10^{15}cm^{-3} is usually reported since this number is approximately the excess carrier density in c-Si solar cells under general operation condition. Under QSSPC condition, the separation between electron and hole quasi-Fermi levels, i.e. V_{oc} of the cell can be derived since Δn can be measured at steady state [7]. This V_{oc}, as derived from lifetime measurement, is called implied V_{oc} (iV_{oc}) which is a very important indicator of the quality of surface passivation and is usually very close to actual V_{oc} of the finished device if there are no major problems of the p-n junction and contact. In other words, the implied V_{oc} is the highest V_{oc} a

device could possibly achieve limited by surface passivation. This is very important tool to quantitatively analyze the laser induced damage in both LFC and laser isolation process. In this Thesis, all effective lifetime measurements, including both PCD and QSSPC methods, were measured using commercially available Sinton WCT100 instrument, and Figure 3.5 shows the picture for the instrument in IEC. [2]

.

Figure 3.5: Sinton WCT100 tester for effective lifetime measurement in IEC. [2]

3.3.3 Current-Voltage Analysis with Temperature Variation

The most important and straightforward characterization of solar cell performance is the measurement of current density-voltage (J-V) curve under illumination. An artificial light source that simulates the sunlight shines on the solar cell meeting the following conditions: (a) Air mass 1.5 spectrum (AM1.5) for

terrestrial cells and Air Mass 0 (AM0) for space cells and (b) Intensity of 100 mW/cm^2 [8]. As scanning the voltage, the current between the probes is recorded for each applied voltage. During the measurement, the solar cell is cooled with fan or water, and cell temperature is monitored with thermometer.

Besides the device J-V measurement, the J-V characteristics of various test structures especially the LFC test structures are also measured under different temperatures by using a Linkam Cryostat attached to the J-V tester, which serves as the temperature controller. The Linkam Cryostat system is a temperature stage with liquid nitrogen pump and temperature controller to cool down or heat up samples for electrical characterization. By testing the J-V characteristics of LFC contact under different temperature, the contact mechanism and the local doping level could be qualitatively studied [9]. The details of the temperature variation J-V measurement will be discussed in later Chapter.

3.3.4 Electroluminescence Mapping (EL)

In Electroluminescence measurement, current is fed into a solar cell, which is basically a diode. Both non-radiative and radiative recombination occur as the excessive carriers are injected, and only the light emission from the radiative recombination will be sensed using an external detector. [10] The non-radiative recombination usually happens at defects and in this studies, the laser induced defects. The technique requires electrical contact and so can only be used once the metallization has been applied which means a complete cell is required. However, EL is able to provide data about the area related uniformity of solar cells with high spatial resolution (< 20 um) with short period of time compared with other mapping

techniques such as LBIC. In this study the EL mapping is used to qualitatively determine the recombination area caused by LFC on FJ-SHJ solar cells.

3.3.5 Spatially Resolved Photoluminescence (PL)

Unlike EL, Photoluminescence (PL) is light emission from material after the absorption of photons rather than carrier injection. This means PL is a contactless method to characterize the electronic structure of materials. Therefore, any test structure without a junction or a solar cell at any stage of fabrication could be tested. Camera-based photoluminescence imaging is used in this study for the fast spatially resolved analysis of the quality of surface passivation quality and inhomogeneity, especially caused by LFC and laser isolation.

3.3.6 Laser Beam Induced Current Scanning (LBIC)

LBIC has been widely used to analyze processing techniques and related device performance including photosensitive transistors and diodes besides solar cells. LBIC mapping is a technique by which only a small area (beam size ~ 50μm x 50μm) of the device is illuminated and the resulting photo-generated carriers are measured, therefore localized electronic defects can be detected. Usually, the incident Laser beam is modulated into a pulsed (AC) signal through a mechanical chopper, so that it will be able to measure the photo-generated current while the sample is being illuminated by a constant light bias. At IEC the LBIC imaging system utilizes a moving laser beam and fixed the sample position. This designed has been able to maximize scan areas, which range from areas larger than 1 square meter to as small as 100 square microns. Also the LBIC system in IEC can provide a DC voltage bias from -5 V to +5 V as well as a DC bias illumination that can range from greater than 1 sun

to 0.01 sun. In the device analysis IBC-SHJ solar cell with LFC on n-strip, LBIC is used to measure the current collection uniformity around the LFC spots.

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Chapter 4

LASER FIRED CONTACT ON N-TYPE CRYSTALLINE SILICON

4.1 Introduction

4.1.1 Laser Fired Contact

The concept of laser fired contacts (LFC) was first proposed by Schneiderlochner et al. at Fraunhofer in 2002 [1] It is an elegant way to develop the rear point contact of crystalline silicon solar cells together with a well-passivated back surface without using photolithography.

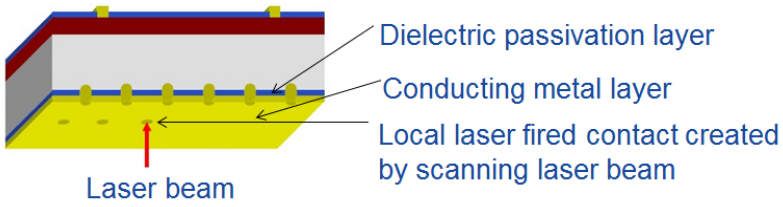

Figure 4.1 Laser Fired Contact Introduction

As shown in Figure 4.1, during LFC process, a laser pulse drives the dopant through the insulator and into the Silicon, locally doping with the Silicon and forming a low-resistance ohmic contact between Silicon and back contact metal. The goal of the LFC is always to provide sufficient contact with minimum damage to the surface or bulk wafer induced by laser. Since the inception of LFC, electrical properties, local composition, lifetime impact and device properties of LFC have been widely studied

[1-8]. The LFC device has achieved efficiency as high as 21.3% [1]. The contact resistance measurement of LFC has been comprehensively studied by Ortega group [7]. The morphology and compositional distribution have been studied by several groups with TEM and SIMS [9]. The lifetime degradation after LFC was studied by Anroite group on hetero-junction solar cell. [8]

Most studies focus on Al LFC on p-type Si to form the base contact or n-type Si to form the emitter, respectively [3], while there are very few publications applying LFC to obtain the ohmic base contact for n-type Si wafers [4]. As n-type crystalline silicon becomes more promising in photovoltaic research, it is important to develop the LFC techniques on the n-type crystalline silicon. To successfully transfer the LFC technique from p-type silicon to n type silicon, it is important to understand the basic physics of metal-semiconductor contact and LFC on p-type crystalline silicon.

4.1.2 Metal-Semiconductor Ohmic Contact

In general, there are two types of contacts between metal and semiconductor, depending on the band structure change when those two materials are intimately touching each other. Take n-type semiconductor as example, if the work function of metal ϕ_M is larger than the work function of semiconductor ϕ_S, a depletion contact is formed during the Fermi-level alignment. There is an energy barrier ϕ_B which is given by:

$$\phi_B = \phi_M - \chi \quad (4.1)$$

where χ is the electron affinity of the semiconductor. [10]

This type of metal-semiconductor contact is called depletion contact. A minimum activation energy $q\phi_B$ would be required for the carrier to overcome the

barrier. Therefore, from macroscopic point of view, there would be a significant voltage drop at the metal/ semiconductor junction for the current to transport between the metal and semiconductor, which is not desirable for device application.

On the other hand, when ϕ_M is equal to or smaller than ϕ_B, a 'slope' rather than a 'spike' at the junction is formed during the band alignment. Hence the voltage drop at the contact is considered to be non-existence for the electrons to travel through semiconductor to metal. Vice versa, for metal and p-type semiconductor contact, depletion contact and accumulation contact is formed when $\phi_M$is smaller and larger than ϕ_B, respectively. Figure 4.2 show then two types of contacts between metal and n-type semiconductor.

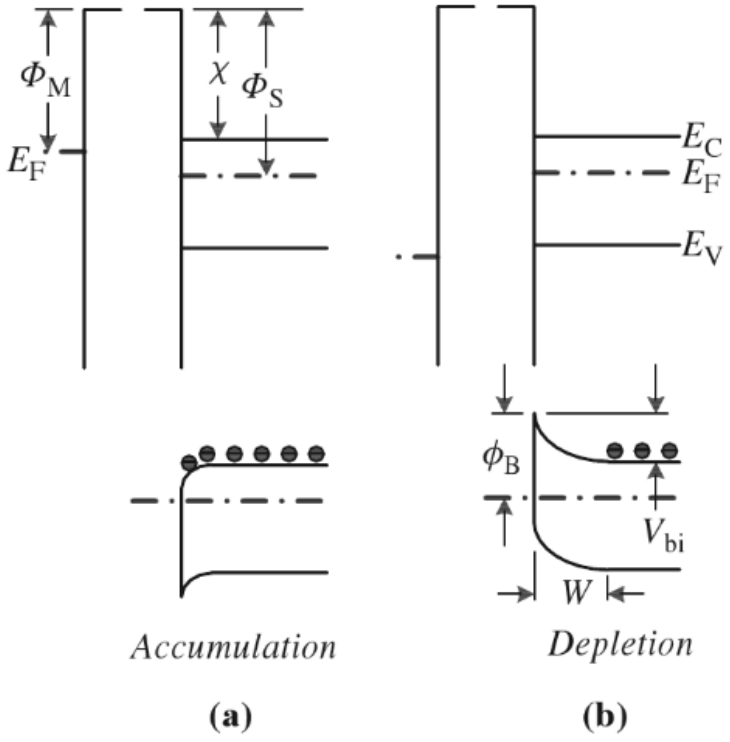

Figure 4.2 Metal-semiconductor band diagram before (upper) and after (lower) contacting. [10]

However, in reality, choosing metal with proper work function according to the above theory does not yield a good ohmic contact with crystalline silicon. In silicon-metal contact, due to the Fermi-level pinning caused by the interface states [11], the barrier ϕ_B always exists and tends to be a constant value which is independent of metal work function. Therefore, an accumulation type of contact generally does not exist for silicon. Rather than changing the barrier height ϕ_B, the practical metal semiconductor ohmic contact is usually achieved by changing the barrier width W, which is proportional to $N_D^{-1/2}$, where N_D is the doping level of semiconductor at the contact. When the silicon surface is heavily doped, the barrier between the metal and silicon is narrowed which enables the possibility of carrier tunneling through the barrier without the need to go over the barrier. This type of depletion contact with narrowed barrier width is called Field Emission (FE) contact, as shown in Figure 4.3(c). If the semiconductor is only lightly doped at the contact area, the contact mechanism is called Thermionic Emission (TE), as shown in Figure 4.3(a). Besides those two extremes, when the semiconductor is intermediately doped, the dominating transport mechanism is called Thermionic-field Emission (TFE), where the carriers in semiconductor need to be thermally excited high enough where the barrier is narrow enough for tunneling, as shown in Figure 4.3(c). For silicon, the relationship between the three regimes of mechanism and the doping level is plotted in Figure 4.4 [12].

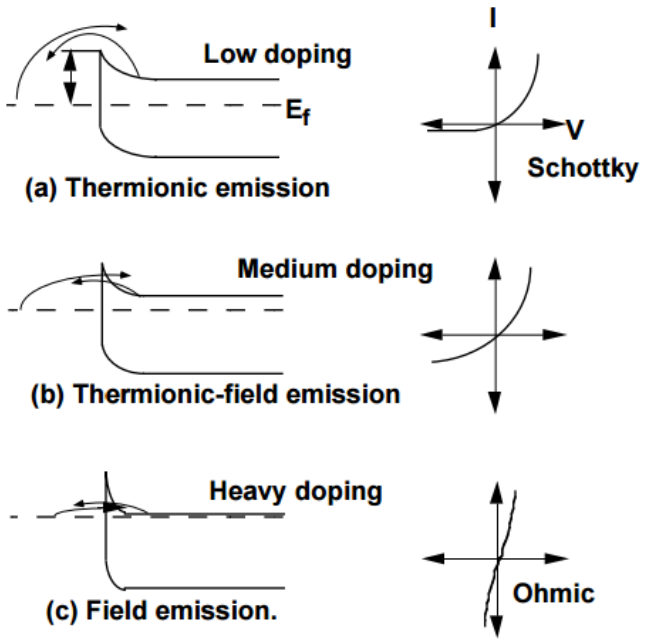

Figure 4.3 Depletion-type contacts of metal and n-type semiconductor with different level of doping. [12]

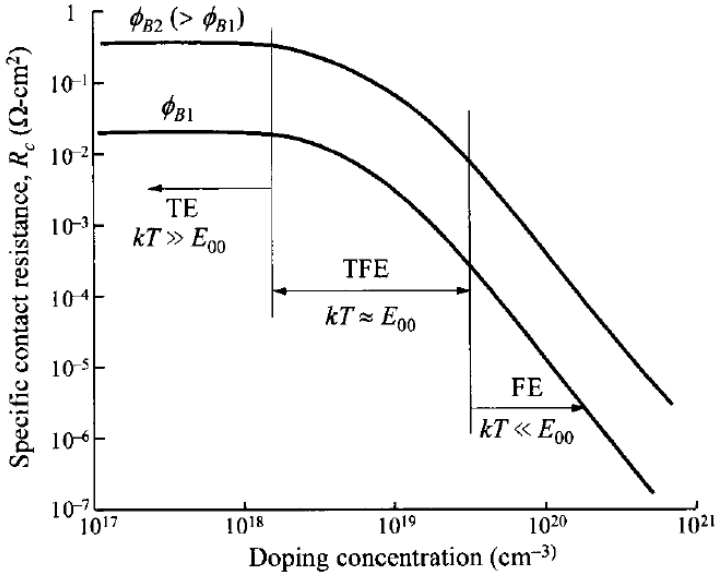

Figure 4.4 Dependence of specific contact resistance and contact mechanism on doping concentration. [12]

In p-type crystalline silicon LFC, the Aluminum is the only metal used in all groups, as Aluminum is a good conductor as well as a p-type dopant at the same time. During LFC, the local silicon and the Aluminum top metal layer melt and re-crystallize together resulting in a high level of doping. The theory was confirmed by micro SIMS study of local LFC contact by Zastrow et. al [].

4.2 Electrical Test Structure

Effective LFC's must have a low contact resistance and the firing process must have only a minimum impact on the Si surface passivation. The LFC impact on passivation will be mainly discussed in Chapter 5. The contact resistance, ρc, was evaluated by two methods: 1) the vertical test structure shown in Figure 4.5, which was proposed by Ortega et. al [7] and used by Sánchez-Aniorte et al [8]; and 2) the lateral structure shown in Figure 4.6 which is similar to Transfer Length Method (TLM) [10] [13].

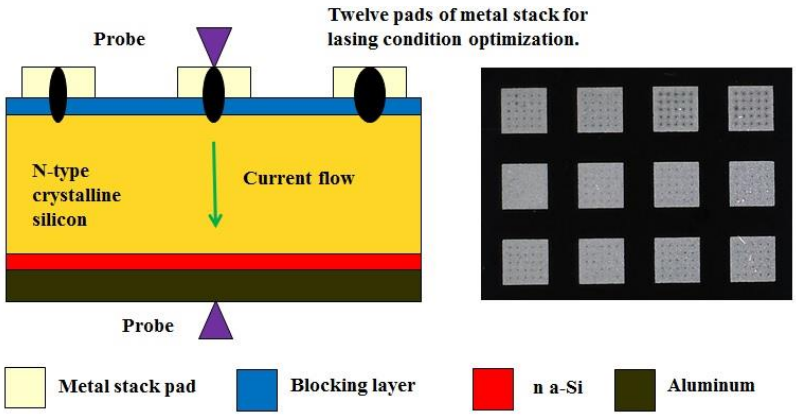

Figure 4.5 Vertical test structure of LFC

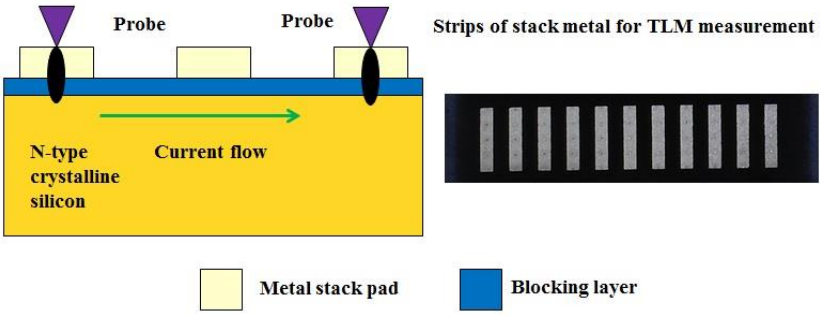

Figure 4.6 Lateral test structure of LFC

In the vertical test structure, the resistance was measured between the Al back contact and an array of 3 mm by 3 mm square metal stack pads each with identical LFC spots. By assuming that the spots are connected in parallel and are electrically independent, the resistance of a single LFC spot could be extrapolated from the measured total resistance according to:

$$R_t = N \times R_{LFC} \qquad (4.2)$$

where R_t is the measured total resistance, N is the number of LFC spots on the pad being characterized, and R_{LFC} is the resistance of a single LFC consisting of three components:

$$R_{LFC} = R_c + R_s + R_{bc} \qquad (4.3)$$

where R_c is the contact resistance of a single LFC spot, R_s is the wafer bulk spreading resistance of a single LFC spot, and R_{bc} is back contact resistance, which is negligible due to large area and demonstrated low resistance contact between Al and n-type a-Si. R_s can be calculated by the following equation [14]:

$$R_s = \frac{\rho_b}{2\pi r} \tan^{-1} \frac{2t}{r} \qquad (4.4)$$

where ρ_b is wafer resistivity, r is the radius of the LFC spot and t is the wafer thickness. With extrapolated R_{LFC} and calculated R_s, and by assuming the electrically active area is uniform over the LFC spot, the specific contact resistance ρ_c could be calculated from R_c as:

$$\rho_c = \pi r^2 \times R_c \quad (4.5)$$

The advantage of using the vertical test structure is that it allowed more rapid and efficient optimization of the lasing condition on many different pads of the metal stack on a single sample. To validate whether the LFC spots could be considered as electrically independent in the vertical model, both the number and spacing of LFC spots in the array were varied for different metal stack pads. As shown in Table 4.1, the calculated $R_{LFC}'s$ are similar when pitch (distance between adjacent LFC spots) is varied from 500 μm to 1500 μm, indicating that the assumptions used to analyze the vertical test structure are valid for determining R_C. This is not surprising given that the spot radius r is < 30 μm which is much smaller than pitch and wafer thickness.

TABLE 4.1. R_{LFC} with different pitch

Number of LFC spots	Pitch (μm)	R_{LFC} (Ω)
4	1500	925
9	900	864
16	700	917
25	500	958

However, if $R_c \ll R_s$, which is usually true when a good quality ohmic contact is formed, a small variation in R_s due to an uncertainty in electrically active area LFC spot could result in a large deviation in R_c and ρ_c. Therefore, the vertical test structure may not be accurate when ρ_c is very low. A lateral test structure similar to TLM was used where the resistance was measured between two strips of metal stacks with different spacing, d. On each strip, a string of separated LFC spots were fired with the same lasing condition. The measured resistance is:

$$R_t(d) = 2 \times \frac{R_c}{N} + d\frac{R_{sh}}{Z} \quad (4.6)$$

where $R_t(d)$ is the measured total resistance, N is number of LFC spots in each string, d is the lateral spacing between strings of LFC spots being measured, R_{sh} is the sheet resistance of the bulk wafer, Z is the width of the metal strip. By plotting R_t vs d, the $\frac{R_{sh}}{Z}$ is the slope where Z was fixed at 8 mm and the intercept is $2 \times \frac{R_c}{N}$.

The typical experimental loop is to investigate different metal stacks, blocking layers and lasing conditions, by using the vertical test structure first since this test structure allows rapid measurement of specific contact resistance of a certain metal/ blocking layer combination. Once a promising material system is found, and then its specific contact resistance is more accurately calculated by using the TLM lateral test structure.

4.3 Material and Lasing Condition Optimization

In this section, different metal or metals stacks are studied for their suitability for LFC on n-type crystalline silicon. Different blocking layers between metal and crystalline silicon, mainly p a-Si or a-SiNx, are studied. As discussed in last section,

due to the Fermi-level pinning the metal with work function larger does not necessary form the accumulation contact with crystalline silicon.

To validate the theory, the metal selection for LFC on n-type crystalline silicon starts with Aluminum and Silver. Aluminum is the common metal for LFC on p-type crystalline silicon, and silver is commonly used to form n-type contact with n-type crystalline silicon. The vertical test structure was used, and no blocking layer was asserted between metal and crystalline silicon for simplicity.

Before LFC, the J-V characterizations show that both test structures behave as open-circuit, meaning no ohmic contact was formed between the metals and silicon wafer. After laser firing, for Aluminum, the J-V results show a diode shape characteristics, as shown in Figure 4.7. The reason is that Aluminum is a p-type dopant and during the LFC process, the Al is locally doping the n-type crystalline silicon to p-type. Therefore a p-n junction is formed on the surface of the silicon wafer. For silver, an ohmic-like contact was obtained after LFC. The specific contact resistance changes over voltage and is generally over 20 $m\Omega cm^2$ which does not meet the requirement of photovoltaic device. Furthermore, when a blocking layer, either p a-Si or a-SiNx, which are possible layers need to be fired through in the actual IBC-SHJ device proposed in Chapter 1, was inserted between Ag and n c-Si, the laser processing does not yield any ohmic contact J-V characteristics. Therefore, an n-type dopant is necessary in obtaining low resistance of LFC on n-type crystalline silicon.

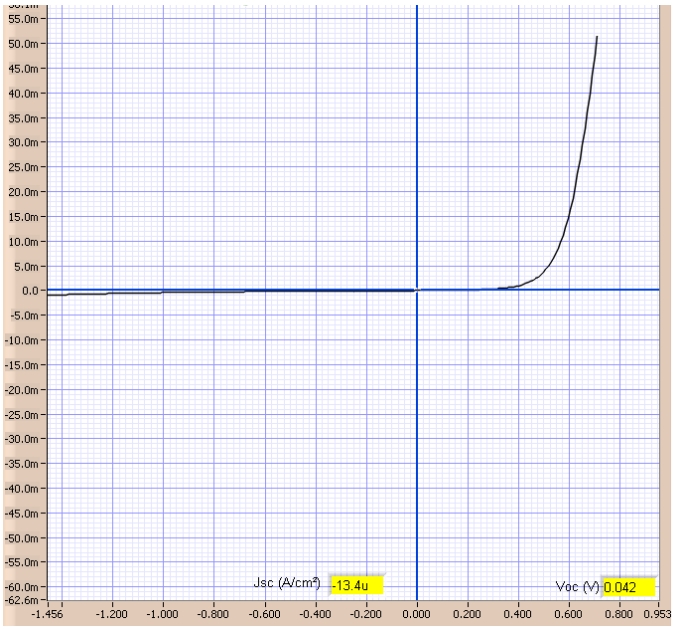

Figure 4.7 J-V Characteristics of vertical test structure of Al/ n c-Si

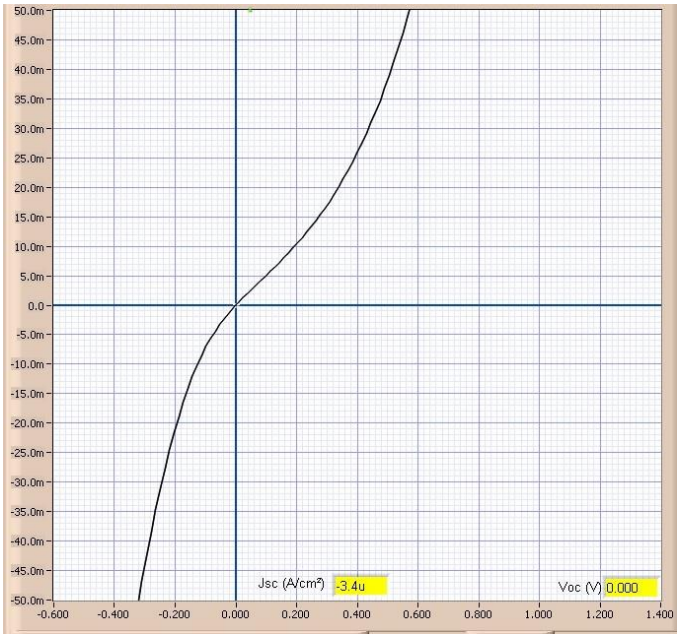

Figure 4.8 J-V Characteristics of vertical test structure of Ag/ n c-Si

To add the n-type dopant needed in LFC on n-type crystalline silicon, a layer of 50 nm antimony (Sb), which is an n-type dopant, was deposited in a four pocket E-Beam system which allowed metal stacks to be deposited without breaking vacuum. Unlike LFC on p-type crystalline silicon where Al could serve as the dopant source and current carrying layer at the same time, the resistivity of Sb is ~ $4x10^{-5}$ Ω-cm which is orders of magnitude higher than common contacting metal Al or Ag whose resistivity is at the level of 10^{-8} Ω-cm. Therefore, using Sb alone will cause a large sheet resistance from the metal layer. A thicker and more conductive layer of either Ag, Al or Ni was deposited on top of Sb layer for lateral current conduction. Another problem of Sb is that it tends to have poor adhesion to the c-Si. To address this issue, a very thin layer of titanium was deposited between Sb and Si to aid adhesion. Thus, a unique metal stack system of X-Sb-Ti was used in for LFC on n-type crystalline silicon where X refers to Ag, Al or Ni in this thesis.

To validate the effectiveness of adding Sb as dopant source for LFC, the J-V characteristic of vertical test structures laser fired contacts through a-SiNx or p a-Si were compared Ag and Ag-Sb-Ti metal stack. The J-V characteristic plots are shown in Figure 4.9 and Figure 4.10. Before LFC, neither structure has any current flow due to the insulating SiNx layer. After LFC, the structure with Ag is still highly resistive or blocking although Ag is often used to form ohmic contact on n-type crystalline silicon. However, the Sb containing structure has a linear JV characteristic with very low resistance indicating that the Sb is doping the Si.

Figure 4.10 shows the J-V characteristic of vertical test structures having metal contact laser fired through a-Si p-layer comparing both Ag and Ag-Sb-Ti metal stack. Before LFC, both structures are clearly diodes created by the p-type a-Si / n-type c-Si

heterojunction. After LFC, the structure with Ag is still a blocking diode contact while the Sb containing structure has a linear J-V characteristic with very low resistance indicating that the Sb is doping the Si and has shunted the p-n junction. Figures 4.9 and 4.10 clearly demonstrate the necessity of Sb in creating a low resistance ohmic contact for n-type crystalline silicon when firing metal through either an insulator or p-n junction.

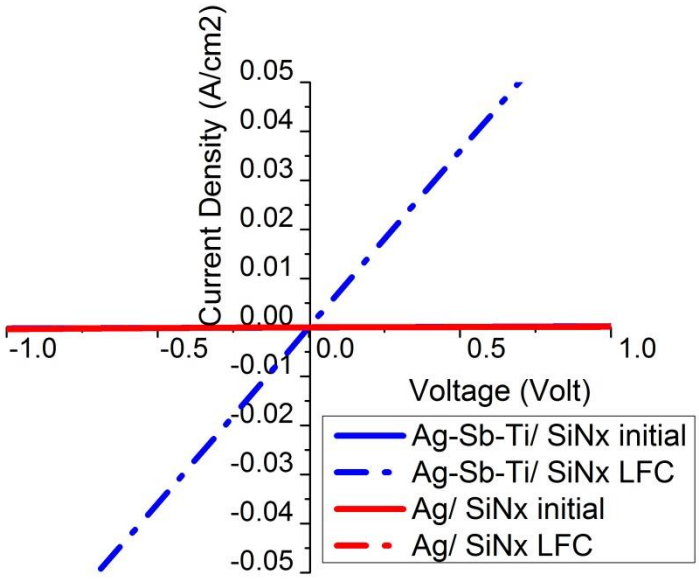

Figure 4.9 J-V characteristic of vertical test structure with Ag (red) and Ag-Sb-Ti (blue) stack fired through SiNx insulator layer. Only Sb containing stack after LFC shows low resistance J-V curve. Other three curves are open-circuit and overlap with x-axis.

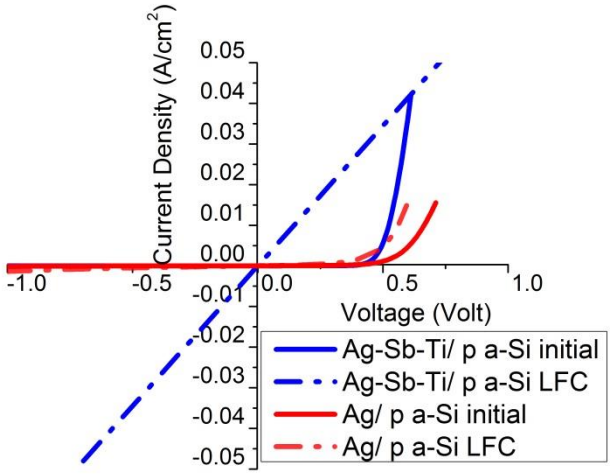

Figure 4.10 J-V characteristic of vertical test structure with Ag (red) and Ag-Sb-Ti (blue) stack fired through p a-Si layer.

Laser firing was performed on the metal stack structures using an Nd-YAG solid state pulse laser where the wavelength, output power and number of pulses per LFC spot were varied to optimize the contact properties. The firing of metal stacks was found to be relatively insensitive to wavelength - 532 or 1064 nm - and thus, 532 nm was used to optimize the contact properties. However, the processing window for obtaining a proper-fired LFC is very sensitive to the components of stack metal and surface texturing. Both laser pulse energy and pulses per spot were varied to obtain a properly fired contact. It was found that using lower pulse energy and increasing the number of pulses per LFC spot gave a more gradual transition of LFC spot morphology especially with the Al-Sb-Ti stack as shown in Figure 4.11. Thus, optimizing the number of pulses at lower pulse energy gave better process control.

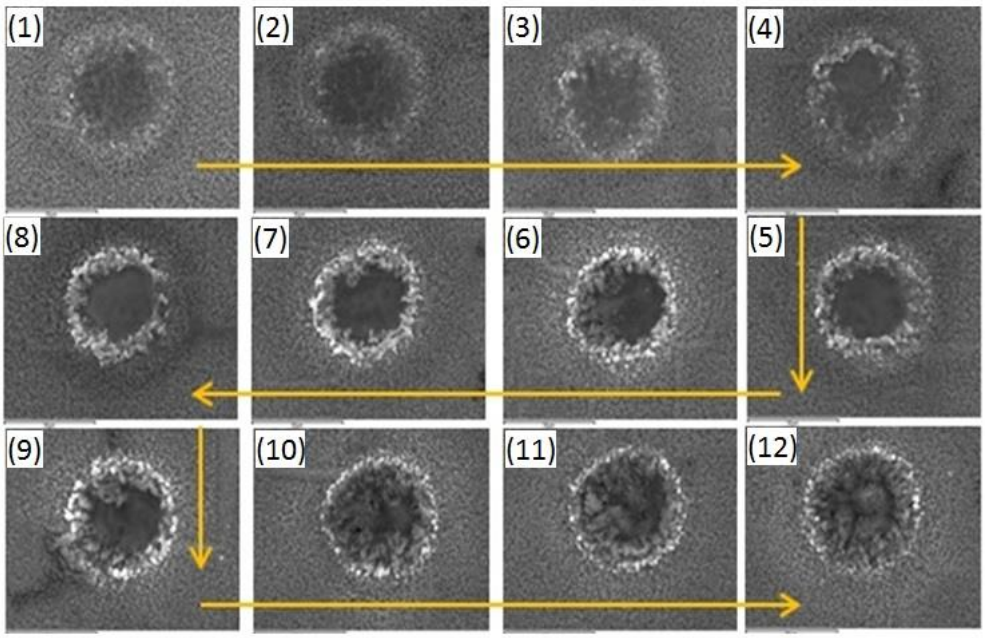

Figure 4.11 SEM images of LFC of Al-Sb stack. The progress indicates increasing number of shots per spot. The morphology of LFC spots transit from under-fired (1-3) through proper-fired (4-9) and finally to over-fired (10-12).

Typical lasing conditions used in this study are summarized in Table 4.2. The LFC could be characterized qualitatively as under-fired, proper-fired and over-fired, as shown in Figure 4.12 which examines the morphology and elemental distribution after LFC by SEM and EDX. For an Al-Sb-Ti stack on p a-Si/ n c-Si, a correlation between the morphology, the EDX mapping and ρ_c was found by comparing SEM and EDS with electrical measurements. Although the EDX is not sensitive enough to detect the doping level of Sb, it could serve as a quick diagnosis in LFC process control and lasing condition optimization.

TABLE 4.2 Lasing Condition for LFC

LFC Parameters	Condition/Value
Laser Type	Nd-YAG
Pulse Duration	7ns
Laser Mode	TEM00
Wavelength	532nm
Full Angle Beam Divergence	1.2mrad
M^2	1.2
Frequency	10 kHz
Power	110-150 mW
Pulses per LFC Spot	15-40
LFC Spot Radius	15-25 um
LFC Spot Pitch	500-1000 um

A properly fired contact, i.e. LFC with lowest ρ_c with no silicon bulk damage, was correlated with a smooth surface where the current carrying layer Ag, Al, or Ni was completely ablated as shown in the top row of Figure 4.12. For under-fired, a smooth surface was observed but the current carrying layer Ag, Al, or Ni was not completely ablated and a very high ρ_c resulted since the Sb failed to dope the underlying Si. For over-fired, excessive damage was observed that extended down into the bulk silicon wafer. This type of morphology correlates with moderate ρ_c but visible damage. Proper-firing generally gives smooth morphology and, when

optimized, a specific contact resistance below 10 $m\Omega cm^2$. Over-fired has visually noticeable bulk damage and can also have a specific contact resistance below 10 $m\Omega cm^2$, comparable to the properly fired LFC. The typical laser power for proper-firing an Al-Sb-Ti stack is around 100 mW to 150 mW. Higher laser power (either higher energy dose per pulse or more pulses per LFC spot) will result in an over-fired LFC, while lower laser power will result in under-fired LFC.

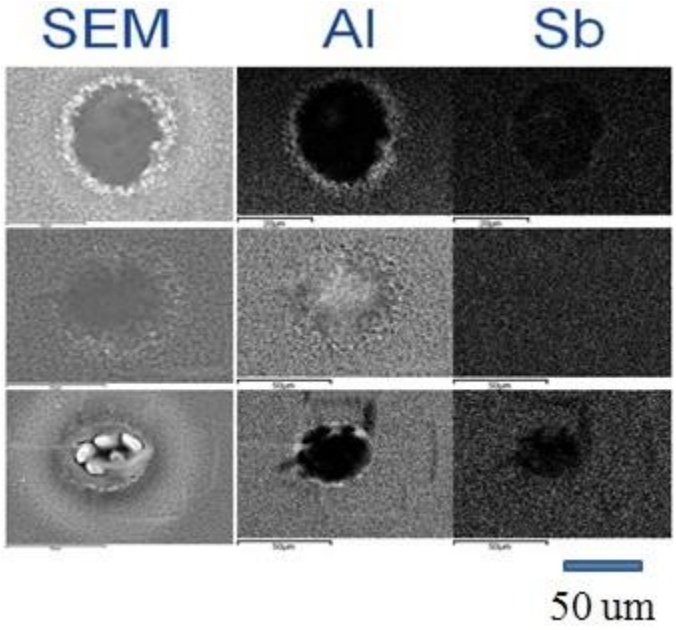

Figure 4.12 SEM and EDX maps of LFC. Top row: optimal-firing; Middle row: under firing; Bottom row: over-firing.

The calculated specific contact resistances for various metal stack and blocking layer structures are listed in Table 4.3. For both the vertical and lateral test structure, ρ_c is less than 20 $m\Omega cm^2$ indicating reasonable quality ohmic contact after laser firing the metal stack through the blocking layer including the p-n hetero-junction blocking

layer. The ρ_c calculated by the TLM method was always larger for the vertical test structure probably due to over-estimating the effective radius of the LFC spot of the contact. With larger r the spreading resistance would be smaller than real value, leaving the R_c part in equation (4.3) larger than reality.

TABLE 4.3 Specific contact resistance of LFC. The common back contact BC=n c-Si/ n a-Si/ Al

Structure	ρ_c Vertical ($m\Omega cm^2$)	ρ_c TLM ($m\Omega cm^2$)
Ag-Sb-Ti / p a-Si/ BC	<1.0	5.0
Al-Sb-Ti / p a-Si/ BC	<0.3	1.9
Al-Sb-Ti / SiN_x/ BC	<0.7	7.1
Ni-Sb-Ti/ p a-Si/ BC	NA	20.6
Ni-Sb-Ti/ SiN_x/ BC	NA	20.0

Surprisingly the Al-Sb stack has the lowest ρ_c of three stacks, even though Al is known as a p-type dopant in silicon which indicates Sb doping is more efficient than Al doping after laser firing. The Ag-Sb stack was problematic due to the high reflectivity of Ag, which made the laser processing window for properly fired contacts very narrow and irreproducible. The rough features of the Ag-Sb LFC spot may also lead to a non-uniform conductance within the LFC spot [15]. The Ni-Sb was also not

as successful since the Ni is brittle which makes deposition of thick Ni difficult and results in a high lateral resistance within Ni-Sb stack.

To further evaluate the electrical properties of the laser fired contacts, a temperature dependent TLM measurement was performed on an Al/Sb/SiNx stack after firing. Five TLM measurements were taken at temperatures from 213 K to 333 K, as shown in Figure 4.13. A plot of specific contact resistance vs. temperature is shown in Figure 4.14. The ρ_c has a very weak dependence on temperature indicating a Thermionic-Field Emission type of ohmic contact [12] where the narrowing of the potential barrier at the metal silicon interface can be attributed to successful n^+ doping in the LFC area.

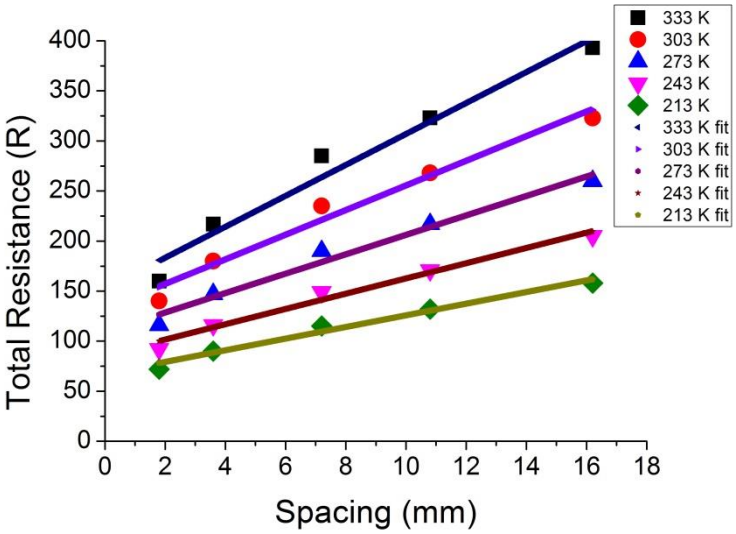

Figure 4.13 TLM measurements of contact resistance of LFC at different temperatures

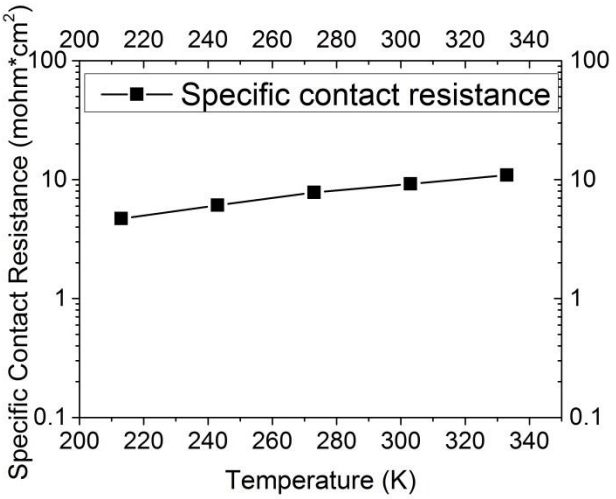

Figure 4.14 Specific contact resistance of LFC as function of temperature changing from 213 K to 333 K.

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Chapter 5

LASER FIRED CONTACT IMPACT ON LIFETIME

As mentioned in previous chapter, the goal of the LFC is to provide sufficient ohmic contact, while trying to minimize the damage to the surface or bulk wafer induced by laser. In chapter 4, the main focus was on the specific contact resistance of LFC.

In the vertical test structure of LFC in chapter 4, individual LFC spots could be considered resistances that are connected in parallel. The series resistance of the total test structure or the device can consistently go down with increased LFC area fraction f. As seen in Figure 5.1, for a test structure of LFC of early Ag-Sb-Ti stack through p a-Si layer, the normalized device series resistance goes down with the increase of f. However, this is not a practical approach to reduce the series resistance of device since the LFC process inevitably induce de-passivation on the surface layer, or even bulk defects if the lasing condition is not properly chosen. Reflecting on the device level, more LFC will reduce the device resistance at the cost of greatly reducing the V_{OC} at the same time. The more reasonable approach would be to achieve the resistance with smallest possible LFC area fraction, and the contacting area should have minimum possible laser induced damage. In this chapter 5, the other side of LFC which is the laser damage will be discussed.

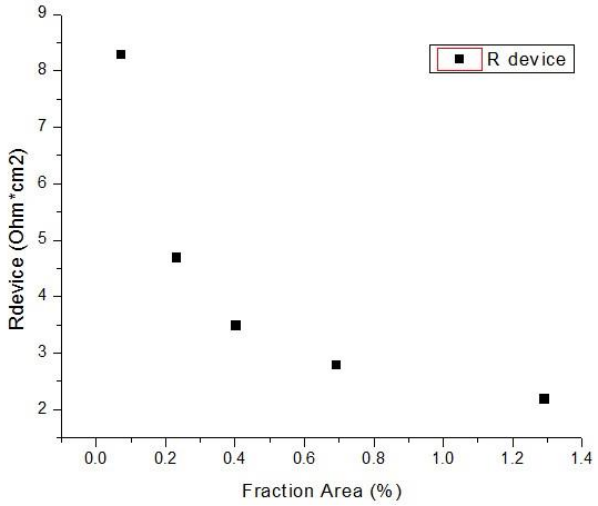


Figure 5.1 Normalized test structure resistance with increasing LFC (Ag-Sb-Ti stack through p a-Si layer) area fraction.

5.1 Recombination of Crystalline Silicon Solar Cells

Generally, there are three types of recombination occurring in a silicon solar cell device: the radiative recombination, the Auger recombination, and the Schokley-Read-Hall (SRH) Recombination. In radiative recombination, the electron in conduction band falls to a lower energy state in valence band with the emission of photo. In Auger recombination, the electron in conduction band recombines with the hole in the valence band as well, but instead of emitting photon, the process gives the excess energy to another free electron. The SRH recombination usually occurs at the defects within band gap. The defect state first captures an electron and then a hole and then the captured electron and hole recombine with each other at the recombination site. The three mechanisms of recombination are shown in Figure 5.2. [1] Considering

all these three mechanism, the total lifetime of a semiconductor could be described in the following equation:

$$\frac{1}{\tau} = \frac{1}{\tau_R} + \frac{1}{\tau_{Auger}} + \frac{1}{\tau_{SRH}} \quad (5.1)$$

Where τ is effective lifetime, $\tau_R$is radiative lifetime, $\tau_{Auger}$is Auger lifetime, and τ_{SRH} is Shockley-Read-Hall lifetime.

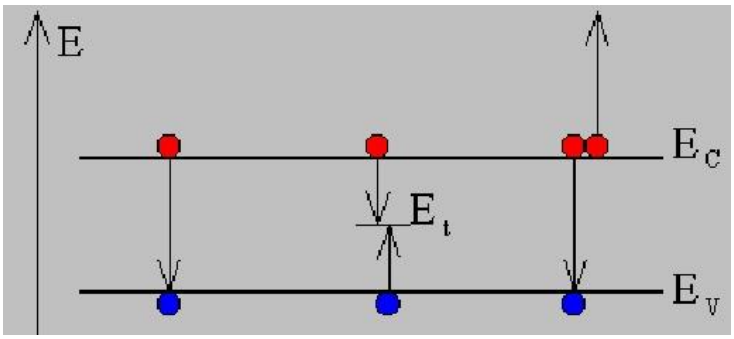


Figure 5.2. Recombination Mechanisms from left to right: radiative recombination, SRH recombination and Auger recombination. [1]

The radiative recombination and Auger recombination are two types of intrinsic recombination that even happen in perfect crystals. The SRH recombination happens when defects are present in the semiconductor and is the main limitation of lifetime of the device in this study. In today's silicon, the radiative recombination is negligible. For Auger lifetime, it only becomes significant when the carrier injection level is greater than $10^{-17}cm^{-3}$ [1], which is usually much higher than the injection level at which the solar cell device is operating. Therefore the SRH recombination is the most important mechanism affecting the total lifetime of the silicon solar cell device, and therefore is the only recombination mechanism being discussed in this chapter.

Recombination can also be classified according to the region of the cell in which it takes place. The SRH recombination could take place either at bulk silicon wafer, or at the surface of the silicon wafer. The equation 5.2

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_b} + \frac{1}{\tau_S} \qquad (5.2)$$

describes the total effective lifetime composed of surface lifetime τ_s and bulk lifetime τ_b.

Bulk recombination must be taken into consideration for multi-crystalline silicon or other lower quality silicon wafers used in device. In the work of this thesis, only high quality of FZ or CZ wafer with bulk lifetime exceeding 5ms were used. Therefore, the limitation of the device or test structure lifetime is the surface recombination loss, which is represented by surface lifetime τ_S.

Surface recombination can have a major impact both on the V_{OC} and J_{SC} [2]. If the high recombination rate takes place at the top surface where the light is being absorbed, it will have a larger impact on the J_{SC} since it is where the generation rate of carriers is highest. Luckily the LFC only is only processed at the rear surface. The LFC only serves as ohmic base contact which is far away from carrier generation for 150 um wafer used in this study. Therefore J_{SC} is not very sensitive to the LFC induced damage. In this thesis, we mainly focus the loss of V_{OC} and iV_{OC}, which is the implied open-circuit voltage, due to the degradation of effective lifetime caused by the increase of surface recombination velocity.

5.2 Previous Work

In the earlier work of LFC on p-type crystalline silicon, the impact of LFC on passivation is not widely studied quantitatively. The consideration on lifetime impact

is usually included in the device results. In the first LFC work, Schneiderlochner et.al [3] applied LFC of Aluminum through either SiO_2 or SiN_x rear side passivation layer on a diffused front junction solar cell, and then compared the efficiency to those cells with rear side point contacts developed by photolithography. For SiO_2 passivation layer the LFC cell exhibits small degradation compared with photolithography device. The V_{OC} only drops between 4-7 mV and a 21.3% efficiency cell was achieved. The degradation is more noticeable when firing through a lower temperature passivation layer SiN_x, with a V_{OC} drop slightly over 10 mV and 2 mA/mc^2 drop in J_{sc}. A total efficiency of 19.5% is still achieved for SiN_x passivation. Later on, Daniel Kray [4] successfully applied the Fischer's model, which calculates recombination velocity at surface with non-uniform passivation quality, to evaluate the local recombination loss at the LFC spot. The surface recombination velocity at the local LFC contact was concluded to be above the level of $1x10^5$cm/s. The de-passivation effect on hetero-junction LFC solar cell was also studied by I. Martin group [5]. By using the PC1D simulation and the Fischer model, they also concluded a local recombination velocity above $1x10^5$cm/s at contact region. An interesting discovery is that in their EL mapping on a front junction cell with LFC, the recombination center has a much larger diameter at the level of 150 um. The darker halo may even extend to hundreds of micron of length, while the actual diameter from the morphology of LFC spot is only slightly larger than 100 um. This is probably an indication that laser process is depassivating a larger area than the contact region.

In this thesis, we have prepared test structures specifically for evaluating the LFC depassivation effect using Fischer's model and the model developed by Muller [6] that specifically deal with point-like laser processed local base contact. Front

junction devices with LFC were also fabricated and characterized to determine the V_{OC} loss due to laser and to validate the calculation from test structures.

5.3 LFC Morphology and TEM

From previous section of the chapter we could easily see the depassivation effect on the surface passivation is inevitable. However, when the lasing property, metal stack and surface condition are properly combined, the damage extended into the bulk wafer can be avoided. And in fact the bulk damage must be avoided in order to fabricate high efficiency as well as to calculate the recombination velocity at the contacted surface.

As discussed in chapter 4, Figure 4.12, the damage from laser processing could well extend into the bulk wafer when the laser energy dose is high enough. When the laser power is higher, an over-fired contact is formed, shown in Figure 5.3, and the laser induced damage will not only affect the surface lifetime τ_S, but also the bulk lifetime τ_b. There is currently no analytical model to de-couple the two factors from the measured lifetime of the sample which serves as the starting raw data in both models developed by Fischer and Muller. In figure 5.4 the visible bulk damage was eliminated by using a lower laser energy dose. However even if the laser is not machining into the wafer, the laser induced stress could still develop cracks into the bulk of the wafer. Ortega et.al presented that even a very smooth surface of LFC cannot guarantee a damage free bulk under the LFC spot. In Figure 5.5, the cracks are visibly extending through the cross section, which is not visible when looking from the top view.

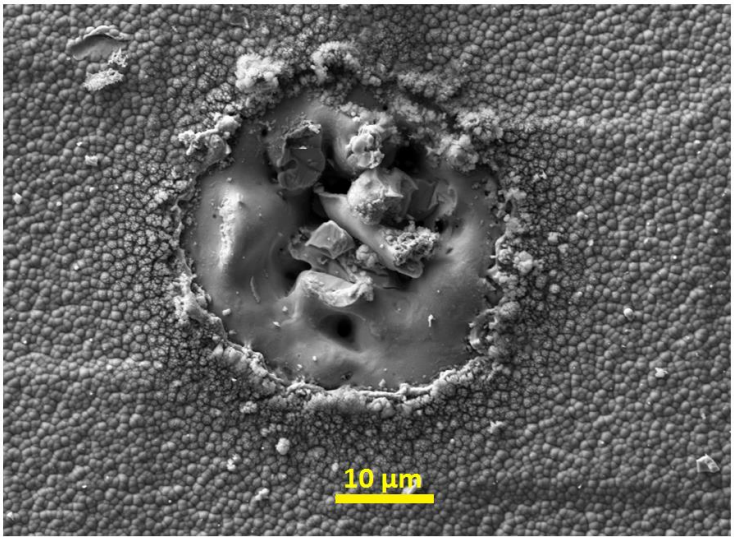


Figure 5.3 Top view of LFC spot with visible bulk damage

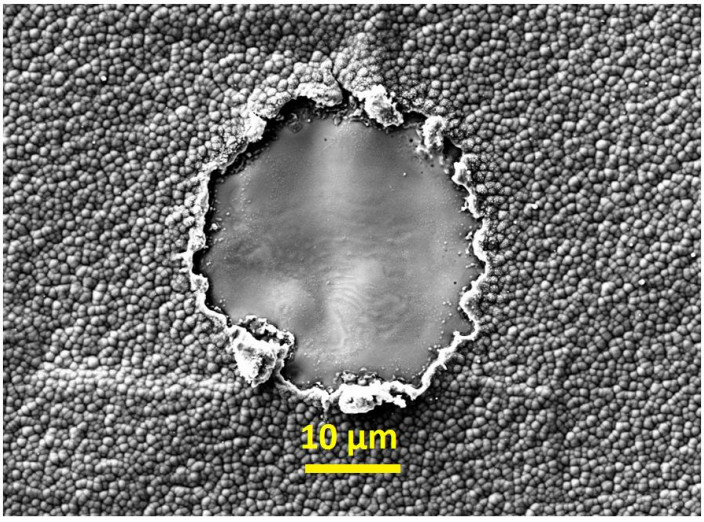


Figure 5.4 Top view of LFC spot with no visible bulk damage

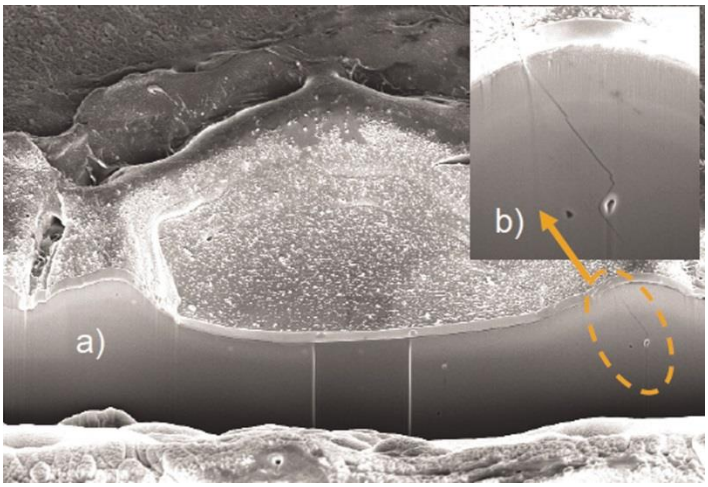


Figure 5.5 Cross Section-view of LFC spot. Although no bulk damage is observed at surface from top view, crack is visible through a cross section view. [7]

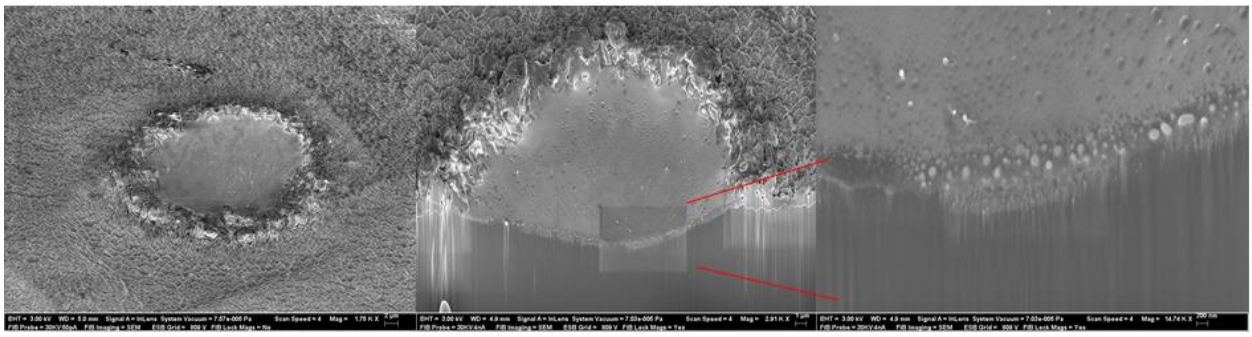


Figure 5.6 Top view (left) and cross section view (middle and right) of LFC spot. In both pictures no bulk damage was observed.

As a result, a cross section view of LFC spot is necessary to determine whether the combination of lasing condition and material system will not yield any bulk defect. A LFC spot on Al-Sb-Ti stack through p a-Si on textured wafer was studied. A top view of the proper-fired LFC spot was first taken as shown in Figure 5.6 left. The spot was smooth and no physical damage is visible from the top view. Then a focused ion beam was then applied into the center of pit and milled through for ~20um deep.

Visible damage to wafer is limited to 300nm depth from surface, if any, from the middle and right image of Figure 5.6. Vertical lines are un-smooth milling due to textured surface rather than defects.

Second order defect like crystal disorder due to laser heating and crystal re-growth is not detectable through cross section SEM. Therefore a cross section TEM image of proper fired LFC spot was taken externally at MIT to investigate any possible crystal defects. From Figure 5.7, no crystal distortion is found.

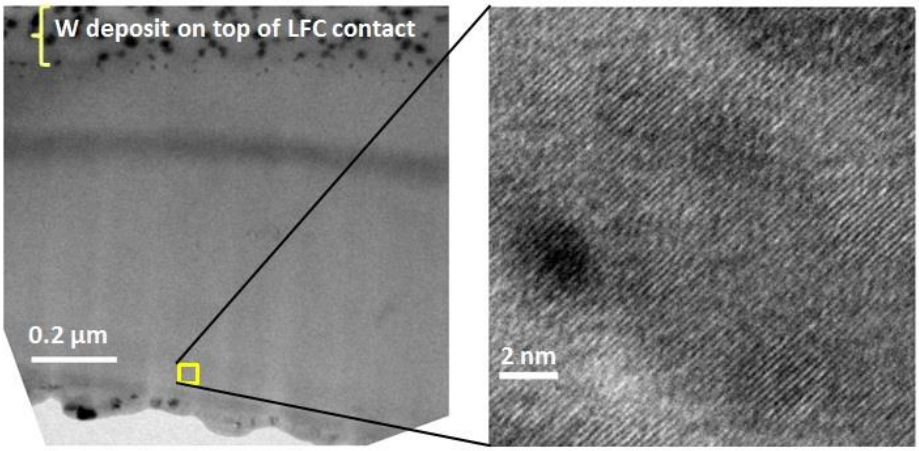


Figure 5.7 Cross-section TEM analysis of LFC spot for crystal structure defect.

Therefore, based on the top view and cross section view of SEM image as well as the TEM analysis, we make the assumption that the laser damage is limited to the surface passivation and no bulk lifetime degradation is associated with laser. Based from this assumption a set of test structures were fabricated and quantitatively analysis of SRV at LFC contact was performed.

5.4 Surface Recombination Velocity of LFC:

To evaluate the impact from LFC on the surface passivation, samples with both sides passivated by intrinsic a-Si layers were fabricated to quantitatively investigate the recombination loss. The lifetime was first measured by QSSPC for structures with intrinsic a-Si layers on both sides of the wafer before metallization. The metal stack was then deposited on the rear side of all samples and laser firing was performed on metal stacks except for a control sample. The metal stack was chemically removed and effective lifetimes were measured again for all samples.

The relation between measured effective lifetime $\tau_{eff}$and the effective surface recombination velocity S_{eff} is described as [8]:

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_b} + \frac{1}{\tau_S} \qquad (5.2)$$

with

$$\tau_S = \frac{W}{2S_{eff}} + \frac{1}{\mathrm{D}}\left(\frac{W}{\pi}\right)^2 \qquad (5.3)$$

where W is wafer thickness, τ_s is surface lifetime, τ_b is bulk lifetime which is set to be 5 ms for high quality FZ wafer [9] [10]. D is minority carrier diffusion coefficient for an n-type wafer with resistivity of 2 Ω-cm. The second term in equation (5.3) is at the order of 1 us and is almost negligible in calculation.

Before metallization, the front and rear surface recombination velocities are assumed to be the same.

$$S = S_{eff,f} = S_{eff,r} = S_p \qquad (5.4)$$

where S_p is the surface recombination velocity of passivated area before metallization, $S_{eff,f}$ and $S_{eff,r}$ are effective surface recombination velocities of front and rear wafer surface, respectively. After metallization and metal removal by etching, $S'_{eff,r}$ of the control sample with no LFC is still uniform over the rear surface but may have increased to a higher value of S'_p due to possible damage from metallization and etching. The $S'_{eff,r}$ of samples with LFC, however, is no longer uniform over the rear surface after LFC and could be represented as follows [6]:

$$S'_{eff,r} = \frac{4DS_cf}{\pi r S_c + 4D} + S'_p \qquad (5.5)$$

where S_c is surface recombination velocity of the LFC area, f is the area fraction of LFC of the passivated surface, and r is the radius of the LFC spot. With above equations, S_c could be calculated from lifetime measurements, as shown in Table 5.1. S_c was determined to be ~ 20,000 cm/s, which is in agreement with [4] [5].

The exact number of SRV at the local contact is greatly influenced by the size of the LFC spot one is using. In this thesis we use the LFC spot size determined by the visible morphology. In other literature, the electrical contact radius or the recombination radius could also be used. Generally the active electrical contact size is smaller than the morphology size, which means only a portion of the LFC spot performs as ohmic contact after laser processing. This is investigated by either EBIC or Lock-in Thermography [11]. Besides the radius, the actual shape of active LFC spot could vary. In some research the active contacting area is in the center of the LFC spot while other researcher sometimes claim the active contacting area is at the rim of the LFC spot. The recombination radius, on the other hand, is usually larger than the

morphology radius. It was confirmed in the EL mapping image by Martin group [5], and also investigated and confirmed in this thesis at MIT with the Photoluminescence mapping technique as shown in Figure 5.8. The degradation of passivation around LFC spot is often not uniform but shows a gradient characteristic. Therefore comparing only the SRV at the local contact is less meaningful than comparing the degradation of the solar cell device parameter caused by LFC.

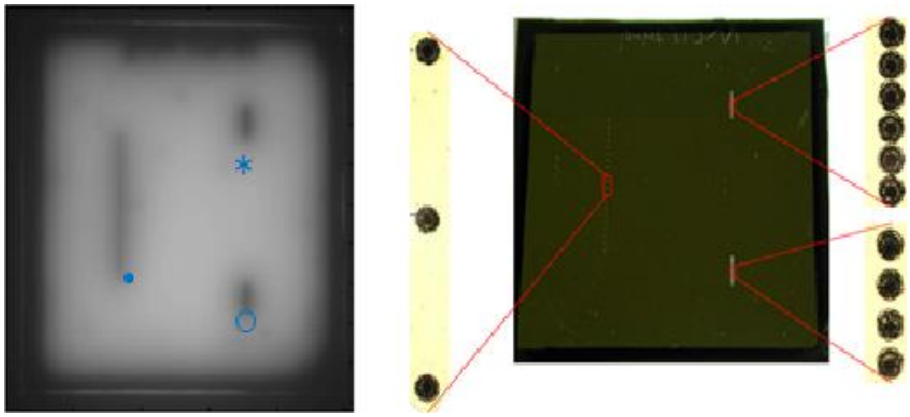


Figure 5.8 PL mapping of sample with LFC spots on passivated surface. The brighter area represents higher lifetime. The darker halo around LFC spots suggests the lower recombination quality extends from the physical LFC spots.

To evaluate LFC damage on an operating photovoltaic device, we use the standard QSSPC technique where the excess minority carrier density obtained during lifetime measurement was converted into implied open circuit voltage iV_{OC} by the following equation

$$iV_{OC} = \frac{kt}{q}\ln[\frac{(N_A+\Delta n)\Delta N}{{n_i}^2}] \quad (5.6)$$

Where iV_{OC} is the highest possible open circuit voltage being limited only by recombination, $\frac{kt}{q}$ is the thermal voltage, N_A is the doping concentration, Δn is the excess carrier concentration and n_i is the intrinsic carrier concentration. For LFC area fraction $f = 0.15\%$ and $f = 0.38\%$, the iVoc is around 40 mV and 50 mV lower, respectively, than that of the control sample of the test structure with $f = 0\%$, as shown also in Table 5.1 alone with SRV value.

Table 5.1 SRV and iV_{OC} before and after LFC for test structure. iV_{OC} and iV_{OC}' are implied open circuit voltages before metallization and after LFC and metal etch off, respectively. $f = 0\%$ is control sample of LFC test structure without any LFC

f (%)	$S_{eff,f}$ (cm/s)	$S'_{eff,r}$ (cm/s)	S_c (cm/s)	iV_{OC} (mV)	iV_{OC}' (mV)
0	8	25	NA	698	684
0.15	10	70	15,000	691	652
0.38	10	105	20,000	692	639

Table 5.2 Laser Fired Contact: Voc vs LFC area fraction

Number of cells	Avg iVoc (mV)	σ iVoc (mV)	Avg Voc with 0.15% LFC (mV)	σVoc with 0.15% LFC (mV)
8	681	19	655	15

Actual front junction cells solar cells with LFC were fabricated to investigate the relationship between Voc drop and LFC area fraction. The device structure is shown in Figure 5.9. Most layers in the device are similar with standard front junction

device, except for the rear side where the n a-Si back surface field and Aluminum contact layers were replaced by a 90 nm SiN_x blocking layer and Al-Sb-Ti LFC stack, respectively. After all PECVD depositions, all 8 device precursors were tested by lifetime tester to record the implied V_{OC}. The average V_{OC} is 681 ± 19 mV. After metallization and a 0.15% area fraction LFC, the average actual V_{OC} is measured and determined to be 655 ± 15 mV. The decrease in the voltage is close to 30 mV for f = 0.15% as shown in Table 5.2. This is in well correspondent with the calculated iV_{OC} change over f in the test structures experiment.

Another 3 set of devices were selected to experiment with larger LFC area fraction. The device structure is also the same as in Figure 5.9. For LFC area fraction 0.15% and 0.3% the drop in V_{OC} is close to results in Table 5.2. With area fraction higher than 0.4% and up to 1.2% the slop of V_{OC} drop is less steep and is only 5-10 mV every 0.3% percent. This means the V_{OC} drops slower as the LFC area fraction increases to larger number.

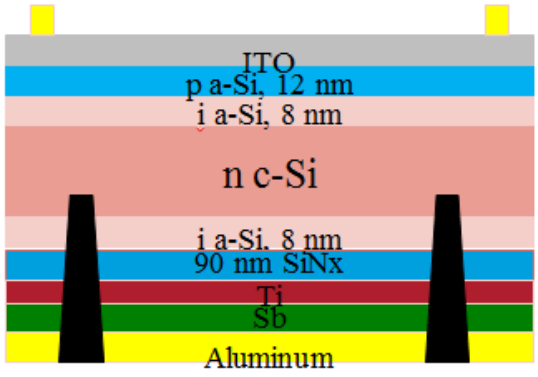
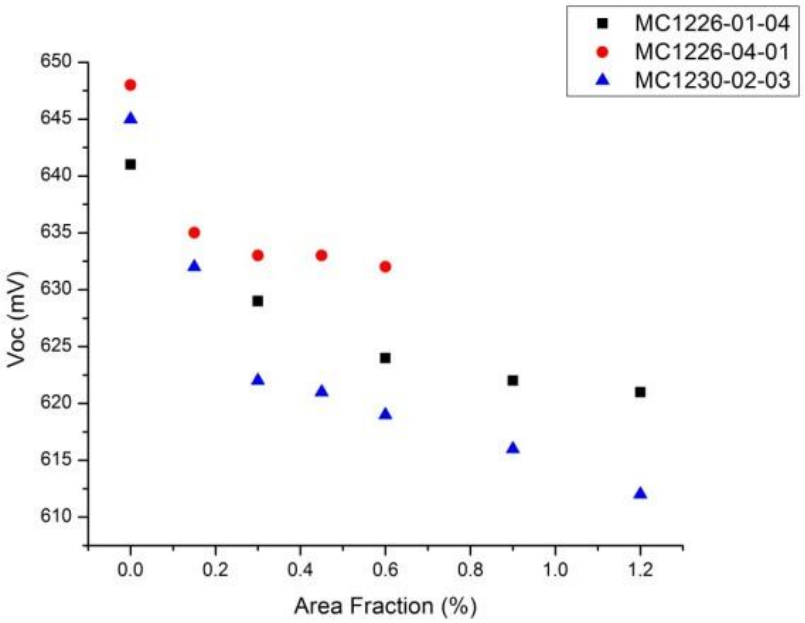


Figure 5.9 Schematic of front junction with SiNx blocking layer and LFC on the back side.



Fgiure 5.10 Actual cell open circuit voltage drop v.s. LFC area fraction up to 1.2%. The Voc at 0% LFC area fraction is implied Voc derived from lifetime test before cell metallization.

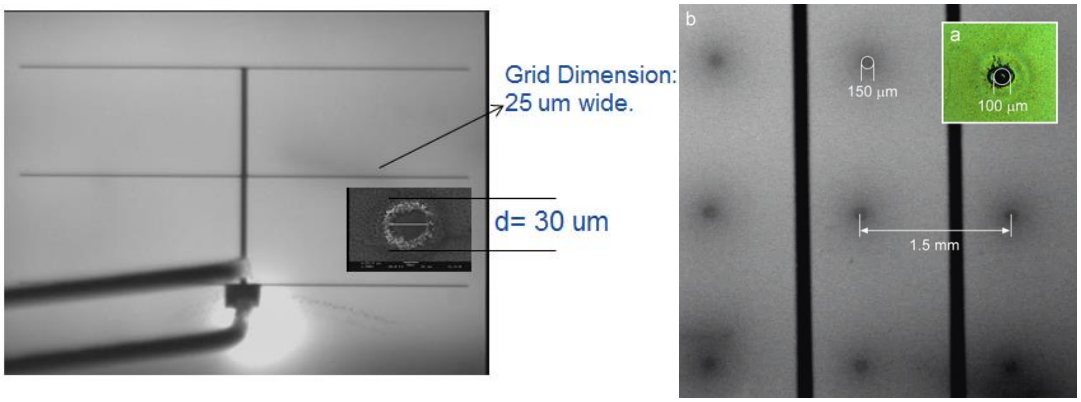


Figure 5.11 Electroluminescence image of a front junction cell with LFC. Left picture is EL mapping of a n-type solar cell with LFC in this thesis, while right picture is EL mapping of a p-type solar cell with LFC [5]. Note no visible LFC related recombination center is observed in the left image.

Table 5.3 Device results of LFC on front junction solar cells with n a-Si back surface field.

	V_{OC} (mV)	J_{SC} (mA/cm^2)	FF (%)	Eff (%)
MC1311-02	690	32.5	73.5	16.5
MC1311-02 LFC	670	32.0	73.3	15.7
MC1334-01	707	32.9	71	16.5
MC1334-01 LFC	683	32.5	70.9	15.8

Finally we selected 2 standard front junction solar cells with n-type a-Si layer back surface field instead of the SiNx blocking layer. The rear side metal is still Al-Sb-Ti stack layer. In this case, since there is already n-type amorphous silicon layer between the metal and silicon wafer, a good ohmic contact should already be establish without LFC. The LFC only induces the damage and reduces the V_{OC} without contributing to the ohmic base contact formation. In this way, the V_{OC} loss due to the passivation loss can be de-coupled from the contact formation. The solar cell parameters before and after LFC are listed in table 5.3. The V_{OC} drops by 20-25 mV for both cells, for a LFC area fraction of 0.15%. The drop in open circuit voltage is consistent with test structure and SiNx-back front junction device results. The fill factor remains almost unchanged since the LFC is not contributing to the base contact.

We also selected one piece of rear-SiNx front junction solar cell with LFC for Electroluminescence mapping characterization. In Martin's work the LFC induced recombination centers are significant in EL mapping on a heterojunction solar cell

precursor with over 700 mV implied open-circuit voltage. Interestingly, we were not able to see the same periodic recombination centers associated with LFC array in our FJ solar cell. One possible explanation is the starting iV_{OC} is only around 630mV in this case, and the contrast between LFC and background is less significant. This is also indicated by the actual Voc of 639mV for the same device after LFC.

In summary, when lasing condition is properly chosen, the bulk defect could be completely avoided based on the cross section SEM and TEM investigation. The surface recombination loss due to laser firing was analyzed and a recombination rate for the LFC area was estimated to be ~20,000 cm/s which would result in a 30-40 mV loss in Voc for 0.15% LFC area fraction. This is usually true when the starting lifetime and iVoc is high for the solar cell precursor. The LFC induced depassivation effect is less significant for implied Voc less than 650 mV.

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Chapter 6

LASER FIRED CONTACT ON HETEROJUNCTION DEVICES

In chapter 4 and 5, the contact properties and the impact on passivation of LFC have been discussed mostly on test structure level. We have concluded that the specific contact resistance of LFC is generally below 10 mΩcm^2 and the laser induced damage is limited to the surface de-passivation when the lasing condition is properly chosen. A 0.15% LFC area fraction usually causes a ~20-30 mV drop in open-circuit voltage for a device precursor with iV_{OC}>680 mV. Based on these properties, the LFC should be suitable for device application. In this chapter, LFC will be applied on both front junction solar cells and IBC solar cells. Various blocking layers between metal stack and wafer have been investigated and their critical roll on device performance will be discussed.

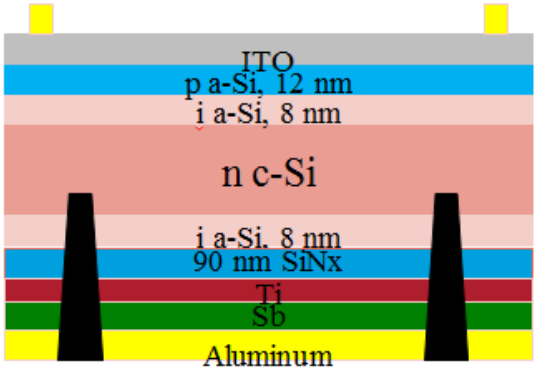


Figure 6.1 Schematic of front junction with i a-Si/ SiNx stack blocking layer and LFC.

6.1 LFC through non-Doped Layer SiN_X

Although in chapter 1, the purpose of LFC in this thesis is to fire through an oppositely doped p a-Si layer form a base contact with n-type wafer. In most LFC studies, the blocking layer is a dielectric layer rather than a doped layer, independent of the doping type. In this study, a stack passivation structure consisting of i a-Si/ SiN_X is applied on rear surface as passivation and blocking layer. The i a-Si layer is 8 nm thick and does generally impede the ohmic contact. The complete structure of the device with i a-Si/ SiN_X is shown in Figure 6.1. Textured n-type FZ wafers with 1-5 Ω cm resistivity were used for both test structures and solar cell devices. The wafers were randomly textured with pyramidal structures of 1-3 μm and were cleaned by organic solvents, Piranha solution (mixture of 1:3 H_2O_2:H_2SO_4) and HF before a-Si or SiN_x was deposited by Plasma Enhanced Chemical Vapor Deposition (PECVD). All metal layers were deposited by Electron Beam Evaporation and ITO layer was deposited by Sputtering.

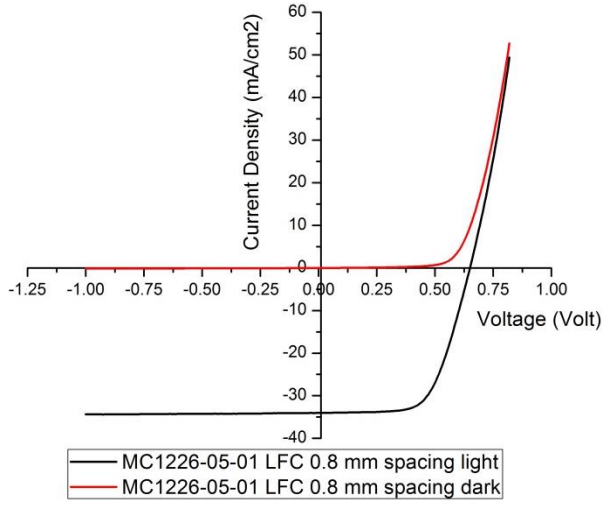


Figure 6.2 J-V characteristics of FJ solar cells with SiN_X rear passivation layer after LFC. Before LFC both dark and light J-V curve are open-circuit due the no ohmic contact at the rear side of the device. After LFC a fully functional solar cell is formed proving the success of contact formation fired through SiN_X layer.

The lifetime of the solar cell precursors without metallization was measured and determined to be generally around 100 us to 150 us. In Figure 6.2 the particular cell has a lifetime of 180 us and iV_{OC} of 649mV. After 0.15% area fraction of LFC, the actual V_{OC} reached 650mV, with a FF of 63.5%, Jsc of 34.1 mA/cm^2 and final efficiency of 14.0%. The V_{OC} did not drop noticeably compared to the implied $V_{OC.}$ This is in agreement with the test structure result in chapter 5 that when the starting lifetime is in the mediocre range where the V_{OC} degradation is less significant. The loss in V_{OC} is mainly due to the low lifetime in the surface passivation. The reason is that the deposition of SiN_x in PECVD requires at least 200 C to avoid dust in the chamber.

The deposition time for SiN_x is at least 20 minutes, including the pre-heating time. The emitter p a-Si layer deposited prior to SiN_x usually will degrade after such thermal history, therefore the initial lifetime of this structure is usually not as high as the standard FJ structure.

To improve the precursor lifetime, an alternative way of fabrication was to deposit the emitter p a-Si layer after SiN_x. However it was not successful since the SiN_x is a dielectric layer which changes the potential of the sample carrier holder and thus changes of emitter deposition condition. The unusual high voltage during emitter deposition caused by dielectric SiN_x on substrate resulted in poor emitter quality. Although those cell precursors showed very high initial lifetime above 2000 us, they are not able to develop a normal diode J-V curve as Figure 6.6. It would be possible to improve the emitter quality by changing the sample carrier after SiN_x deposition. However this would require vacuum break where the samples would be physically taken out of chamber which could lead to the surface oxidation and potential

contamination. The precursor lifetime did not improve significantly with the vacuum break method and remain from 100 us to 250 us. Although the FJ LFC with SiN_x did not yield very high V_{OC}, the purpose of this device structure was not to make champion cell but to serve as a first test structure for devices such as FJ with doped blocking layer and IBC cells with LFC. We are still able to achieve a 650 mV open-circuit voltage with SiN_x blocking layer for FJ LFC device indicating the suitability of LFC on device. It is also confirmed that the drop in open-circuit voltage is smaller or could be almost insignificant when starting from mediocre implied open-circuit voltage. This is suggesting when starting from a high iV_{OC} the, the expected V_{OC} could be at least around 630 mV as shown in Figure 6.3 and Table 6.1. Although the front-junction usually cannot start from a high initial lifetime and thus a high iV_{OC} due to its unique structure, there is no such problem for IBC cells. We will go back to examine the V_{OC} after LFC on IBC cells in later part of this chapter. Finally, through careful processing the current FJ-LFC device with best overall efficiency is presented in Figure 6.4 and Table 6.2. The V_{OC} is 639 mV and FF is 71.9% resulting in an overall efficiency of 15.2%. Note that the current highest FJ-LFC with a heterojunction is around 16% [1]. This is a demonstration that LFC technique could at least obtain low series resistance and reasonable V_{OC} at the same time.

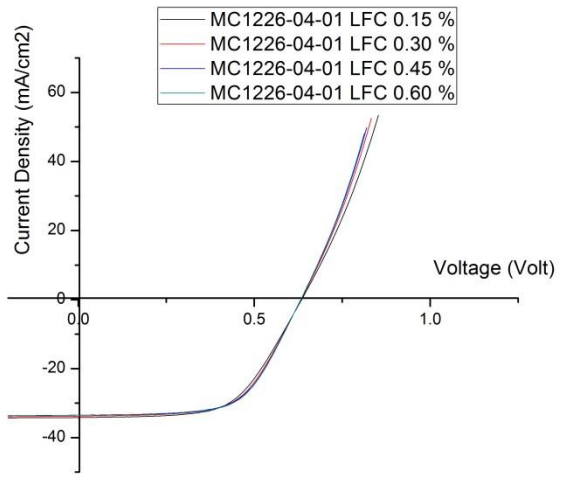


Figure 6.3 J-V characteristics of SiN_X -FJ solar cells with increasing area fraction of LFC.

Table 6.1 Performance parameters of SiN_X -FJ solar cells with increasing area fraction of LFC.

LFC fraction (%)	Voc (mV)	Jsc (mA/cm2)	FF (%)
0.15	635	34.2	59.3
0.30	633	33.8	61.0
0.45	633	33.5	62.0
0.60	632	33.5	62.4

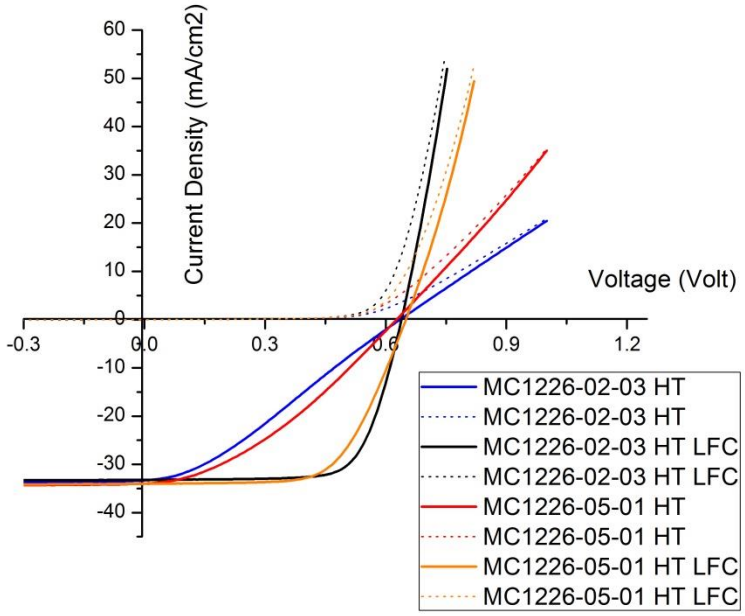


Figure 6.4 FJ-SiNx devices with optimized deposition, heat treatment and LFC. In MC 1226-02-03 a 15.2% efficiency device was obtained.

Table 6.2 Parameters of FJ-SiNx devices with optimized deposition, heat treatment and LFC.

Piece	**Voc (mV)**	**Jsc (mA/cm2)**	**FF (%)**	**Rs (Ohm*cm^2)**	**Eff (%)**
MC1226-05-01	650	34.1	63.5	2.5	14.0
MC1226-02-03	639	33.2	71.8	1.8	15.2

6.2 LFC Through Doped Layer P-Type Amorphous Silicon

We mainly use FJ-SiNx device as a test structure to verify the suitability of LFC on heterojunction device and found that both low series resistance and V_{OC} above

630 mV could at least obtain at the same time. However, the purpose of LFC is to obtain good contact in a device where an opposite doped layer is present between metal and n-type wafer base. Based on the information from FJ-SiNx devices performance, we fabricated another FJ-p a-Si device as test structure, shown in Figure 6.5. Compared with Figure 6.1, the only difference is that the blocking layer SiNx was replaced with a 20 nm thick p-type amorphous silicon layer. The deposition conditions are the same used in our standard IBC-SHJ devices to reproduce the same quality and doping level of p a-Si layer. All other processing steps are similar with FJ-SiNx devices.

The device performance of FJ-p a-Si device is drastically different from FJ-SiNx device, after LFC. As shown in Figure 6.6 the device only has slightly over 500 mV $V_{OC,}$ less than 30 mA/cm2 J_{SC} and S-Shape light J-V curve resulting in 63.8% FF. The efficiency is only 9.6% for the FJ-p a-Si device after LFC.

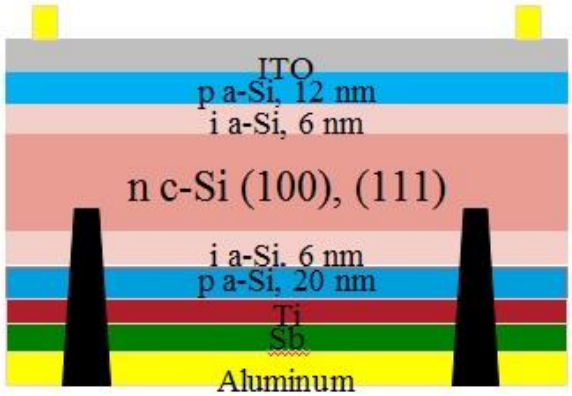


Figure 6.5 Schematic of front junction with i a-Si/ p a-Si stack blocking layer and LFC.

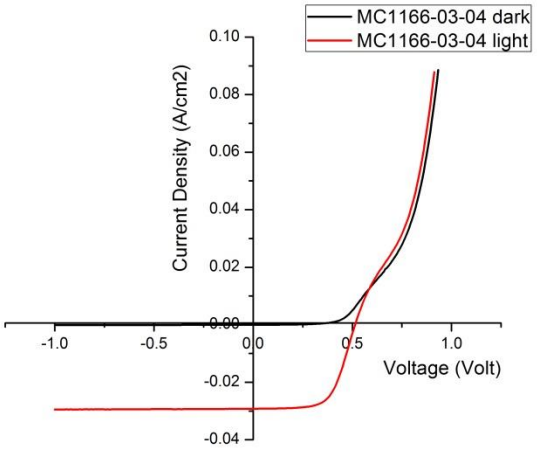


Figure 6.6 J-V characteristics of FJ-p a-Si solar cells after LFC.

The first suspicion is that the LFC was not forming well enough ohmic contact resistance and delivering too much damage, causing the S-shape curve and low parameters. However, when carefully evaluating the J-V curve and other data, we found it is not the case. Figure 6.7 shows the J-V curve of a FJ-p a-Si device after LFC together with a standard FJ device with n a-Si layer on the rear side without a LFC. The series resistance at Voc of FJ-p a-Si device is much larger than standard FJ device due to the S-shape of the light J-V curve. However, when evaluating the dark J-V curve at high forward bias both devices showed low series resistance. The reason of choosing forward bias dark curve to analysis series resistance is that the resistance is no longer dominated by the diode but by the ohmic contacts of the device. The R_S is 1.6 Ωcm^2 and 1.4 Ωcm^2 for FJ-p a-Si LFC device and standard device, respectively. This means the laser fired rear base contact of FJ-p a-Si device is not responsible of the low resistance of the device. The morphology and EDS results of the device also showed that the LFC exhibited a properly-fired characteristic, as described in chapter 4. This type of LFC through p a-Si usually yield a specific contact resistance less than

5 Ωcm^2 which is sufficient for a LFC area coverage between 0.15% to 0.3% for this case.

Next, to determine whether the low V_{OC} was due to the high recombination rate at device rear surface due to laser induced damage, we etched off the front ITO and metal grids together with rear side metal stack, to create a structure for lifetime testing of LFC as described in chapter 5. For this sample set, all devices precursors have an initial iV_{OC} between 615 mV to 640 mV. After etching the device, the lifetime was ~ 40 us with an iV_{OC} of 610 mV indicating the laser induced damage only limits the device V_{OC} up to ~ 610 mV which is more than 100 mV higher than the actual device $V_{OC.}$

After excluding both poor contact property and poor recombination property, it was concluded that the poor device performance is due to the actual structure of device rather than LFC. To be specific, the structure responsible is the rear side p a-Si/ metal structure. The reason is that by using this laser firing the stack layer with Sb through p a-Si to form a base contact with n c-Si, a pathway for majority carriers is created. However, this cannot prevent the minority carriers from being collected by the rear side p a-Si layer where no LFC but an external contact is present. The oppositely doped layer without contacting the external metal is called 'floating collector' [2]. The doped layer can form a floating junction with the base wafer and has been widely used as a method to passivation in silicon solar cells, especially in diffused junction solar cells. Excellent surface passivation quality has been achieved via floating junction method. [3] Some architectures of device using the floating junction passivation are shown in Figure 6.9 [4] and Figure 6.10 [5]. In both cases, most of the area of the rear side of device is passivated by an oppositely doped layer.

For Figure 6.9, in the interdigitated back buried contact device, the floating collector p^+ layer is separated from the base contact by a thermally grown insulating SiO_2 layer. For Figure 6.10, both the floating collector and base contact are patterned to ensure they do not touch each other.

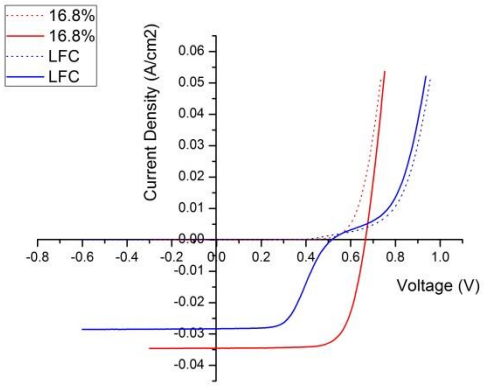


Figure 6.7 J-V characteristics of FJ-p a-Si solar cells after LFC together with standard FJ with n a-Si rear side without any LFC.

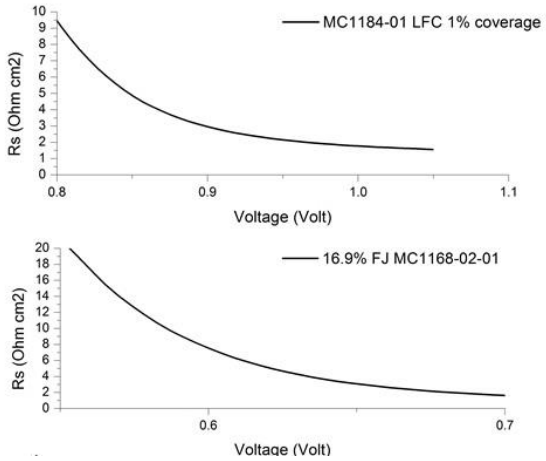


Figure 6.8 Series resistance comparison between FJ-p a-Si device and standard FJ device

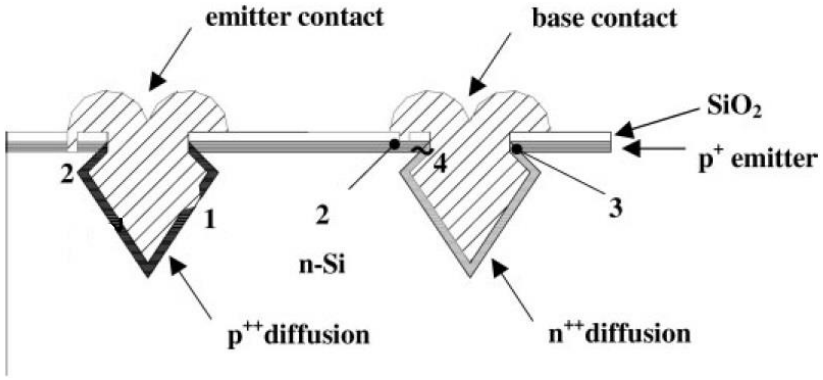


Figure 6.9 Interdigitated Back Buried Contact (IBBC) device architectures with 4 different parasitic shunt sources. [4]

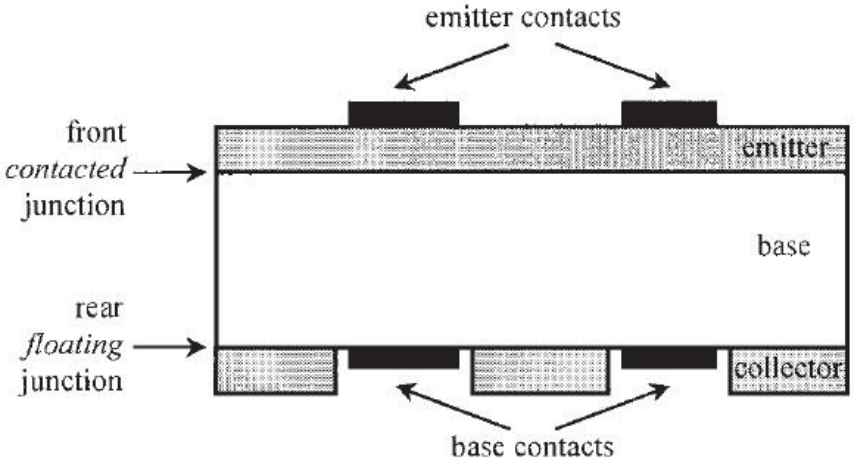


Figure 6.10 Front junction device with rear floating junction passivation. [5]

Once the base contact is in touch with floating collector, however, a pathway of parasitic shunt is created to allow minority carrier to be collected through floating collector. For example, in Figure 6.9, there are 4 possible pathway of parasitic shunt: 1) uncompensated diffusion in groove; 2) pinholes through dielectric layer; 3) diffusion overlap region and 4) laser processing induced defect.

Since the doped layer is achieved through diffusion in IBC device, the sheet resistance is relatively low compared with heterojunction device. Therefore, a very

small fraction of base contact metal touching the floating collector could result in serious device performance degradation because the lateral conductance within the floating collector is much higher.

For the test structure shown in Figure 6.5, the sheet resistance of p-type doped amorphous silicon layer is orders of magnitude higher than diffused doped layer, the contact area is almost 100% except for the LFC area. As shown in Figure 6.11, holes generated in the bulk could be collected by either front emitter p a-Si, or the rear p a-Si layer.

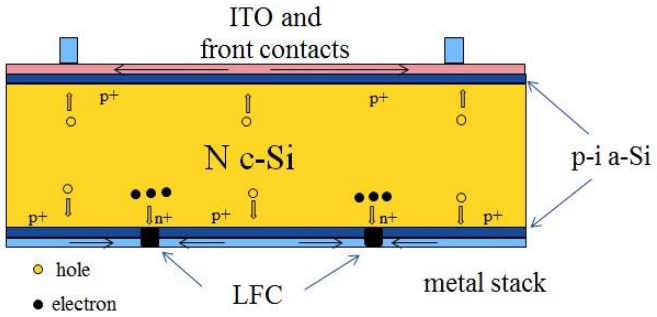


Figure 6.11 FJ-p a-Si device with rear LFC. Minority carriers can be collected either by the front junction or the rear junction. When collected by the rear junction, the holes will quickly recombine with majority carrier through the rear contact.

To validate our hypothesis of the reason of low performance of p a-Si LFC device, the Ebers-Moll equivalent circuit [5] was used to analyze the shape of the J-V curve of the device. The Ebers-Moll circuit was originally used to describe current flow in a transistor [6]. This model was then extensively used to characterize the parasitic shunt induced by floating junction. [7][8] When the shunt resistance is infinite, all current flows through the rear side floating junction will be returned back to the front junction. When the shunt resistance is not infinite some portion of current flows into rear floating junction will not be returned to the base and front junction and

is therefore lost from the solar cell. When the shunt resistance is very small the rear floating junction behaves as a surface with infinite recombination velocity since no current will be re-injected back to the solar cell. The detailed discussion could be found at [7].

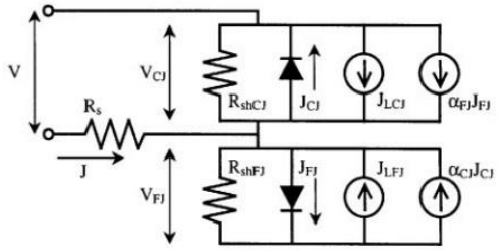


Figure 6.12 Modified Ebers-Moll equivalent circuit for a floating junction passivated solar cells.

With the parasitic shunt serving as a recombination site, the kink which represents the transit from bad to good surface passivation quality will present in the J-V curve. The smaller (pooer) the parasitic shunt, the lower voltage the kink occurs. If the shunt resistance is high enough, the transition will occur at lower voltage; if the shunt resistance is small then the transition will occur at higher voltage since larger voltage is needed to let the front emitter junction collect most of carriers. The simulated results from Keith group [7] are shown in Figure 6.13. If the kink happens before or around the maximum power point it will severely affect the device performance. We have measured LFC front junction device with p a-Si back together with a standard front junction device without any LFC as reference. The dark J-V curve is plotted as shown in Figure 6.14. Local idea factor is strongly dependent of voltage and is also plotted as shown in Figure 6.15. The kink for FJ-LFC p a-Si device happened around 550 mV and resulted in a local ideality factor larger than 7.

Compared with Figure 6.7 one could find the transit happened way before the maximum power point. On the other hand the standard FJ device showed no significant kink all around the voltage range being examined.

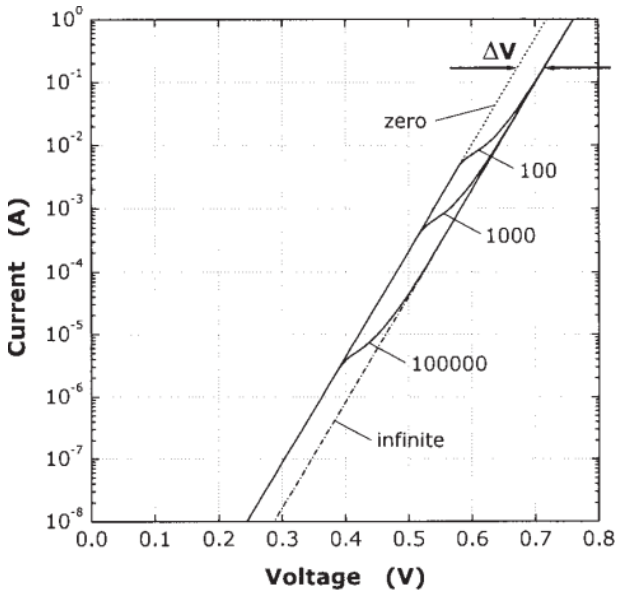


Figure 6.13 Dark J-V curves generated with Ebers-Moll model with different parasitic shunt resistance caused by rear floating junction. [7]

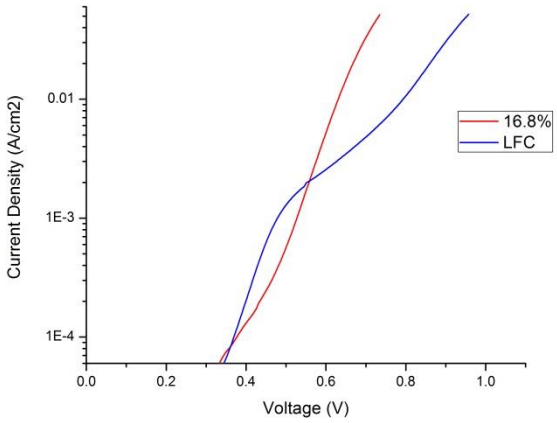


Figure 6.14 Comparison of dark J-V curve of FJ-LFC p a-Si and standard FJ device.

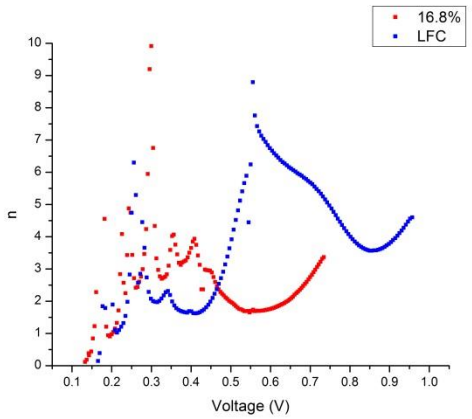


Figure 6.15 Comparison of local ideality factor of FJ-LFC p a-Si and standard FJ device.

To eliminate or relieve the detrimental effect from the floating junction, a SiN_X layer was inserted between LFC metal stack and p a-Si. With the dielectric SiN_X layer, the interface of p a-Si/ metal stack where there is no LFC will no longer exist and the rear side pathway for minority carrier to pass through is eliminated. The structure of the FJ-LFC p a-Si/ SiN_X is shown in Figure 6.16.

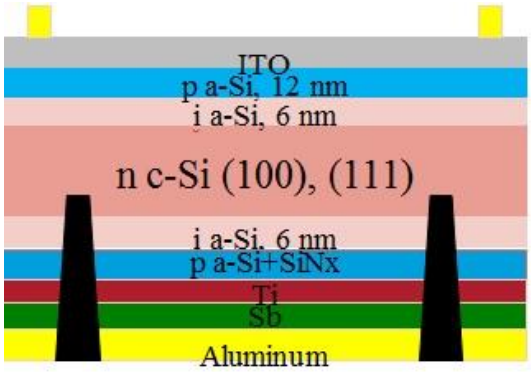


Figure 6.16 Schematic of front junction with p a-Si/ SiN_X stack blocking layer and LFC.

The specific contact resistance of LFC through SiN_X and p a-Si stack was examined with lateral test structure as discussed in chapter 4. The specific contact

resistance was calculated to be around 1 mΩ-cm^2 which is sufficient for device application. The open circuit voltage of the device increased significantly to 620-630 mV from ~550 mV. Due to the non-optimized front contact quality those device show high series resistance and thus low overall performance. Since the front junction device only serves as test structure for IBC-SHJ device, we did not pursue the highest overall efficiency but a proof of concept that 1), the LFC is suitable for n-type crystalline silicon solar cell device and 2), the p a-Si/ metal stack rear side device architecture will yield low device performance due to parasitic shunt, and a non-doped dielectric blocking layer will greatly reduce the detrimental effect of parasitic shunt.

6.3 LFC on IBC-SHJ Devices with Varies Structures On N-strips

With the knowledge we learnt from test structures in chapter 4 and chapter 5, and the FJ-LFC device results discussed above, we applied LFC on IBC-SHJ devices without laser isolation which will be discussed in chapter 7. IBC rear-side patterning was accomplished by photolithography and mask deposition.

We started with the same device structure with blank p a-Si deposition on the rear side. Instead of n and p strips by laser, the patterning was accomplished by a mask deposition (Figure 6.17 left) during metallization process. After metallization, LFC was applied on n strips to achieve base contact. The finished device has structure as plotted in Figure 6.18 right. By using the shadow mask, the four devices with different emitter coverage from 82% to 89% can be fabricated without using any photolithography processing. The picture of actual device is shown in Figure 6.18.

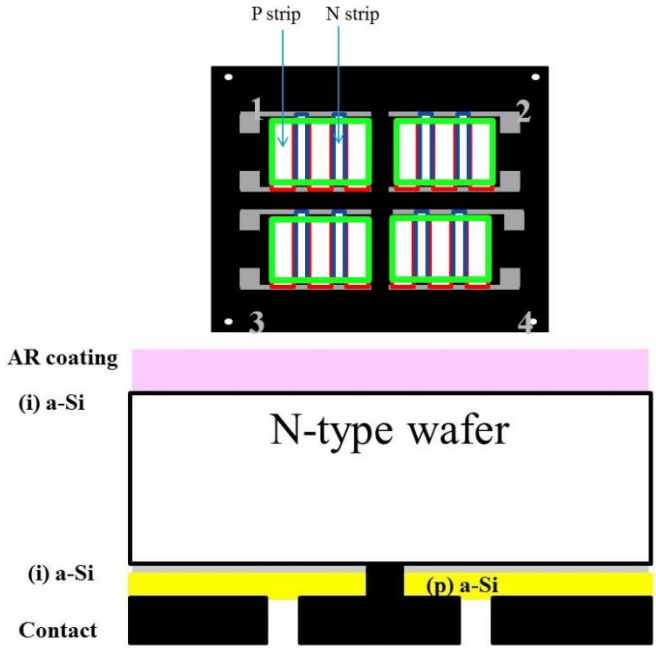


Figure 6.17 Left: Metallization shadow mask for all p a-Si rear IBC-SHJ-LFC device; Right: Structure of all p a-Si back IBC-SHJ with LFC patterned with metallization shadow mask

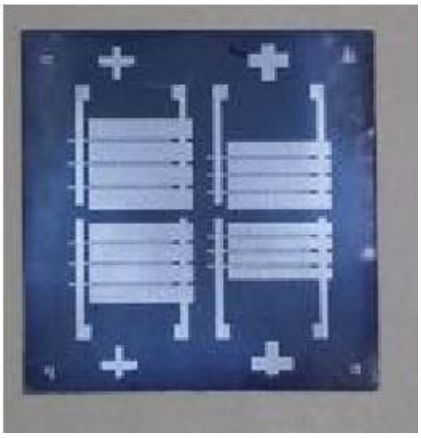


Figure 6.18 Sample with four all p a-Si back IBC metallized through shadow mask.

LFC was performed on the n-strips of the device. Since there was lateral transport of carriers, a higher area fraction of LFC was required to achieve good series resistance and overall cell efficiency. Typically the area fraction needs to be from 3-5% of the n strip, and even higher if a high resistivity 8-10 Ω·m wafer (5-8%) is used. Before any LFC, the device was basically a p-n-p structure, with two diodes connected in series. Therefore, the dark J-V curve was open-circuit, while the light J-V curve showed conduction due to the illumination.

After LFC, the p-n junction was shorted by local metal stack-base contact and a diode curve was formed for both dark and light J-V curve. Both JV curves before and after LFC were plotted in Figure 6.19. The device results were shown in Table 6.1. The all p a-Si back IBC-LFC shows 590 to 610 mV V_{OC}, which is increasing with the emitter fraction. The series resistance of the device has the reverse trend compared with V_{OC} since smaller area of n-type contact will increase the series resistance when LFC area fraction is kept same. The overall efficiency of the device is still, however, much lower compared with standard IBC-SHJ devices. Similar with FJ-LFC device, we measured lifetime after etching off the rear side metal stack to evaluate whether the low V_{OC} is caused by laser damage. The average implied V_{OC} of the sample with 4 cells is over 640mV, which is at least 30 mV higher than any of the cell.

Table 6.3 Device parameters of IBC-LFC with different emitter coverage (EC) after LFC. The EC is defined as the area of emitter on all p strips over the total area of device. The n strips are covered by p a-Si.

EC %	Voc (mV)	Jsc mA/cm^2	FF %	Roc $Ohm\text{-}cm^2$	Eff %
89	610	30.6	63.2	4.0	11.8

87	606	30.3	63.3	3.7	11.6
86	597	30.4	65.6	3.6	11.9
82	589	28.5	66.7	3.4	11.2

In fact, we saw the V_{OC} went up with the increase of LFC area fraction. This is contradicting the trend we saw on FJ-LFC device, where higher LFC area fraction generally results in higher FF due to lower series resistance but lower V_{OC} due to loss of passivation. The relationship of these parameters with LFC area fraction was shown in Figure 20 and Figure 21. This is suggesting that in the case of IBC-LFC the V_{OC} is not limited by surface passivation, but by the unwanted collection and recombination on the n strips.

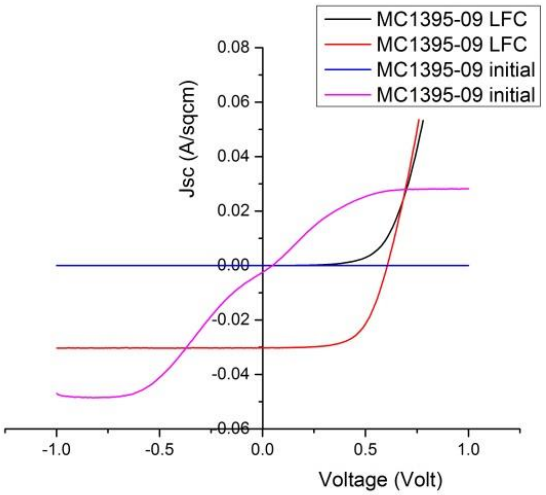


Figure 6.19. J-V curves of IBC-LFC device with all p a-Si back, both before and after LFC.

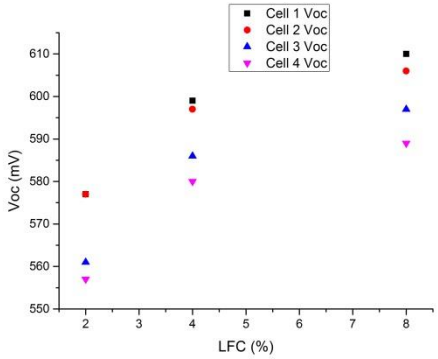


Figure 6.20. IBC-LFC with all p a-Si back device parameter V_{OC} increases with larger LFC area fraction.

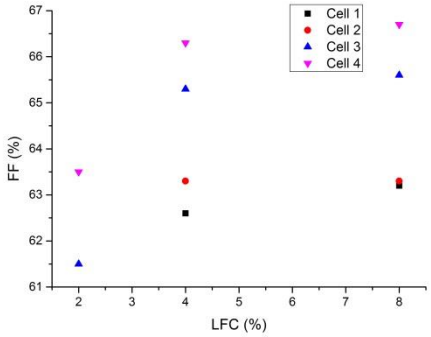


Figure 6.21. IBC-LFC with all p a-Si back device parameter FF increases with larger LFC area fraction.

We have designed another set of experiments to evaluate the effectiveness and potential damage of LFC on IBC-SHJ devices. Two IBC-SHJ devices fabricated with standard photolithography were selected.

The first IBC-SHJ device has efficiency of 17.4% and good device parameters all as shown in the first row in Table 6.4. After LFC, the series resistance and FF almost remained unchanged as expected since the n a-Si/ metal stack interface is already a good ohmic contact. The V_{OC} and J_{SC} degraded from 654 mV and 37.7 mA/cm^2 to 643 mV and 36.6 mA/cm^2 respectively. The decrease of both parameters are small and therefore the laser damage cannot be responsible for the ~600 mV V_{OC} and less than 30 mA/cm2 J_{SC} of IBC-LFC with all p a-Si back.

The second IBC-SHJ device has same processing steps as the first one. However, due to the incomplete development of photoresist, additional SiNx was left on n strip blocking the contact formation between metal stack and n a-Si/ n c-Si base. Therefore, the device shows very high series resistance and low Fill Factor before LFC, as shown in Figure 6.23 and Table 6.5. Since there is no p a-Si floating collector, after LFC the J-V curve was restored to normal working solar cell. The V_{OC} reached 660 mV together with a 3.0 Ohm*cm^2 R_{OC} and 65.8% FF. The total efficiency is 15.2% percent for non-optimized Processing. From those three sets of devices which have different structure on n strips 1) p a-Si; 2) n a-Si and 3) SiNx/ n a-Si, we can conclude that LFC can be a reliable processing step in IBC-SHJ device fabrication. However, the p a-Si/ metal stack structure must be avoided on n strip even with LFC. Therefore a single shadow mask deposition of metal for p strips and n strips patterning is not feasible for high efficiency device. This requires additional patterning techniques and/ or mask depositions.

We started with the efforts to reduce the steps of other etching and deposition steps in IBC-SHJ processing with LFC technique to form base contact. Standard IBC-SHJ device requires up to three steps of photolithography to remove SiNx/ p a-Si stack before n a-Si deposition on n strips. For IBC-SHJ with LFC, no n a-Si is required on n strip as long as the unwanted floating collector structure n c-Si/ p a-Si/ metal stack is not present. With this advantage we have developed processing flows with less steps of etching and PECVD deposition. The IBC-SHJ-LFC device processing flow is plotted and compared with standard IBC-SHJ processing flow as shown in Figure 6.24. Both processing flows require front side passivation, anti-reflection and rear side passivation. The first photolithography step for p strip patterning is also identical.

After the second photolithography to pattern the n strip, the standard IBC-SHJ processing will need HF etching to remove the blocking SiN_X layer followed by PECVD n a-Si deposition. The purpose of these two steps is to form good base contact with n c-Si/ i a-Si/ n a-Si/ metal structure. If the developing of the second lithography is not complete, or the etching is not well controlled, the SiN_X layer may not be completely removed which will result in poor contact quality, similar as situation shown in Figure 6.23. For IBC-SHJ-LFC processing, after the second photolithography, neither SiN_X etching nor n a-Si PECVD deposition is required since the base contact will be formed by firing metal stack through metal stack through blocking layer. With optimized processing steps, the best IBC-SHJ-LFC has achieved efficiency of 16.9%, with Voc=0.645V, Jsc=36.2 mA/cm^2, FF=72.1%. The J-V curve before and after LFC for this device was plotted in Figure 6.25.

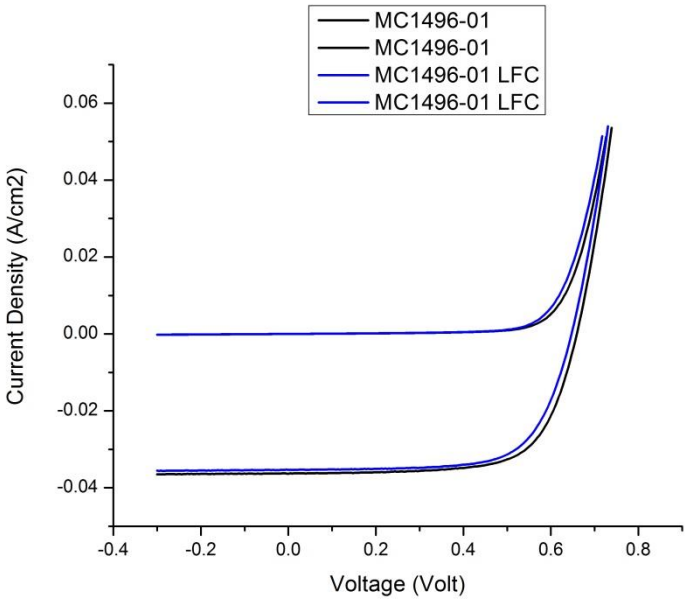


Figure 6.22 J-V curve of standard IBC-SHJ with n a-Si on n strip, before and after LFC. Patterns developed by photolithography. For good device, LFC cannot improve series resistance, and will induce some degradation of both V_{OC} and J_{SC}.

Table 6.4 Device parameters of standard IBC-SHJ with n a-Si on n strip, before and after LFC. Patterns developed by photolithography. 5% LFC was applied on device.

	Voc (mV)	Jsc (mA/cm^2)	FF (%)	Roc ($Ohm*cm^2$)	Eff (%)
Before LFC	654	37.7	70.4	1.9	17.4
After LFC	643	36.6	70.2	2.0	16.5

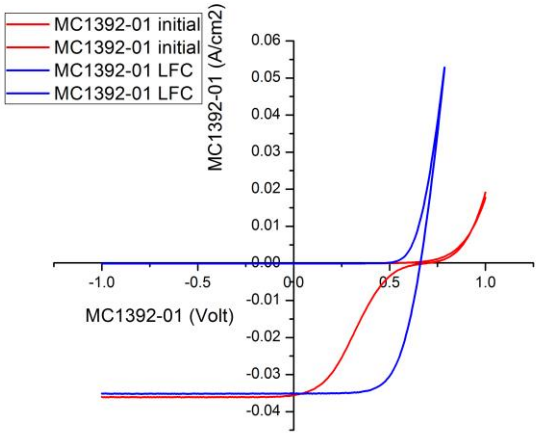
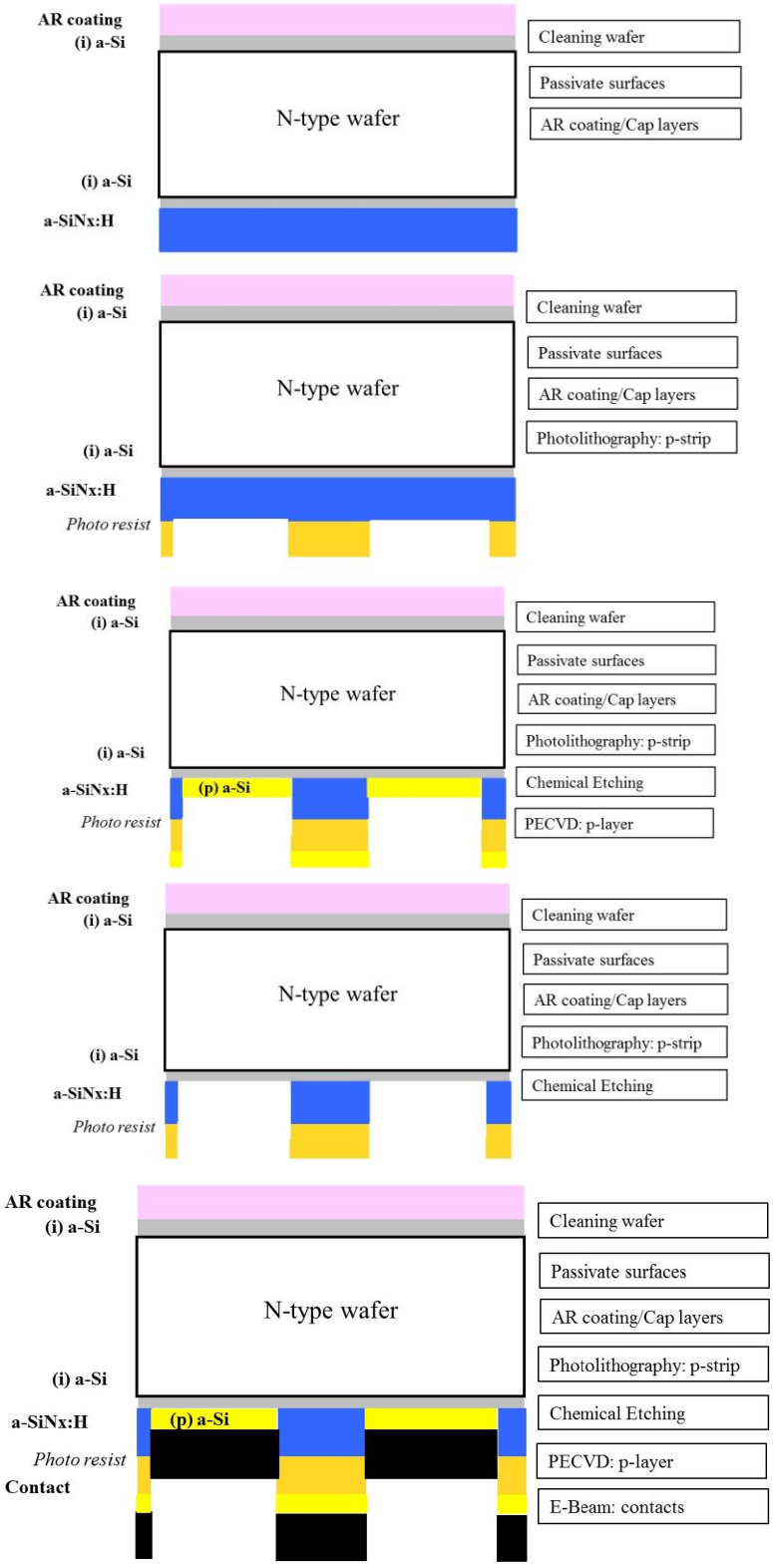


Figure 6.23 J-V curve of standard IBC-SHJ with n a-Si on n strip, before and after LFC. Additional SiNx layer was present between n a-Si and metal stack due to incomplete developing in photolithography process. For IBC device with contact problem on n strip, LFC can restore the J-V curve of device to normal working diode.

Table 6.5 Device parameters of standard IBC-SHJ with n a-Si and additional SiN_X on n strip, before and after LFC. Patterns developed by photolithography. 5% LFC was applied on device. Before LFC device was limited by series resistance (FF=26%, R_{OC}=155 Ohm*cm^2). After LFC R_{OC} reduced to 3.0 Ohm*cm^2 and FF increased to 65.8%, resulting total efficiency of 15.2%.

	Voc (mV)	**Jsc (mA/cm2)**	**FF (%)**	**Roc (Ohm*cm^2)**	**Eff (%)**
Before LFC	687	35.6	26	155	6.4
After LFC	660	35.2	65.8	3.0	15.2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(i) a-Si
a-SiNx:H
Cleaning wafer
Passivate surfaces
AR coating/Cap layers
AR coating
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N-type wafer
(i) a-Si
a-SiNx:H
Photo resist
Cleaning wafer
Passivate surfaces
AR coating/Cap layers
Photolithography: p-strip
AR coating
(i) a-Si
N-type wafer
(i) a-Si
a-SiNx:H
(p) a-Si
Photo resist
Cleaning wafer
Passivate surfaces
AR coating/Cap layers
Photolithography: p-strip
Chemical Etching
PECVD: p-layer
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a-SiNx:H
Photo resist
Cleaning wafer
Passivate surfaces
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Photolithography: p-strip
Chemical Etching
AR coating
(i) a-Si
N-type wafer
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a-SiNx:H
(p) a-Si
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Contact
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Passivate surfaces
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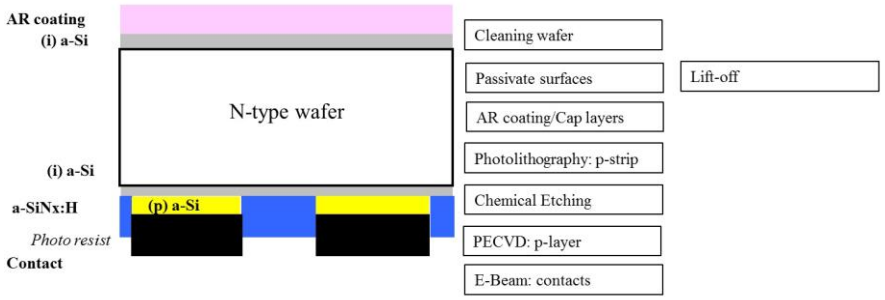
Photolithography: p-strip
Chemical Etching
PECVD: p-layer
E-Beam: contacts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Contact
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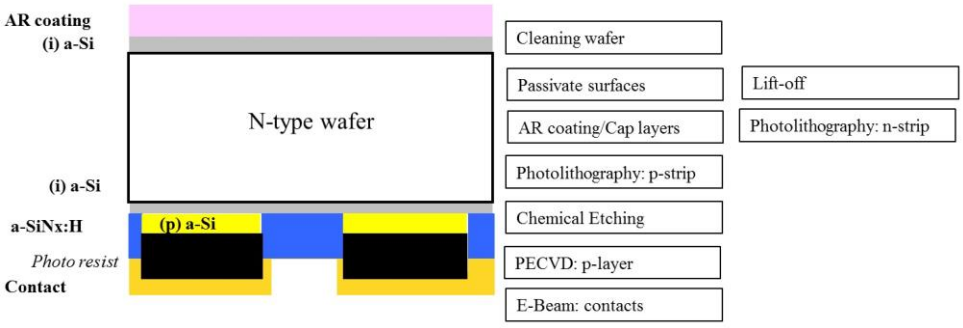
Chemical Etching
PECVD: p-layer
E-Beam: contacts
Lift-off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(p) a-Si
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Contact
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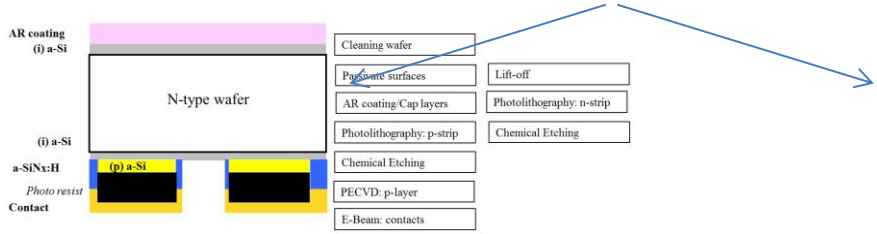
Chemical Etching
PECVD: p-layer
E-Beam: contacts
Lift-off
Photolithography: n-strip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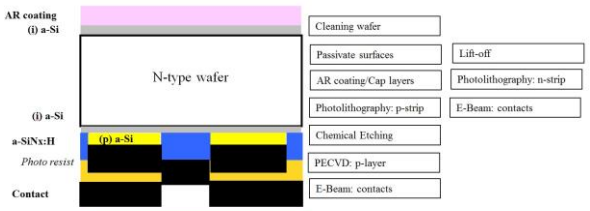
Chemical Etching
PECVD: p-layer
E-Beam: contacts
Lift-off
Photolithography: n-strip
Chemical Etching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Passivate surfaces
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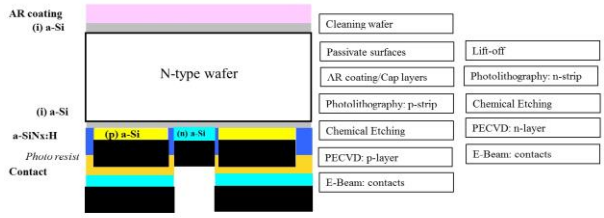
Chemical Etching
PECVD: p-layer
E-Beam: contacts
Lift-off
Photolithography: n-strip
E-Beam: contacts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(n) a-Si
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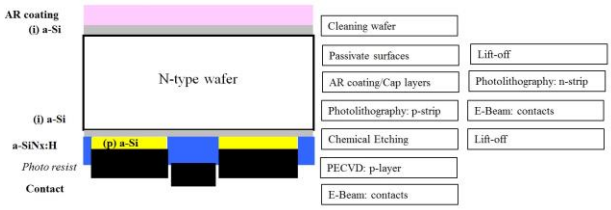
Contact
Cleaning wafer
Passivate surfaces
AR coating/Cap layers
Photolithography: p-strip
Chemical Etching
PECVD: p-layer
E-Beam: contacts
Lift-off
Photolithography: n-strip
Chemical Etching
PECVD: n-layer
E-Beam: contacts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(p) a-Si
Photo resist
Contact
Cleaning wafer
Passivate surfaces
AR coating/Cap layers
Photolithography: p-strip
Chemical Etching
PECVD: p-layer
E-Beam: contacts
Lift-off
Photolithography: n-strip
E-Beam: contacts
Lift-off

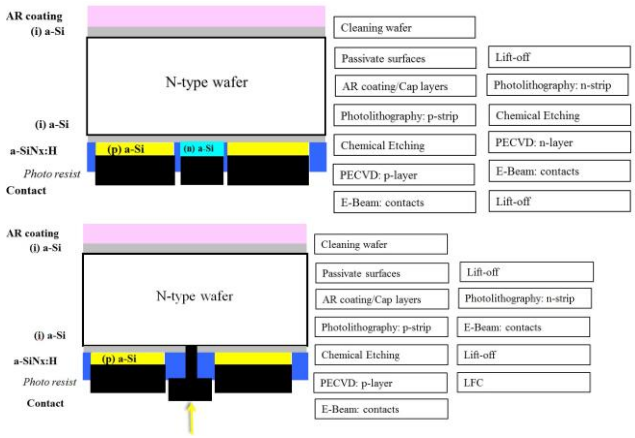


Figure 6.24 Standard IBC-SHJ Processing flow and IBC-SHJ-LFC processing flow. Both flows have same processing steps at the beginning until the second photolithography. After the second photolithography, standard processing needs additional step of HF etching to remove SiN_X layer. Additional step of n a-Si deposition after etching is also required to form the base contact. For IBC-SHJ-LFC, since the base contact is formed by LFC rather than n a-Si/ metal structure, neither the HF etching nor the PECVD n a-Si deposition is required. The processing flow can skip the two steps and jump to final metallization of Al-Sb-Ti stack and lift off.

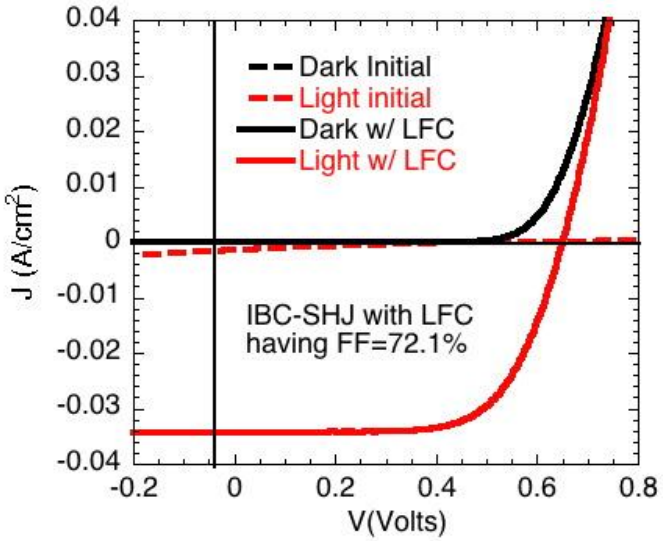
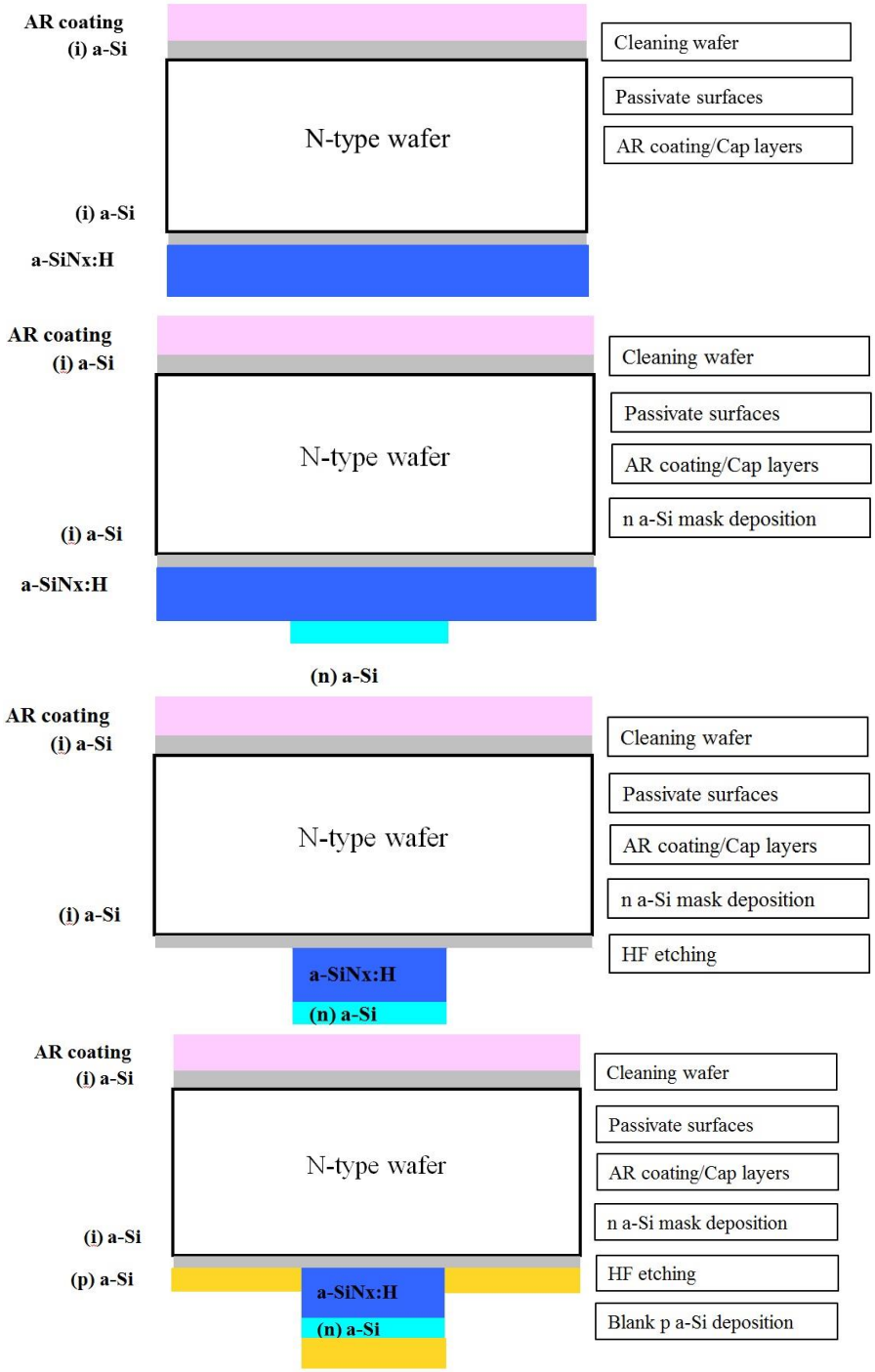


Figure 6.25 J-V plot of IBC-SHJ with one step photolithography and LFC. With optimized processing condition a 16.9% efficiency IBC-SHJ device was obtained.

To completely avoid photolithography step in IBC-SHJ fabrication, we have made shadow mask for PECVD deposition and metallization. To be specific, we made

set of two masks. One mask is for n a-Si and n strips metal deposition. The other mask is for p a-Si and p strips metal deposition. During the process, the i a-Si and SiN_X layers are initially deposited without any mask followed by depositing n a-Si through n strip mask. The n layer on the n strips will serve as protecting layer for SiN_X on n strips in the HF etching step. In the etching step unprotected SiN_X on p strips will be removed, while n a-Si/ SiN_X will be intact since n a-Si is HF resistant. After that, p a-Si emitter is deposited blankly on the rear side. This is the last step of PECVD amorphous silicon layer deposition. After that, p a-Si/ i a-Si is present on p strips. The structure on n strips will be p a-Si/ n a-Si/ SiN_X/ i a-Si. No floating collector structure is present, and metal/ n a-Si/ wafer structure is not required neither since the base contact will be formed by LFC. Lastly, n strips and p strips metal are deposited through n mask and p mask, respectively. The processing steps are shown in Figure 6.26. The device result is shown in Figure 6.27. The Efficiency reaches 15.4%, with other parameters Voc=0.656V, Jsc=36.6 mA/cm^2, FF=64.2%. This process has eliminated the photolithography process completely, therefore greatly reducing the cost of fabrication. Moreover, photolithography free process will make the whole process suitable for 50 um thin kerfless wafer. The main limit of the mask-LFC IBC devices are the gap between p strips and n strips produced by masks cannot reach under 100 um with the accuracy of our existing tools. This is still much wider than 3-steps photolithography IBC-SHJ device which usually has gap less than 30 um. Gap area usually has poor passivation quality and will lower the emitter coverage.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Cleaning wafer
Passivate surfaces
AR coating/Cap layers
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Cleaning wafer
Passivate surfaces
AR coating/Cap layers
n a-Si mask deposition
AR coating
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a-SiNx:H
(n) a-Si
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Passivate surfaces
AR coating/Cap layers
n a-Si mask deposition
HF etching
AR coating
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N-type wafer
(i) a-Si
(p) a-Si
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n a-Si mask deposition
HF etching
Blank p a-Si deposition

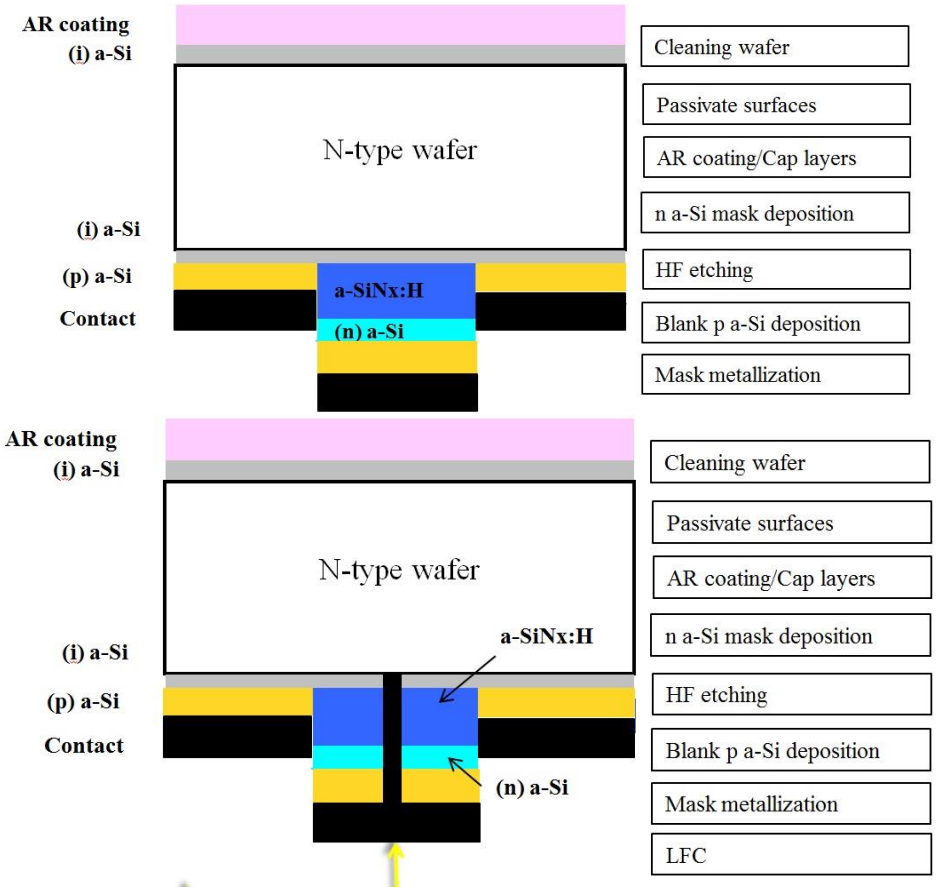

Figure 6.26. Photolithography free IBC-SHJ-LFC proecssing steps realized by set of deposition masks.

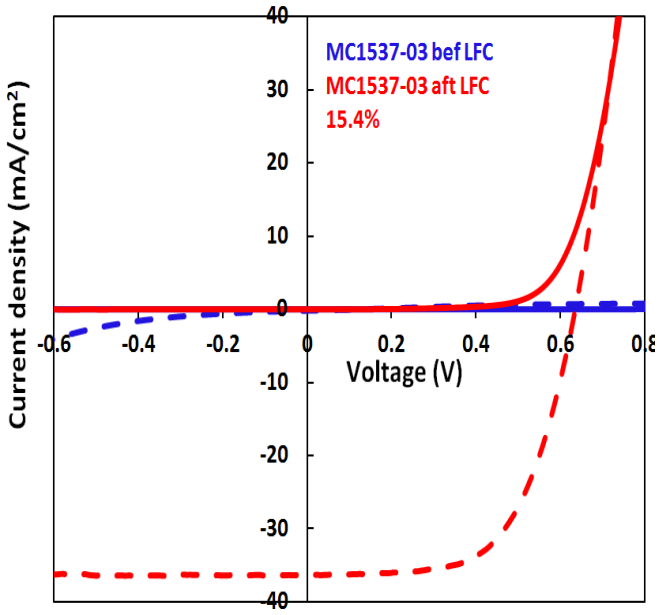

Figure 6.27 J-V plot of photolithography-free IBC-SHJ with LFC. 15-16% device efficiency has been achieved in several batches. Device performance is limited mainly due to the large gap width (100 um)

In summary, LFC has been applied on both front junction devices and IBC-SHJ devices. When there is no floating collector present on rear side or on n strips, up to 15.2% and 16.9% efficiency has been achieved for FJ and IBC-SHJ devices respectively. Two new processing methods, one-step photolithography with LFC and mask with LFC, have been developed to reduce the complexity of IBC-SHJ fabrication, and decent efficiency has been achieved. In next chapter, the laser isolation will be evaluated and incorporated to IBC-SHJ device fabrication together with LFC.

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Chapter 7

DIRECT LASER ISOLATION AND LASER ASSISTED CHEMICAL ETCHING

In chapter 4, 5 and 6, we have discussed the processing and properties of laser fired contact and its application in both front junction device and IBC device. The suitability of LFC application in n-type heterojunction devices has been proven. In this chapter, the second objective in laser process: the laser isolation will be discussed. We will first study direct laser isolation on Al/ SiNx/ n c-Si structure as start. Then we will discuss isolation on more realistic structure Al-Sb-Ti/ SiNx/ n c-Si, both with direct laser isolation and indirect laser isolation with a protective layer and wet chemical etching. The shunt resistance together with the laser induced damaged will be investigated. Finally, the lasing and etching conditions are optimized and the process has been incorporated into the fabrication of IBC-SHJ device, together with the LFC techniques.

7.1 Direct Laser Isolation

Laser isolation is also called laser grooving in traditional laser-crystalline silicon solar cell process. Laser scribing is used to achieve electric isolation between the front and rear sides of solar cells, as shown in Figure 7.1. [1] The laser grooving process is mostly realized by nanosecond pulsed laser. The laser grooving takes place outside the active device area and therefore the sole purpose is to separate the front

and rear contacts. Laser induced damage is not a major concern. On the other hand, however, for the laser isolation in this thesis, the laser needs to scribe on the rear surface between n strips and p emitter strips, as shown in Figure 7.2. Similar as LFC, this requires not only the electrical performance which is the high shunt resistance between n and p strips, but also no significant laser induced damage upon the passivation layer and silicon wafer bulk.

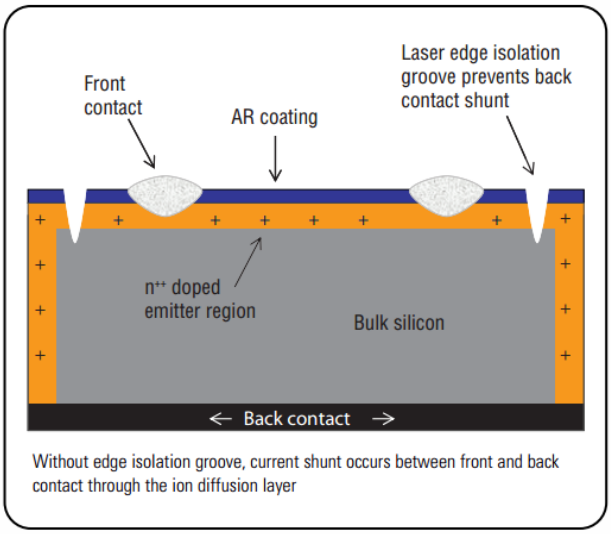


Figure 7.1 Laser grooving (laser isolation) in traditional diffusion front junction solar cells. By scribing around the edge of solar cell the front contact and rear contact is electrically separated. [1]

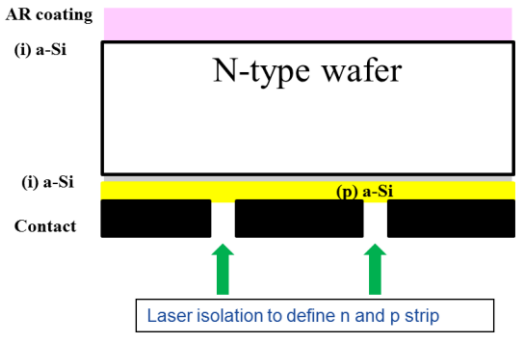


Figure 7.2 Laser isolation on IBC-SHJ device.

We initially focused on an Al/ SiN_X/ n c-Si test structure to determine laser conditions for isolation with high shunt resistance using the laser system at IEC which has pulse duration of 7ns and 1064/ 532 nm wavelength. The laser was programed to scribe a 2 mm by 2 mm square and sequence of lasing conditions were investigated. After lasing two probes are placed within and outside the square respectively to measure the shunt resistance as shown in Figure 7.3.

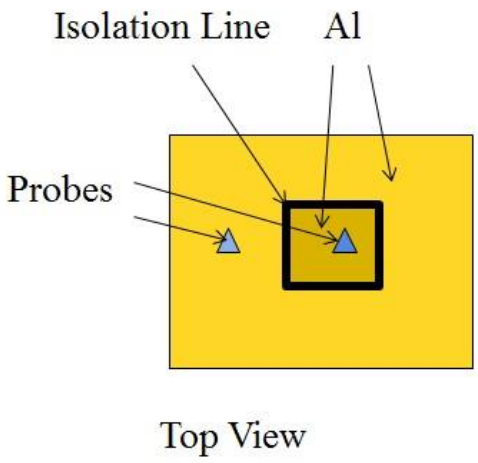


Figure 7.3 Shunt resistance measurement after laser isolation.

For a complete IBC-SHJ device, a shunt resistance > 10^3 Ω*cm^2 is required where the traditional unit of shunt resistance is Ω*cm^2. However, since the shunt source is the gap between the n and p strip, more realistic unit should be Ω*cm. For a complete IBC-SHJ device, the total length of gap between n and p strip is around 27 cm, and the cell area is 2.5 cm^2. Therefore, the 10^3 Ω*cm^2 requirement can be translated to >10^4 Ω*cm for the test structure.

Using the 7 ns laser, a full range of power, path per line and scanning velocity were evaluated and good isolation quality on Al/ SiN_X structure were not achievable and the highest shunt resistance was only 10^3 Ω*cm even with simple Al/SiN_X structure. Going with higher power or more paths per line only induce more series damage to the wafer such as deeper trench, debris in the isolation trench and extended heat affected zone (HAZ), as shown in Figure 7.4.

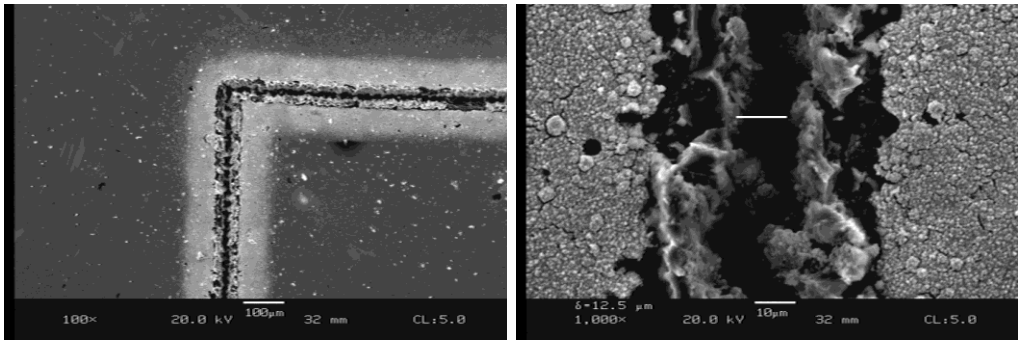


Figure 7.4 Image of trench after laser isolation. The isolation was processed by in-house 7ns pulse laser. The gap is filled with debris of silicon and a heat affected zone has extended beyond 100 um alone both sides of the isolation trench.

The 7ns laser at IEC has failed to satisfy the isolation requirement and we have turned to IPG Phonics to evaluate different laser system with much shorter pulse width at 10ps. The reason for choosing a shorter pulse width laser for isolation purpose has been discussed in Chapter 2. The laser isolation requires the accurate removal of top metal layer with minimum heat transferred into the amorphous silicon layer and

crystalline silicon wafer. Therefore, a laser with pulse comparable to the electron thermalization time is preferred for the isolation.

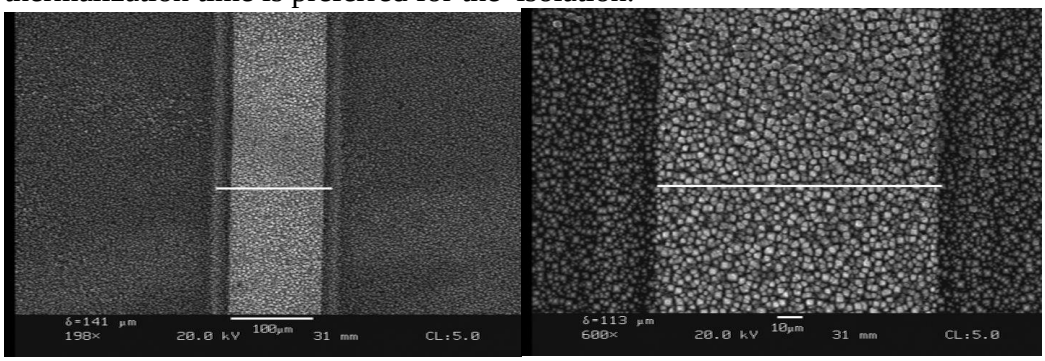


Figure 7.5 Image of trench after laser isolation. The isolation was processed by IPG phonics with 10 ps pulse laser. The silicon surface is not noticeably disturbed, and the heat affected zone is limited within 10 um around the trench.

By using the 10 ps laser, the morphology of the isolation trench has been greatly improved as shown in Figure 7.5. On the Al/ SiNx structure a shunt resistance over 10^4 Ω*cm has been reproducibly achieved. However, to combine the laser isolation technique with the LFC technique together into IBC-SHJ device fabrication, the rear side metal cannot be only Al. The practical metal structure must be the stack containing n-type dopant Antimony which is required by LFC. The isolation on Al-Sb-Ti/ SiNx structure proved to be much more difficult than Al/ SiNx structure. After IPG explored over 100 lasing conditions, it was found that by defocusing the laser beam a reasonable high shunt resistance could be achieved reproducibly. By using the lasing condition listed in Table 7.1 The measured shunt resistance > $5.6*10^3$ Ω*cm.

Table 7.1 Direct isolation lasing condition for Al-Sb-Ti/ SiNx structure.

Wavelength	**Rep Rate**	**Z**	**Power**	**Inst. Fluence**	**Scan Speed**	**PPL**
(nm)	(kHz)	(um)	(W)	(J/cm^2)	(mm/s)	(#)
515	200	+/- 500	7.0	4.3	400	12(x/y), 20(y/x)

SEM images as well as EDS elemental mapping were performed on Al-Sb-Ti/ SiNx/ n c-Si structure after 10 ps laser direct isolation. In Figure 7.6, the Aluminum and Antimony signals are absent in the laser isolation trench, leaving silicon signal alone. In the SEM image, however, the morphology in the laser isolation trench has been noticeably modified, compared with the un-lased area, which raises the concern of lifetime degradation when this technique is applied in IBC-SHJ device. The discussion of laser damage will be discussed in later part of this chapter.

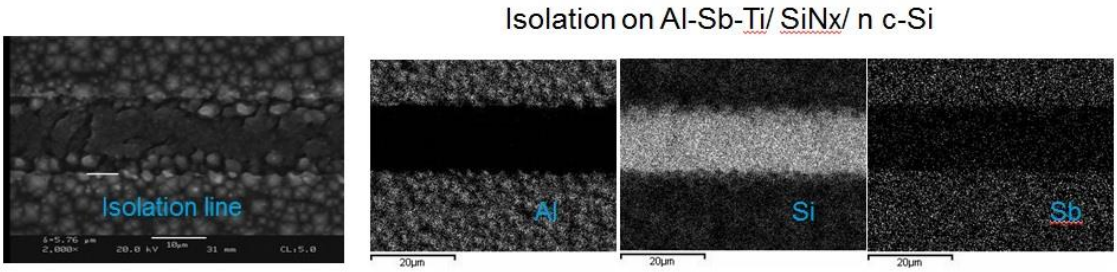


Figure 7.6 10 ps laser isolation SEM image and EDS elemental mapping.

Although a reasonable isolation is achieved on Al-Sb-Ti/ SiNx/ n c-Si structure, no isolation was observed on Al-Sb-Ti / p a-Si/ n c-Si structure even with

the 10 ps pulse width laser. This suggests that the dielectric SiN layer is critically needed to achieve isolation possibly by preventing machining/diffusion into the bulk crystalline silicon base.

This makes sense since the isolation process is the opposite of LFC, since the isolation requires maximum metal removal and minimum metal reflow/ diffusion, while LFC requires maximum dopant reflow/ diffusion. Within the same structure Al-Sb-Ti/ SiNx/ n c-Si or Al-Sb-Ti / p a-Si/ n c-Si, the removal and reflow/ diffusion process take place at the same time. It is always easier from our experience to achieve low resistance LFC in Al-Sb-Ti / p a-Si/ n c-Si than in Al-Sb-Ti/ SiNx/ n c-Si while the isolation process on Al-Sb-Ti/ SiNx/ n c-Si is usually easier than on Al-Sb-Ti / p a-Si/ n c-Si.

7.2 Indirect Laser Isolation

In last part, the more intuitive direct laser isolation has been discussed. By using 10 ps laser, a reasonable shunt resistance > $5.6*10^3$ Ω*cm could be achieved on a practical structure Al-Sb-Ti/ SiNx/ n c-Si. However, no success has been achieved on another practical structure Al-Sb-Ti/ p a-Si/ n c-Si when SiNx is not present. Moreover, to achieve a reasonable shunt resistance, surface modification is inevitable for the crystalline silicon which will probably result in degradation in lifetime.

To achieve higher shunt resistance while maintaining the passivation layer as well as the silicon wafer intact, a 2-step laser isolation method has been developedand is shown in Figure 7.7. In this method, rather than using the laser to scribe on the metal stack directly, a protective layer is firstly deposited blankly on top of the metal. This layer could be photoresist or silicon nitride, as long as it can have a slower etching rate than the metal stack in the following wet chemical etching step. After the

etching resistant layer has been deposited, the laser beam is then applied on top of the PR layer to develop the desired pattern, and in our case, the gap between n and p strips. The critical part of this process is that the laser energy should completely remove the protective layer in the gap, but not penetrate through Al-Sb-Ti metal stack layer. In this way, the following etching step will completely remove the residual metal in the isolation trench, and the passivation layer and silicon wafer will not be affected by the laser. This critical part is practical because photoresist with thickness of 2 um, as the protective layer, is comparable with the thickness of the metal stack. Therefore by carefully controlling the laser parameter the material removal can stop within the metal stack layer.

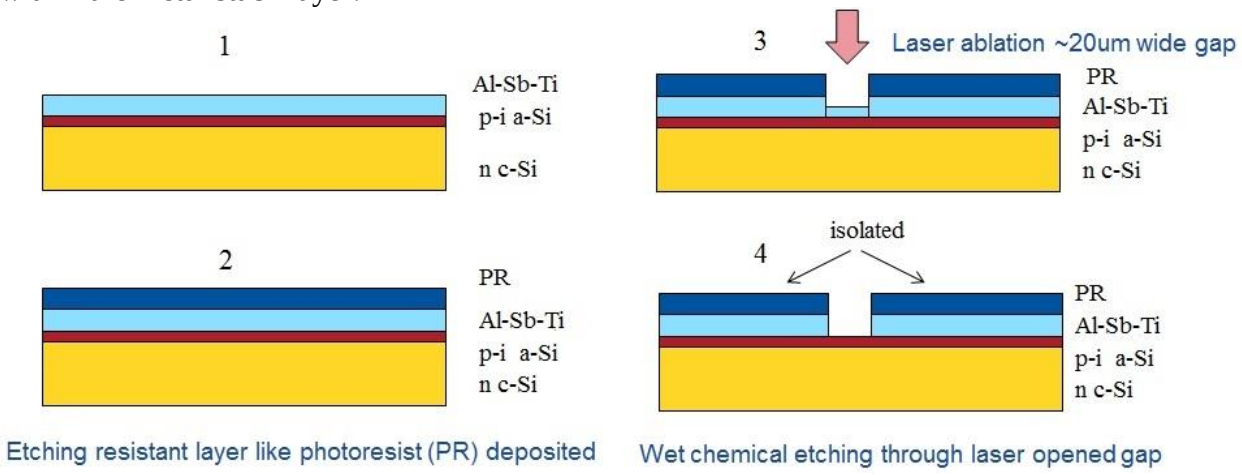


Figure 7.7 Processing steps of indirect laser isolation.

Test structure of Photoresist/ Al-Sb-Ti/ p a-Si/ n c-Si has been fabricated to investigate the concept of indirect laser isolation. The highest shunt resistance achieved by using our internal 532 nm 7 ns laser is around 10^3 Ω*cm for a small area of isolation. The result is not reproducible as can see in Figure 7.8 right image, where there are metal residuals within the gap after the isolation. This is because the

photoresist absorption of 532 nm laser is relatively poor and this will result in the non-uniformity in the photoresist removal and metal etching in the gap afterwards.

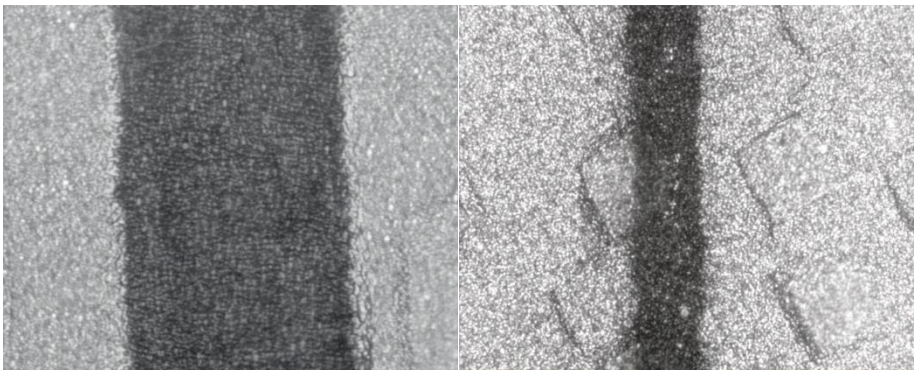


Figure 7.8 Optical microscope image of isolation trench after etching following the internal 530nm laser scribe. The left image shows no metal residual in the gap while the right image has very noticeable residual metal scattered in the isolation trench.

To address the poor absorption issue, we have applied the external laser with wider selection of parameters. Ultra-violet laser ablation of PR layer on PR-Al-Sb-Ti structure was performed at IPG. The absorption was greatly improved but the shunt resistance dropped to 100 Ω*cm. After examining the images of the trench it was found that at the corner of the isolation scribe, the energy laser impact is much higher than the rest scribing area, as shown in the left image of Figure 7.9.

The reason of the non-uniformity is that near the corner when the laser accelerate and decelerate, there will be more number of pulses at the corner as shown in Figure 7.10. With the constant velocity scanning shown in Figure 7.11, the laser energy will be evenly distributed at the corner of the scribing.

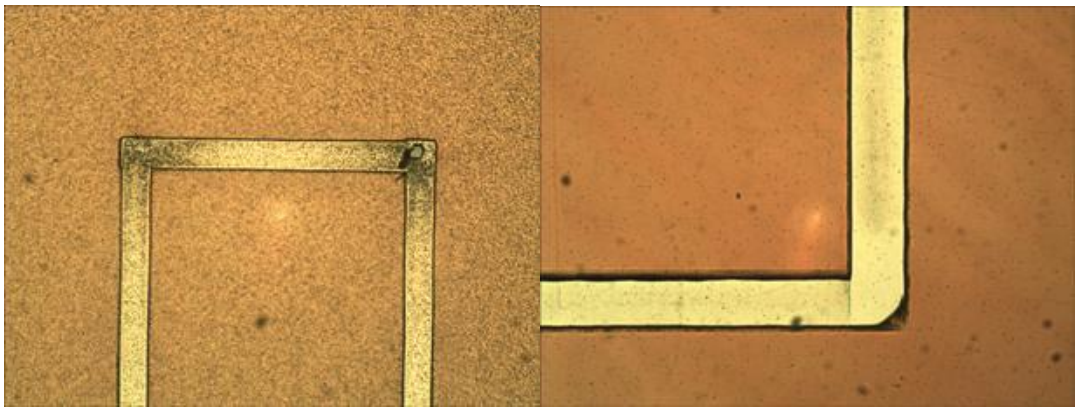


Figure 7.9 Images of UV-laser scribing without constant velocity (left) and with constant velocity (right). Note that the scribe with constant velocity has uniform morphology even at the corner.

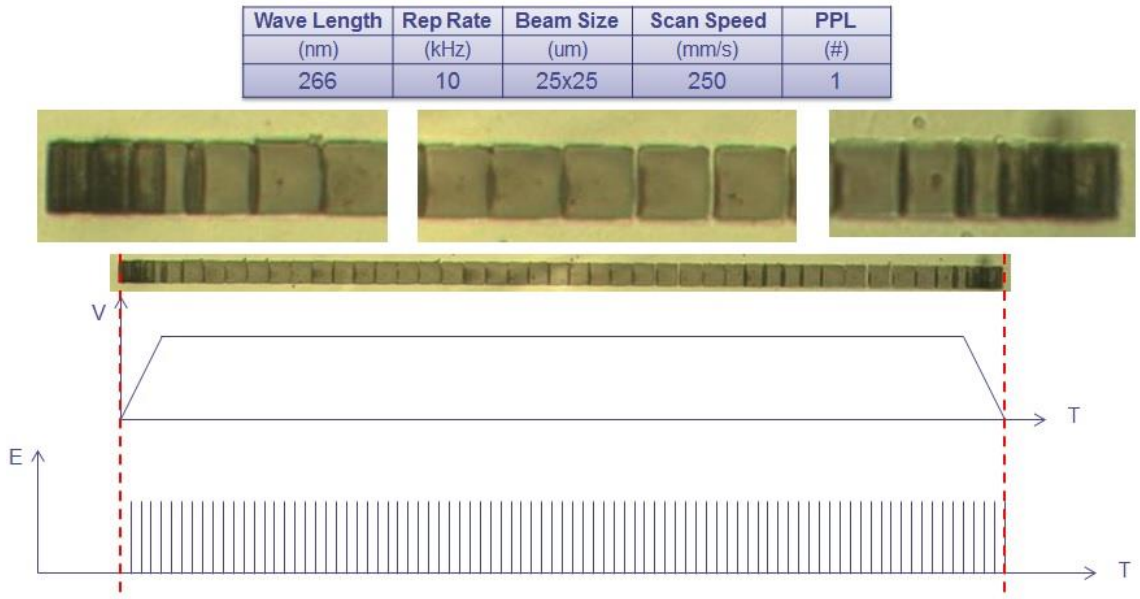


Figure 7.10 Laser scanning without constant velocity control. When the laser starts or stops to move more energy dose will be applied on the surface.

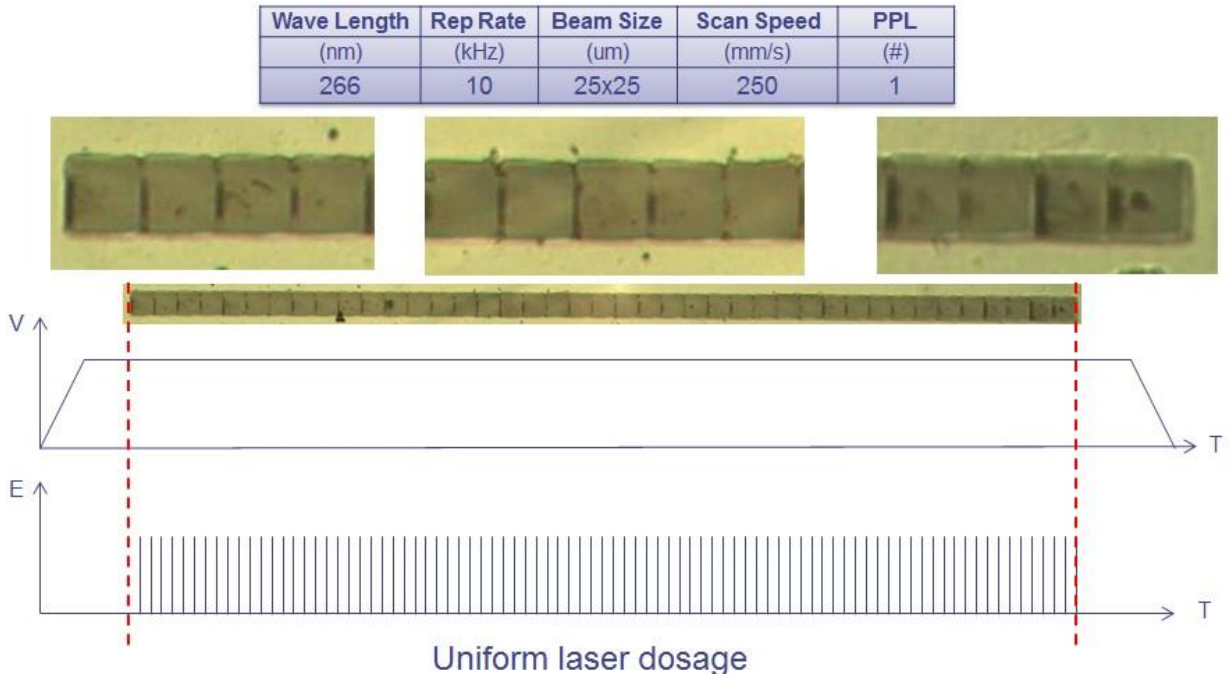


Figure 7.11 Laser scanning with constant velocity control. The energy dose is evenly distributed when the laser starts/ stops to move.

The uniformity of photoresist removal can also be confirmed by the EDS mapping of the isolation trench before chemical etching. As shown in Figure 7.12, Carbon signal is completely removed in the trench which means the organic photoresist is ablated by the laser. The Aluminum signal on the other hand is intact suggesting the laser energy is not penetrating through the metal stack.

A final step of optimization is the wet chemical etching step. The etching solution for Al-Sb-Ti removal in this experiment is HNO_3 : HCl : H_2O = 1:1:1 in volume. The solution will removal the stack layer at room temperature. The etching time is important for the isolation. If the etching time is too short the residual metal will remain in the trench causing the shunt. If the etching time is excessive, the solution will laterally etch the metal underneath the photoresist at the un-lased area. The lateral etching will cause the unwanted lift off of the photoresist and removal of

larger area of metal stack, reducing the emitter coverage and n strip coverage. The image of lateral etching is shown in Figure 7.13. The relationship between the etching time and the trench gap width as well as the shunt resistance and plotted in Figure 7.14. Based on the results, an average etching time of 4 minutes was chosen for optimized shunt resistance and gap width for device application.

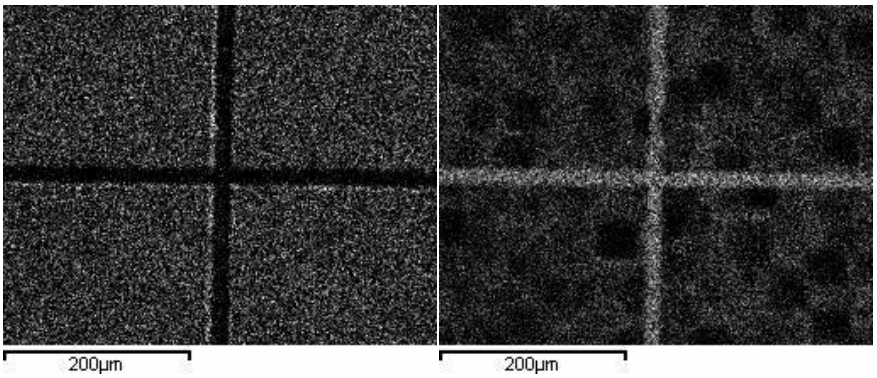


Figure 7.12 EDS mapping of laser isolation trench before wet chemical etching. The left image is Carbon signal and the right image is Aluminum signal.

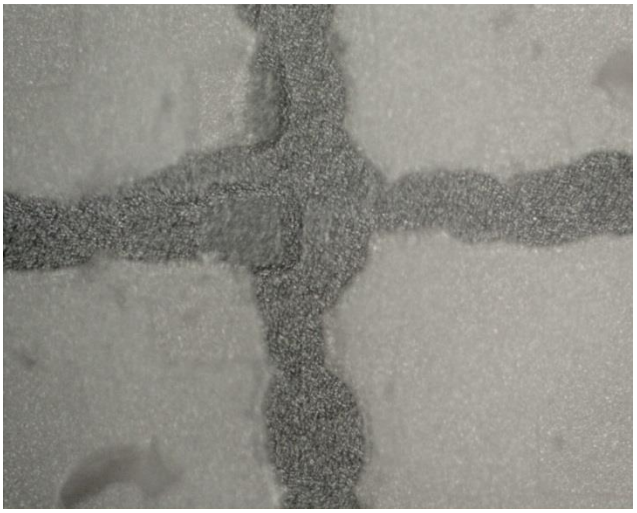


Figure 7.13 Lateral etching of metal stack outside lased trench due to excessive etching time.

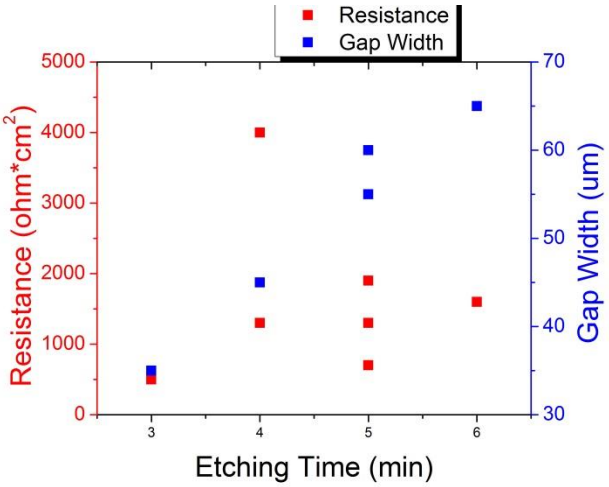


Figure 7.14 Gap width increases with longer etching time and more etching cycle; Longer etching time does not necessarily yield higher shunt resistance;

Shunt resistance > $1.6*10^5$ Ω cm has been achieved repeatedly with optimized processing incorporating the UV laser, the constant velocity laser scanning and 4 minutes etching time at full size IBC-SHJ pattern Figure 7.15.

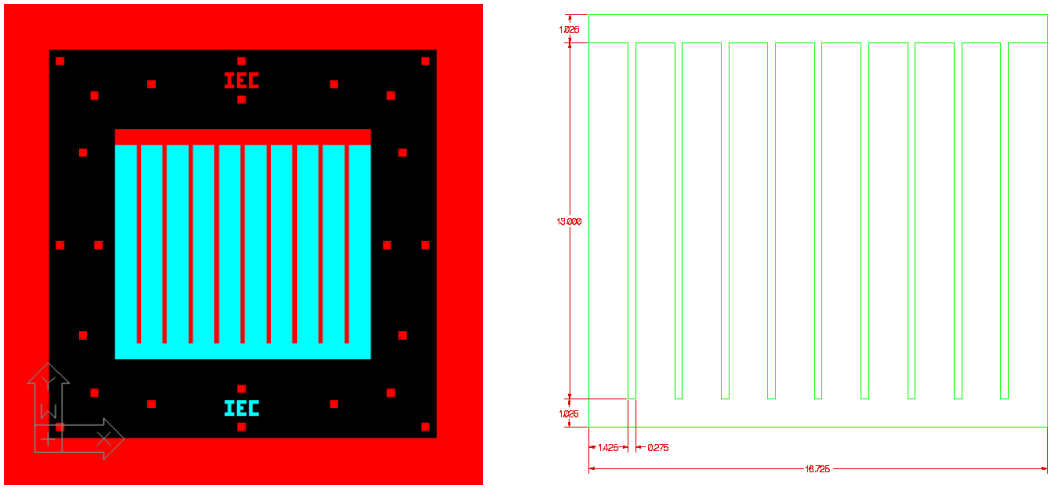


Figure 7.15 The laser scribe plus post chemical etching defines the 16.70 mm X 15.00 mm cell area, as well as the isolation gap between 1400um wide p strips/ bus-bars and 250um wide n strips/ bus-bars.

7.3 Laser Induce Damage During Laser Isolation

A high shunt resistance has been achieved by the laser plus chemical isolation as discussed in the last part of this chapter. Before it can be successfully applied in the device application, it still needs to prove that it will not pose significant lifetime drop after the process. Theoretically the indirect laser isolation should not impact the lifetime during the process since the laser energy will not penetrate the metal stack layer reaching the passivation layer.

To validate the hypothesis, a test structure of has been made with intrinsic amorphous silicon plus SiN_X layer on both sides of wafer to achieve high initial lifetime. The lifetime was measured before metallization. After metallization, the test structures went through either direct laser isolation or laser-chemical 2-step isolation. The lifetime change of both experiments is shown in Table 7.2 and 7.3 respectively. Note the for the direct isolation samples, the original passivation layer was removed and new passivation layers were deposited after direct laser process and post laser lifetime measurement. The post re-passivation lifetime cannot fully recover. This is suggesting that the direct laser isolation is damaging beyond the surface passivation and extending into the bulk silicon wafer irreversibly.

The samples that went through indirect laser isolation maintained reasonably high lifetime according to table 7.3. The control sample also proved the etching process will not degrade the lifetime. Additional Photoluminescence mapping was conducted by collaborator Photovoltaic Research Laboratory at MIT. No significant recombination centers were observed due to laser and etching process according to Figure 7.16 while significant lifetime drop around the direct isolation lines were observed in Figure 7.17. Together with the lifetime measurement the indirect laser-

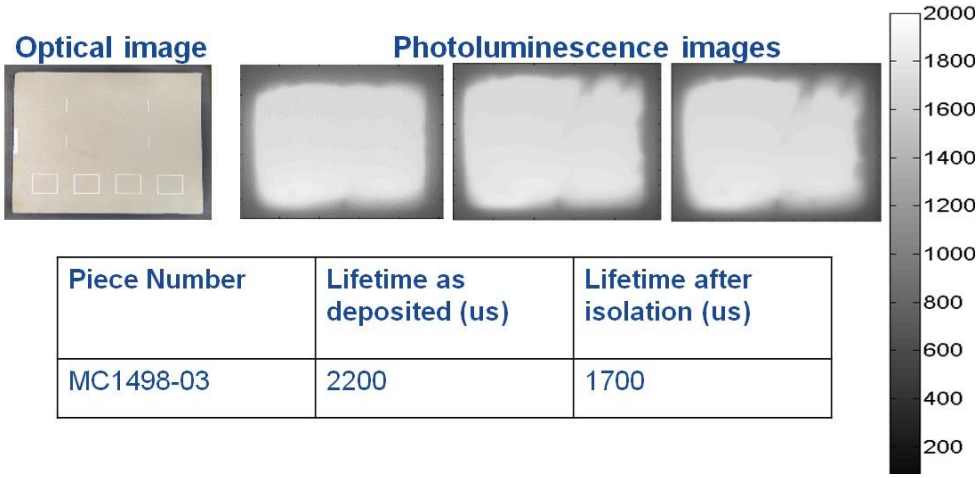
chemical isolation has been proven to be suitable for device application at the passivation point of view.

Table 7.2 Lifetime change of sample before and after direct laser isolation. The lifetime dropped significantly after laser processing and recovered partially after re-passivation.

Label	**Initial lifetime (us)**	**Treatment**	**Post laser lifetime (us)**	**Post re-passivation (us)**
MC1498-02	3000	Direct laser isolation	800	1000

Table 7.3 Lifetime change of sample before and after indirect laser isolation. Lifetime moderately recovered after repassivation.

Label	**Lifetime as deposited (us)**	**Lifetime after 2 steps isolation**
MC1490-02	2900	1600
MC1498-03	2200	1700
MC1498-04 control	2200	2200 (no metal, etching only)



Piece Number	Lifetime as deposited (us)	Lifetime after isolation (us)
MC1498-03	2200	1700

Figure 7.16 Photoluminescence lifetime mapping (taken at MIT) of indirect laser isolation processed test structures. The three PL images are for intact sample, sample after lasing and sample after etching. No significant recombination centers were observed due to laser and etching process.

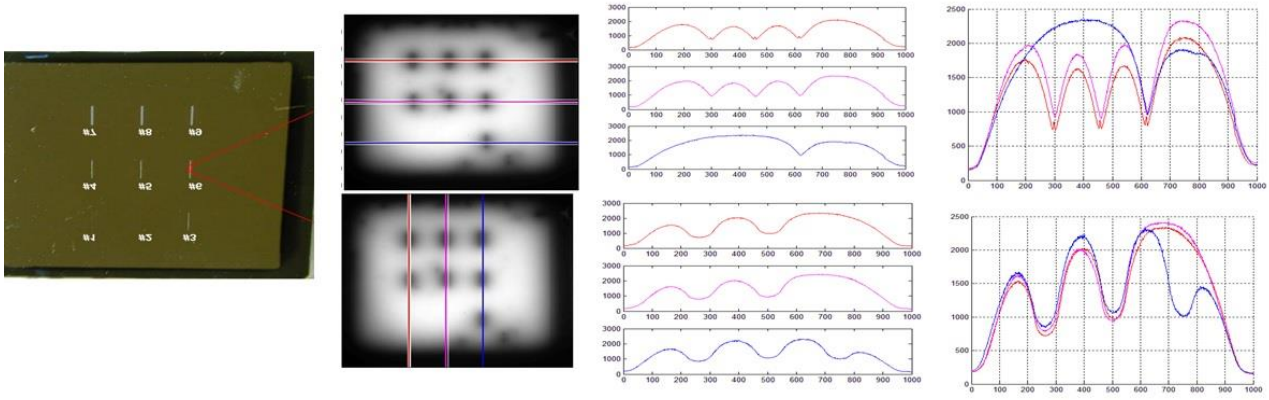


Figure 7.17 Photoluminescence lifetime mapping and line scan of direct laser isolation processed test structures (taken at MIT). Significant recombination centers have been observed around the laser processed area.

Finally, IBC-SHJ devices were fabricated with indirect laser isolation and LFC. The rear side of the device is blank p a-Si. The rear side p-n interdigitated patterns were developed by the indirect isolation and the base contacts on n strips were developed by LFC. The device structure and result are shown in Figure 7.18. The total efficiency of the device reaches 8.8%, with Voc of 570 mV, Jsc of 28mA/cm^2 and FF of 55%. The device performance is very close with the all p a-Si IBC-SHJ fabricated with shadow mask deposition. This is successful demonstration with one extra step of protective photoresist layer deposition and a chemical etching step, the laser isolation technique could reach high shunt resistance while maintaining good surface passivation.

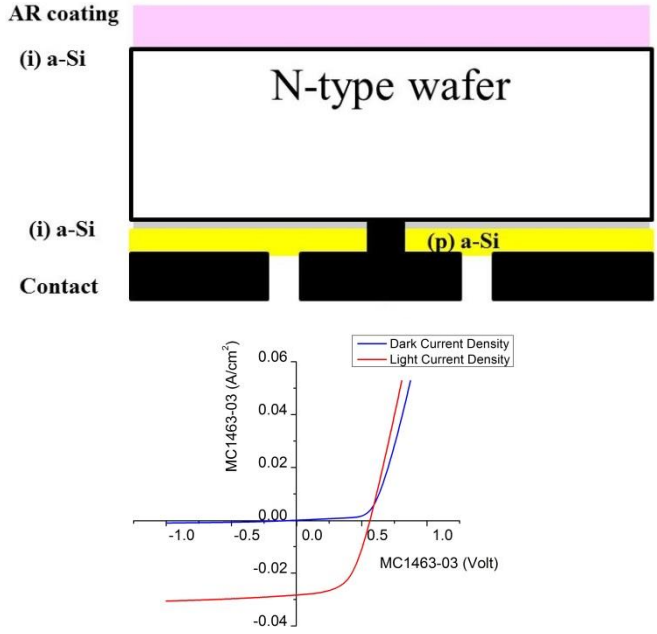


Figure 7.18 IBC-SHJ device fabricated with indirect laser isolation and LFC.

REFERENCES

[1] Spectra-Physics. Laser Edge Isolation Scribing for Crystalline Silicon Solar Cell Production (http://www.spectra-physics.com/documents/Laser_Edge_Isolation_Scribing_SP.pdf)

Chapter 8

SUMMARY

8.1 Summary

Interdigitated Back Contact Silicon Hetero-Junction (IBC-SHJ) solar cell architecture combines the advantages of highest efficient device structure Interdigitated Back Contact solar cell and second highest efficient device structure Silicon Hetero-Junction solar cells. However, its fabrication requires multiple photolithography steps. In this work, two laser-based processing techniques, laser fired contact (LFC) and laser isolation have been developed with intention to simplify the processing steps of IBC-SHJ device fabrication.

Laser fired contacts to n-type crystalline silicon were successfully developed by adding novel metal stacks containing Antimony (Sb). Sb serves as n-type dopant of silicon during the laser process and is determined to be the critical component of the metal stack for n-type crystalline silicon LFC. Lasing conditions and the structure of metals stacks were optimized for lowest contact resistance and minimum surface damage, which are two critical requirements for application in photovoltaic device.

Contact resistance for firing different metal stacks through either SiN_X or p-type amorphous silicon were determined using two unique models and test structures. The vertical test structure was used to optimize the lasing condition efficiently. The TLM lateral test structure was used to accurately determine the specific contact resistance. Specific contact resistance values of 2-7 $m\Omega\ cm^2$ have been achieved

reproducibly. A relationship between the surface morphology, the EDS mapping of the surface elemental distribution and the specific contact resistance of LFC has been found. Although the EDS does not have the sensitivity to detect the local Antimony doping level, the relationship serves well as a processing control. By using low power pulse laser and varying the number of pulses per LFC spot the morphology as well as the contact resistance of LFC can be well controlled and optimized. A temperature dependent TLM measurement was performed and the ρ_c was found to have a very weak dependence on temperature. This indicates a Thermionic-Field Emission type of ohmic contact where the narrowing of the potential barrier at the metal silicon interface can be attributed to successful n^+ doping in the LFC area.

A good LFC should not only have low contact resistance, but also pose minimum laser induced damage to the surface passivation and silicon wafer. Optimized LFC spot has been examined by SEM from both top view and cross section view and no physical damage to the wafer beyond 500 nm has been found. The LFC pit has been further investigated by TEM externally at Photovoltaic Research Lab, the silicon lattice was found to be intact under the LFC pit. Therefore it is concluded that with carefully chosen lasing condition, no bulk damage will be induced by LFC process. To evaluate the potential laser damaged on surface passivation, a test structure was designed and fabricated to evaluate the surface passivation loss. Recombination loss due to laser damage was consistent with an extracted local surface recombination velocity (SRV) of ~20,000 cm/s that is similar to values for laser fired base contact for p-type crystalline silicon. A typical loss of 30-50 mV V_{OC} is found compared with the implied V_{OC} converted from the lifetime of device precursor.

Front junction solar cells were fabricated to test the suitability of LFC in photovoltaic device. A 15.2% efficiency device was achieved using a SiN_X blocking layer which is standard for LFC device for p-type crystalline silicon base device. Poor device performance was found when the p a-Si was inserted as rear side blocking layer since unwanted minority carrier collection by the rear side p a-Si occurred where there was no LFC. By inserting an additional dielectric blocking layer SiN_X which prevents the p a-Si and metal from contacting the device performance was improved. With additional SiN_X dielectric inserted on n strip, proof-of-concept efficiencies of 16.9% were achieved and steps of photolithography and/ or etching steps have been reduced and replaced by LFC during process.

For laser isolation, both direct laser scribing isolation and laser-chemical isolation have been evaluated. The more intuitive direct scribing isolation could achieve shunt resistance over 10^3 Ω*cm on Al/ p a-Si and Al-Sb-Ti/ SiN_X structure, but failed to obtain sufficient isolation on Al-Sb-Ti/ p a-Si structure. The direct isolation also imposes surface passivation damage and irreversible bulk damage. As an alternative method, laser-chemical isolation was developed and achieved high shunt resistance on all structures with possible application in IBC device. By optimizing the lasing condition and etching process, shunt resistance over 10^5 Ω cm can be repeatedly achieved. The passivation loss due to isolation process is found to be insignificant which is confirmed by lifetime measurement internally and Photoluminescence lifetime mapping externally at photovoltaic research lab at MIT. Finally, p a-Si back IBC-SHJ solar cell was fabricated with photolithography-free process. The rear side p and n strips were developed by laser chemical isolation. The base contact was developed by LFC. The device achieved efficiency of 8.8%.

8.2 Future Prospects

LFC is a creative way to develop the local contact without using photolithography and/ or etching steps. However, the contact formation is at the cost of loss of local surface passivation. Therefore it is always crucial to reduce the passivation loss while maintaining good specific contact resistance of LFC. Wider selection of laser pulse width and the application of dual-laser process might be a new way to develop better LFC.

From characterization point of view, micro-SIMS and lock-in thermography with micron per pixel resolution could be great tool to investigate and help to understand the local doping and contact properties of LFC.

The original proposed photolithography –free device architecture has its own limit, mainly because the unwanted collection from p a-Si on the n strip outside the LFC area. With additional SiN_X layer blocking the collection, 16.9% efficiency IBC-SHJ device has been achieved, which is a demonstration of suitability of LFC technique. However, to deposit SiN_X layer the photolithography steps are inevitable. To avoid the photolithography, Mask PECVD and metallization depositions have been applied in the fabrication together with LFC and 15.4% efficiency device has been obtained. To further increase the efficiency and further simplify the processing steps, mask deposition accuracy, better control of wet chemical etching and other patterning techniques need to be carefully chosen and combined.

The indirect laser isolation is a great tool to electrically separate metal contacts. Its concept of using a protective layer with slower etching rate, however, can be extended to develop the complete n or p strips rather than the gap between the

strips. Combined with LFC technique, the extended indirect laser patterning can be the solution to photolithography-free fabrication of IBC-SHJ with high efficiency architecture.

Appendix A

OPERATION OF U.S. LASER CORPORATION MODEL 5024 ND:YAG LASER MICRO-MACHINING SYSTEM

The laser system being used in this dissertation is a class I diode pumped Q-switched Nd:YAG laser operating at 1064nm and 532nm. There are four major components of the laser system: the optical circuit chamber, the steel cabinet, the viewing monitor and the controlling computer as shown in Figure A.1. The system is capable of large field, high precision X-Y positioning and CCTV viewing. In silicon group at Institute of Energy conversion, University of Delaware, the system is currently used for laser fired contact (LFC) on n-type crystalline silicon wafer.

Check if safety light is working properly and availability of laser safety glass before turning on the system. Turn on the main power switch (white 2-post flip switch). Then turn on laser diode power supply (orange rocker switch). Both switches are located on component 4 the controlling computer case. After turning on laser diode power supply, wait until LED screen shows ‘Spectra Physics Lasers’ and then turn on Laser enable key switch interlock (Figure A.2) and the computer. It is important to make sure that the manual safety shutter and Q-Gate switches are set to ‘closed’ and ‘off’ respectively before turning on the computer, as shown in Figure A.2.

Figure A.1 Laser system used in this study. 1: optical circuit chamber; 2: steel cabinet; 3: viewing monitor and 4: controlling computer.

Figure A.2 Laser Enable key Switch.

After the computer is done starting up, double click on "PrmCfg.exe" icon (Figure A.4) on computer desktop. The Character Scribing, Spectra-Physics, and A3200 Controller item boxes should be checked (Figure A.5). Click the 'LOAD'

button to load their configuration utilities then close PrmCfg.exe. Then open Friendly Motion Software “FM50.exe” (Figure A.4) on desktop. The FM50.exe is the main controlling program for the laser system. Select the M108 checkbox to start the laser diode. (Figure A.6) After 2-3 seconds you should hear ‘click’ and the LCD panel alone the laser enable key switch should show the current to be 5.31 or 5.32 A. If the current is not showing correctly, check the interlocks on optical circuit chamber. Once the current is showing correctly, let the laser diode warmup for 20-30 minutes. If the system has been in use prior within same day, and the diodes have been shut off since, the warm up time can be reduced to 5-10 minutes. If the diodes have not been properly warmed up the pulse-to-pulse energy variation of the LASER output will vary significantly. This can result in non-uniform laser energy dosage per shot and problematic LFC.

Figure A.3. Safety shutter switch and Q-Gate switch

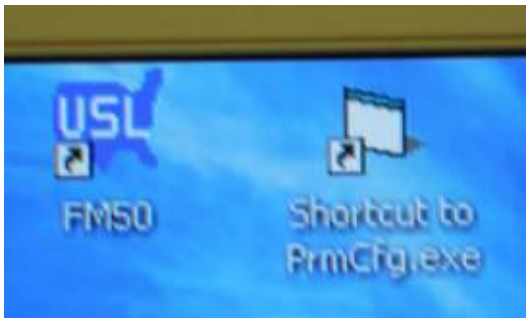


Figure A.4. PrmCfg program and FM50 motion controlling program.

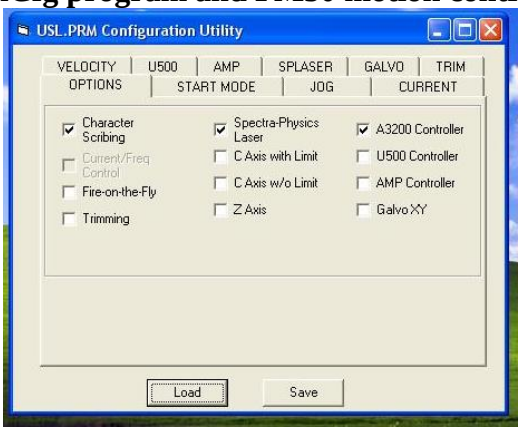


Figure A.5. USL.PRM Configuration Utility.

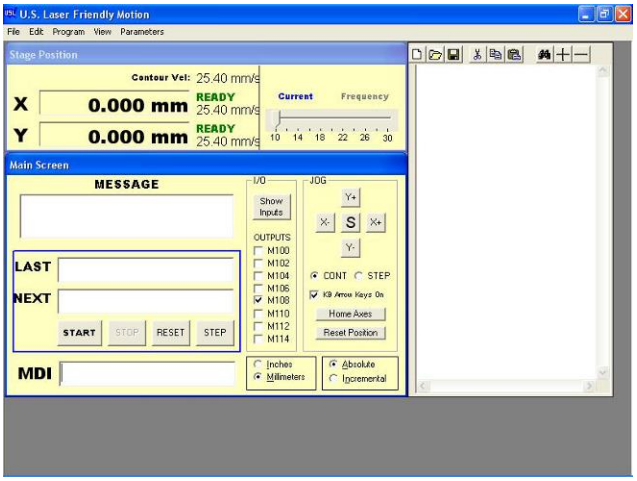


Figure A.6. User interface of FM50 motion controlling program.

After turning on the laser system, load the sample which needs LFC in steel cabinet. The sample must be 1 by 1 inch in size. If the sample is slightly larger and cannot fit the sample holder, carefully snap one or two edges. If the sample cannot fit properly in sample holder it will cause problem in focus in future steps. The focus step is done by twisting the laser exist shown in Figure A.7. Twisting the exit clockwise or counterclockwise makes the laser exit closer or farther from the sample holder. It is also very important to align the gap between n and p strip with the y-axis. A properly focused and aligned sample is shown in Figure A.8. Textured sample has better contrast in the monitor while polished sample has worst contrast which requires patience during focus and alignment.

Once the sample is properly mounted, choose the desired LFC program under MC System LFC Folder in Friendly Motion software. A sample program with explanation is listed at the end of the appendix. Within the program, you can vary number of shots per LFC spot, spacing between each LFC spot, the frequency, the diode current. For LFC on IBC-SHJ device, the default program designed for 13 mm length n-strip will fire 26 spots on each strip with 0.5 mm spacing. You may change the spot number and/ or spacing according to your purpose.

The typical lasing power for LFC is between 150 mW to 400 mW. However, it is always a good idea to use metal pads outside the cell area (the IEC logo for example) to test LFC condition before firing on the n-strip since the lasing condition can vary greatly from batch to batch due to different surface condition. Fire 3-5 LFC spots for each condition being tested. For each condition being tested, record the laser power by using the power meter in Figure A. 9.

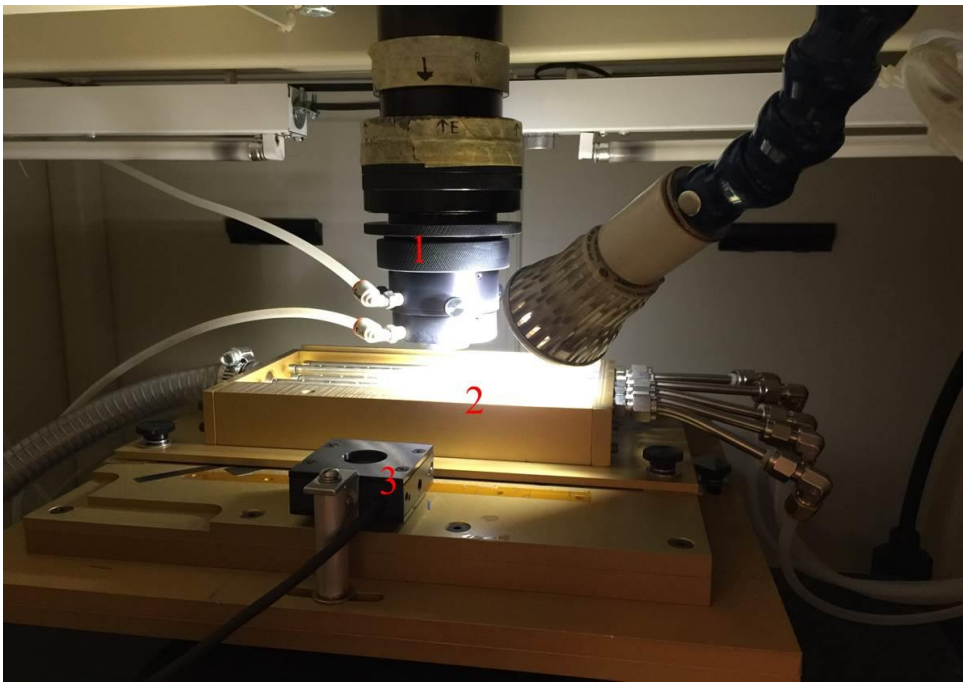


Figure A.7. Inside Steel cabinet. 1: Laser pulse exit; 2: sample stage and 3: power meter.

After running the program, the LFC spots should be visible on the viewing monitor as shown in Figure A. 10. However, it is not possible to determine whether a LFC is properly fired merely from the viewing monitor. It is safest by using the SEM and EDS to determine the category of LFC spot as shown in Figure A.11. Higher energy dosage per LFC spot usually results in over-fired LFC while lower energy dosage per LFC spot usually results in under-fired LFC. To vary the energy dosage one can either change the energy per laser pulse shot by changing the current setting or change the number of laser pulse shots per LFC spot. Both variables can be changed in the program.

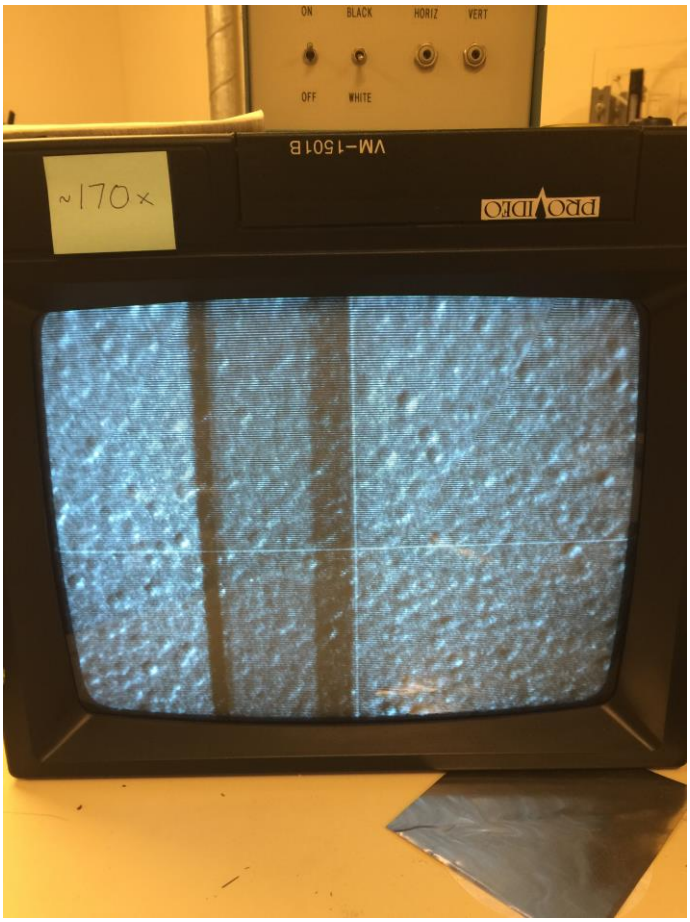


Figure A.8. Properly focused and aligned sample.

Figure A.9 Power meter.

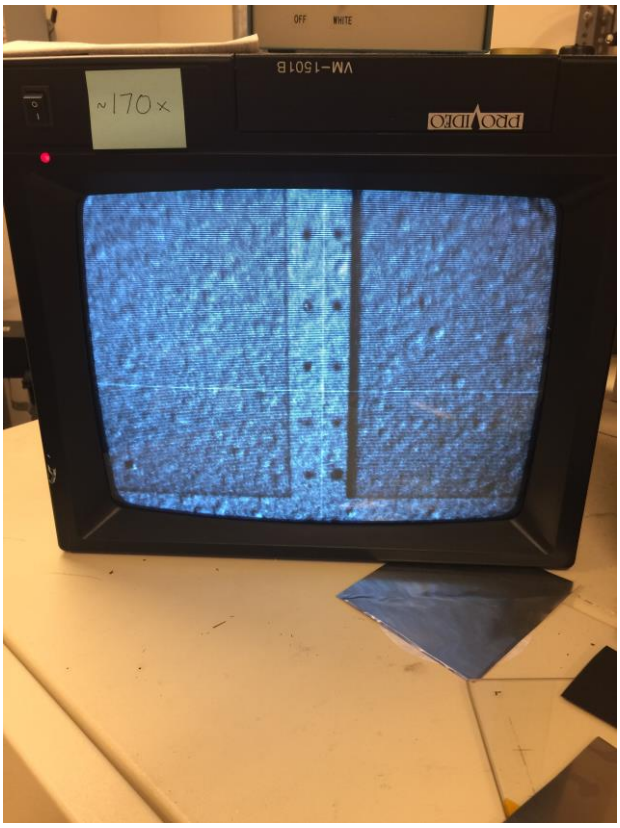


Figure A.10. LFC spots on viewing monitor after running program.

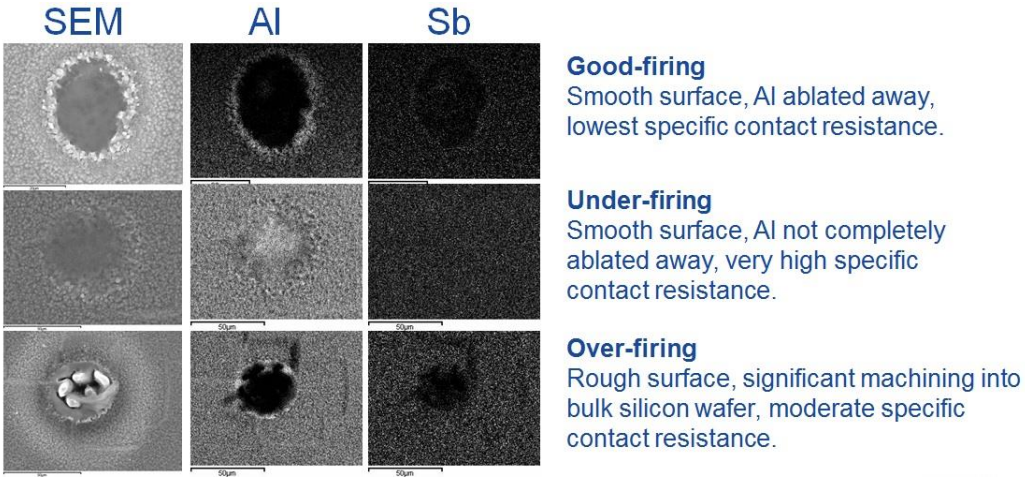


Figure A.11. Different categories of LFC.

Once the proper-fired LFC is obtained, measure and record the power. Apply the same lasing condition on the n strips of real device. It is important to start from larger LFC pitch rather than firing too many LFC spots at the beginning. This is because during the LFC process, the device series resistance will be decreased at the cost of reducing the V_{OC} at the same time. To achieve highest possible device performance the series resistance and V_{OC} must be well balanced. It is always feasible to add more LFC spots on the sample if the device is limited by resistance, but it is not possible to undo LFC if the device is found to be limited by $V_{OC.}$ Apply LFC on all n strips and measure the device performance. The starting pitch of LFC can be 0.5 mm to 1 mm. after measurement if the device is still showing S-shape or has over 4 ohms cm^2 series resistance, consider adding more LFC spots on the non-lased area on n strip and measure the device performance again. After iteration of LFC if the measured device efficiency only increased slightly or starts to decrease, stop further LFC on device and record the final efficiency.

After finishing using the laser system, turn off the system in the order of computer, laser power supply and main power supply which is the reverse order of turning on the system.

Sample LFC Program

g71 ! MM Coordinates

g91 ! Relative Positioning

m99 ! Machine Home

f10 !Set Scanning Velocity mm/sec

sf10 ! Set frequency (kHz.)

sc20 ! Set current

m102 ! Open Safety Shutter

m3 ! Select starting point

KN200R26 ! Run Subroutine KN201 Repeat 26 times

m103 ! Close Safety Shutter

m0 ! STOP PROGRAM

N200 ! Subroutine N200

m100 ! Open Q-Switch

m101 ! Close Q-Switch

y0.5 ! Move Stage Alone y axis 0.5 mm

m6 ! STOP Subroutine

Appendix B

REPRINT PERMISSION LETTERS

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