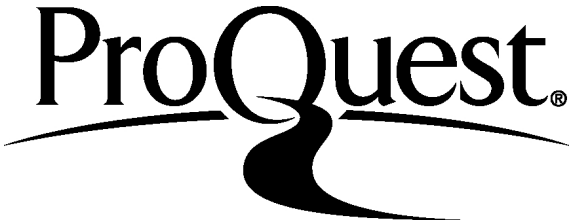
APPROACHES TO IMPROVE THE V_{OC} OF CDTE DEVICES: DEVICE MODELING AND THINNER DEVICES, ALTERNATIVE BACK CONTACTS

by

Curtis J. Walkons

A dissertation submitted to the Faculty of the University of Delaware in partial fulfillment of the requirements for the degree of Doctor of Philosophy in Physics

Spring 2016



APPROACHES TO IMPROVE THE V_{OC} OF CDTE DEVICES: DEVICE MODELING AND THINNER DEVICES, ALTERNATIVE BACK CONTACTS

by

Curtis J. Walkons

Approved: _____
Edmund R. Nowak, Ph.D.
Chair of the Department of Physics and Astronomy

Approved: _____
George H. Watson, Ph.D.
Dean of the College of Arts and Sciences

Approved: _____
Ann L. Ardis, Ph.D.
Senior Vice Provost for Graduate and Professional Education

I certify that I have read this dissertation and that in my opinion it meets the academic and professional standard required by the University as a dissertation for the degree of Doctor of Philosophy.

Signed: _____

Robert W. Birkmire, Ph.D.
Professor in charge of dissertation

I certify that I have read this dissertation and that in my opinion it meets the academic and professional standard required by the University as a dissertation for the degree of Doctor of Philosophy.

Signed: _____

Brian E. McCandless, B.S.
Member of dissertation committee

I certify that I have read this dissertation and that in my opinion it meets the academic and professional standard required by the University as a dissertation for the degree of Doctor of Philosophy.

Signed: _____

Robert L. Opila, Ph.D.
Member of dissertation committee

I certify that I have read this dissertation and that in my opinion it meets the academic and professional standard required by the University as a dissertation for the degree of Doctor of Philosophy.

Signed: _____

John Q. Xiao, Ph.D.
Member of dissertation committee

I certify that I have read this dissertation and that in my opinion it meets the academic and professional standard required by the University as a dissertation for the degree of Doctor of Philosophy.

Signed: _____

Paul A. Evenson, Ph.D.
Member of dissertation committee

ACKNOWLEDGMENTS

I would like to acknowledge everyone at the Institute of Energy Conversion (IEC) who have generously assisted me in completing my dissertation research. These include my advisor Robert Birkmire for his professional support and guidance in directing me throughout my PhD program, including my NSF IGERT fellowship program, my co-advisor and committee member Brian McCandless for all of his help, patience, and guidance that I have had in learning about CdTe science and technology, and his assistance in my experiments, Steve Hegedus for his supervision with my IGERT fellowship, for helping me understand CdTe theoretical concepts as well his training and advice that he has given me on device characterization techniques, Chris Thompson for all of his help and patience that he has had with me learning how to do electrical measurements as well as assisting me in many questions that I have had over the physics of CdTe solar cells, Shannon Fields for letting me use the IEC workshop as well as his guidance that I have had in learning to use the equipment for my experiments, Wayne Buchanan, John Elliott, and Kevin Hart for sample fabrication, Kevin Dobson for informal discussions that we have had about my research, as well as helping me build my resumes, Sherry Stuart and Paula Newton for their assistance in ordering products that I have needed to complete my research, and Siming Liu and Stella Liu for their experimental work on thin CdTe devices.

I would also like to acknowledge Robert Opila, John Xiao, and Paul Evenson for their service on my PhD committee, Rakesh Agrawal from the School of Chemical Engineering at Purdue University for my IGERT fellowship support and everyone at

the University of Delaware's Department of Physics and Astronomy, who has helped guide me and support me throughout my PhD career.

I am eternally grateful for my family, including my mother and stepfather for all of their love and support throughout my life. They have been there to motivate me to go to college and have recognized my creativity and intellect which I have needed to complete this thesis.

Finally, I am also eternally grateful for my father, Carl Walkons (March 30th 1924-April 15th 1996), who recognized my curiosity that I had towards science at a young age and hence nurtured and guided me in that direction. This PhD dissertation is dedicated to him.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

ABSTRACT

An existing commercial process to develop thin film CdTe superstrate cells with a lifetime τ=1-3 ns results in V_{oc}= 810-850 mV which is 350 mV lower than expected for CdTe with a bandgap E_G = 1.5 eV. V_{oc} is limited by 1.) SRH recombination in the space charge region; and 2.) the Cu_2Te back contact to CdTe, which, assuming a 0.3 eV CdTe/Cu_2Te barrier, exhibits a work function of Φ_{Cu2Te}= 5.5 eV compared to the CdTe valence band of $E_{v,CdTe}$=5.8 eV. Proposed solutions to develop CdTe devices with increased V_{oc} are: 1.) reduce SRH recombination by thinning the CdTe layer to $\leq$ 1 μm; and 2.) develop an ohmic contact back contact using a material with $\Phi_{BC}\geq$5.8 eV. This is consistent with simulations using 1DSCAPS modeling of CdTe/CdS superstrate cells under AM 1.5 conditions.

Two types of CdTe devices are presented. The first type of CdTe device utilizes a window/CdTe stack device with an initial 3-9 μm CdTe layer which is then chemically thinned resulting in regions of the CdTe film with thickness less than 1 μm. The CdTe surface was contacted with a liquid junction quinhydrone-Pt (QH-Pt) probe which enables rapid repeatable V_{oc} measurements on CdTe before and after thinning. In four separate experiments, the window/CdTe stack devices with thinned CdTe exhibited a V_{oc} increase of 30-170 mV, which if implemented using a solid state contact could cut the V_{oc} deficit in half. The second type of CdTe device utilizes C61 PCBM as a back contact to the CdTe, selected since PCBM has a valence band maximum energy (VBM) of 5.8 eV. The PCBM films were grown by two different

chemistries and the characterization of the film properties and device results are discussed. The device results show that PCBM exhibits a blocking contact with a 0.6 eV Schottky barrier and possible work function of Φ_{PCBM} = 5.2 eV.

Chapter 1

THIN FILM CDTE DEVICE

1.1 CdTe PV Technology

This section discusses the motivation for thin film CdTe PV technology including the advantages of the CdTe material, the thin film device structure and associated electrical circuit, as well as a general discussion on solar cell efficiency and device performance measurements.

Since 2005, thin film solar cell technologies have begun to influence the photovoltaic (PV) market, due in part to a silicon shortage in 2005 which allowed thin film technologies to meet consumer demand in lieu of the more expensive c-Si technologies. In terms of PV production, in 2013, CdTe thin film PV represented over 50% of the thin film photovoltaic market share (CdTe PV production=1.9 GW_p) and 5% of the total photovoltaic market share [1].

The main advantages of the CdTe material are the following. First, the 1.5 eV CdTe material bandgap is favorable for the solar device since a theoretical device efficiency $\eta(E_g=1.5\text{ eV}) = 32\%$ based on single p-n junction Shockley Queisser (SQ) theory is close to the maximum SQ efficiency $\eta(E_g=1.34\text{ eV})=34\%$. Second, CdTe is highly absorbing with over 99% of light (photon energy $E<E_g=1.5$ eV) absorbed within 2 μm of CdTe due in part to the direct bandgap nature of the film [2]. Third, the material is a stable solid up to a melting temperature of 1100 ºC [3].

The CdTe cell is a heterojunction device consisting of a p-type polycrystalline CdTe layer and an n-type CdS layer which is fabricated in a frontwall superstrate

configuration in which light enters the cell through the glass substrate and window layer stack as shown in Figure 1-1. The window layer stack consists of a transparent conducting oxide (TCO), a high resistivity transparent (HRT) layer which acts as a buffer to prevent CdTe/TCO junction formation which results in excess dark current, and an n-type CdS layer which forms the primary junction with CdTe. Light passing through the window stack is absorbed in the p-type polycrystalline CdTe layer creating photocarriers which separate and travel to the respective positive and negative contacts. It is accepted that the window stack is optically parasitic to ultraviolet light and does not contribute to photocurrent in the cell. The back of the cell carries a nearly ohmic, positive electrical contact, typically consisting of Cu_2Te which forms a 0.3 eV barrier to the CdTe valence band [4].

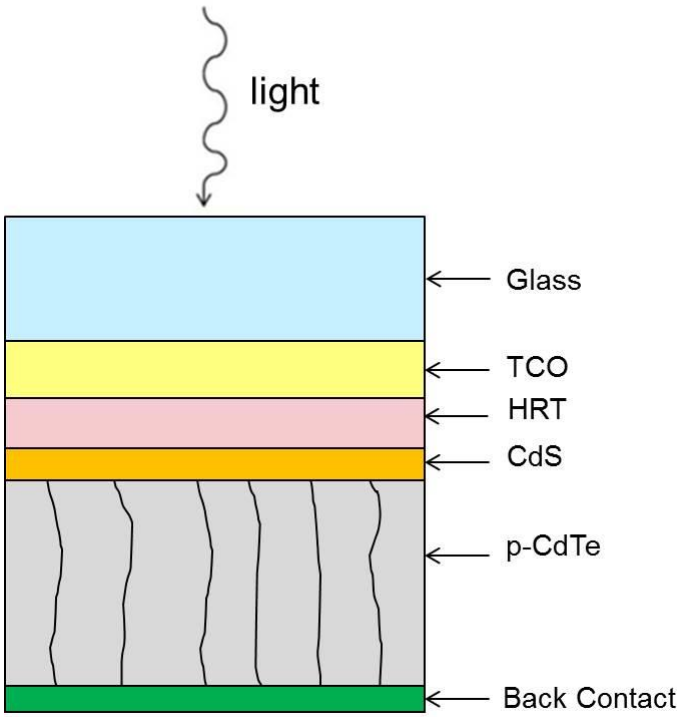


Figure 1-1: Schematic of a polycrystalline CdTe frontwall superstrate device. All layers except glass are polycrystalline, with the CdTe having the largest grains.

The equivalent circuit for a CdTe/Cu_2Te device structure is shown in Figure 1-2.

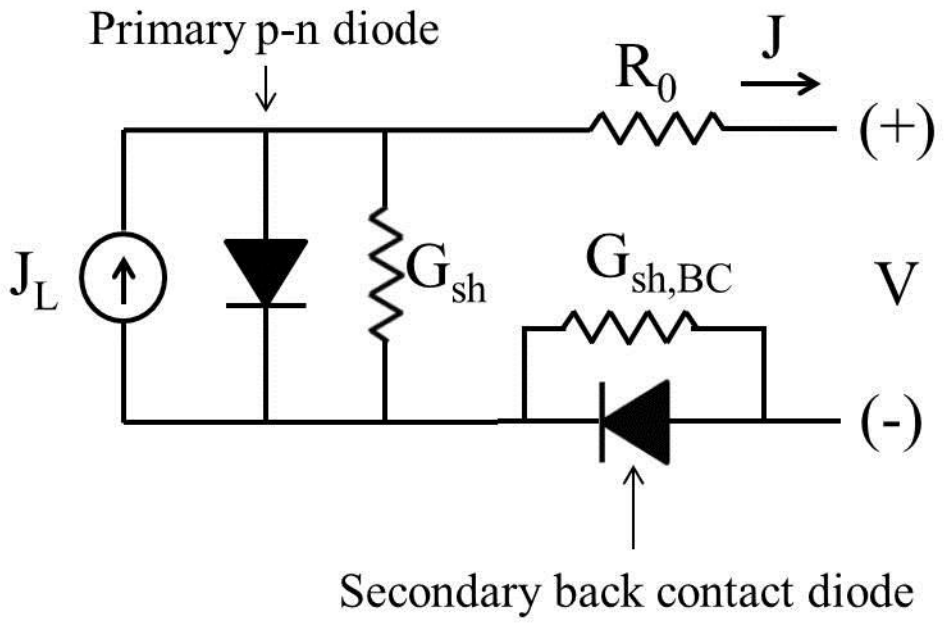


Figure 1-2: Equivalent circuit of a CdTe/Cu_2Te device with a primary p-n junction diode and secondary back contact diode. R_0 and G_{sh} are the series resistance and shunt conductance which are parasitic to device performance. The influence of the back contact in J-V curves is observed in forward bias with $V>V_{oc}$ or for $T<300$ ºK.

If the CdTe layer is sufficiently thick, the electrical transport physics of a CdTe device are dominated by the primary p-n junction limited by bulk recombination in the space-charge region of CdTe, so the voltage drop across the back contact is negligible. This is not the case however when reducing the CdTe thickness, which can reduce the bulk recombination volume and hence lead to a key role of the back barrier affecting electrical transport/voltage as will be discussed later (sections 1.3.1, 1.3.2).

To evaluate changes in the cell processing, the performance metrics of the solar cell must be clearly defined. The voltage and current density J are related as follows.

$$J = J_0 \exp\left(\frac{q(V - JR_0)}{AkT} - 1\right) + G_{sh}(V - JR_0) - J_L \qquad (1\text{-}1)$$

where J_0 is the recombination current, A is the diode factor which gives information on the recombination mechanism, and J_L as the collection current where $J_L=J_{sc}$ in a quality device with minimal recombination.

In order to optimize the efficiency of a solar cell, this requires maximizing the power produced by the device. The maximum efficiency for a solar cell under illumination at standard test conditions (STC: AM 1.5 spectra, T=300 ºK, light intensity = 1000 W/m^2) is represented by

$$\eta = \frac{V_{oc}J_{sc}FF}{1000\ W/m^2} \qquad (1\text{-}2)$$

with each device metric defined as follows: 1.) V_{oc}= open circuit voltage: the cell voltage under illumination when an infinite electrical load is applied, resulting in a net current J=0; 2.) J_{sc}= short circuit current: the cell current under illumination with R=0, resulting in V=0, and 3.) fill factor=FF: the ratio of the maximum power P_{max} available from the device to the product of V_{oc} and J_{sc}. The short circuit current J_{sc} for a solar device can be maximized by minimizing optical losses during light absorption, and electrical losses during light collection. V_{oc} is maximized by minimizing photogenerated electron recombination within the absorber layer and at cell layer interfaces, and to a lesser extent, by minimizing optical losses. FF is maximized by minimizing device series resistance R_s, shunt conductance G_{sh} and recombination mechanisms.

1.1.1 Recent Increases in Device Performance

From 2011 to 2015, the efficiency of champion small-area CdTe cells has increased from 17.3% to 22.1%, at a rate of 1.0%/year [5]. In recent years, high efficiency CdTe cells have exhibited the following device performance [6], [7] [8].

Table 1-1: Device performance of high efficiency solar cells. Bandgap data is calculated from long wavelength (λ>800 nm) spectral response measurements [6], [8]. Key: GE=General Electric Research, FSLR=First Solar

Author-year	V_{oc} (mV)	J_{sc} (mA/cm^2)	FF (%)	Eff (%)	E_g (eV)
FSLR-11'	845	27.0	75.8	17.3	1.47
GE-12'	857	27.0	79.0	18.3	1.48
FSLR-12'	852	28.6	76.7	18.7	1.46
GE-13'	857	28.6	80.0	19.6	Not given
FSLR-14'	876	30.3	79.4	21.0	1.37

Much of this increase in efficiency in the last few years has been the result of advances in solar PV technology from First Solar Inc. This has involved the use of a transparent window layer as well as a graded CdTe bandgap to the CdS/CdTe junction to increase light absorption (increased J_{sc}) [6], [9]. In addition, the increase in V_{oc} may result from compositional grading of the CdTe layer, thereby reducing the lattice mismatch with the CdS layer and hence reducing CdS/CdTe interface recombination.

The record CdTe module efficiency was accomplished by First Solar Inc. with 18.6% [9]. A state of the art commercial module (Series 4 CdTe Thin Film Module) is rated at 16% efficiency based on given values of module area (0.72 m^2) and maximum power at STC (117.5 W) [10]. For module production, the commercial first solar process utilizes a series of glass/TCO/CdS/CdTe/contact devices where the CdS and

CdTe layer are applied using a vapor transport deposition method [11]. CdTe polycrystalline lab cells developed using a vapor transport deposition of CdTe are associated with V_{oc} =800-840 mV.

1.2 Fundamental Limit of Efficiency for CdTe Devices

Using the bandgap values of the laboratory cells (Table 1-1), the theoretical V_{oc}, J_{sc}, FF, and efficiency limits can be computed using Shockley Queisser theory [12]. These device performance limits are shown as a function of the respective absorber bandgap of the quality lab devices in Table 1-2.

Table 1-2: Theoretical Shockley Queisser V_{oc}, J_{sc}, FF, and efficiency η based on absorber bandgap.

E_g (eV)	V_{oc} (V)	J_{sc} (mA/cm^2)	FF (%)	η (%)
1.48	1.21	29.7	89.8	32.3
1.47	1.20	30.0	89.8	32.3
1.46	1.19	30.4	89.7	32.4
1.37	1.11	34.0	89.1	33.6

Based on Shockley Queisser theory, a decrease in bandgap from 1.48-1.37 eV results in a decrease in V_{oc} (1.21-1.11 V) but increase in photon absorption and collection resulting in J_{sc} increasing (29.7-34.0 mA/cm^2) while FF shows little variation (89-90%). However, Shockley Queisser theory is based on a highly simplified model of a single p-n junction device where the only recombination mechanism is radiative. In a radiative recombination process, electrons between the conduction band recombine with holes in the valence band and hence the role of defects influencing bulk and interface defect recombination is neglected.

Theoretical device performance values are shown in comparison to experimental device performance of high efficiency cells (Figure 1-3).

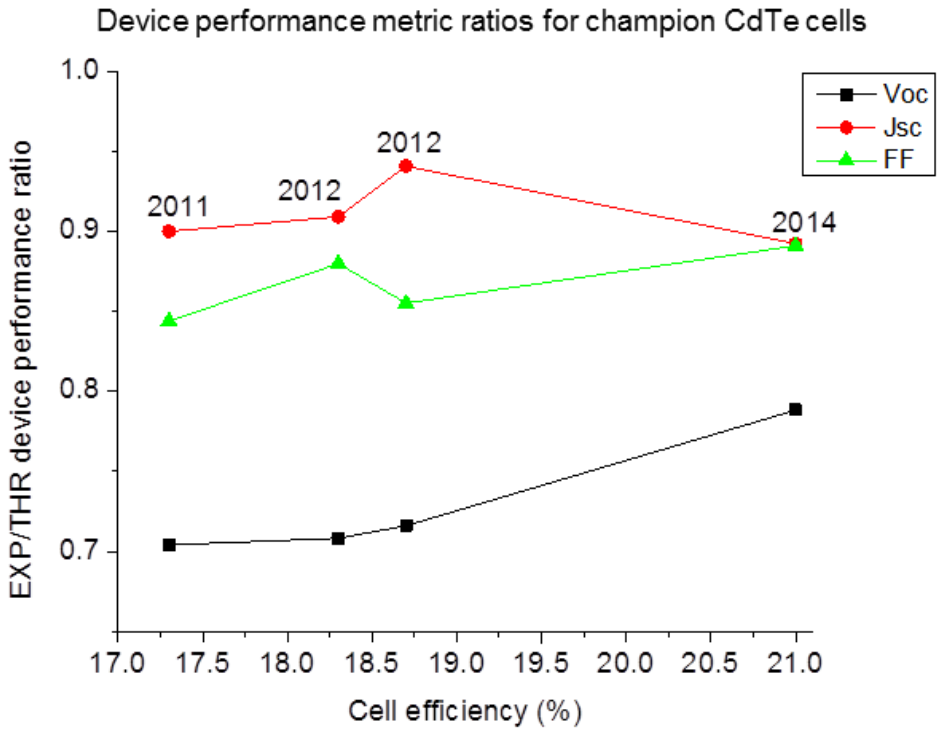


Figure 1-3: Device performance metric ratios for champion CdTe cells. For each champion CdTe cell, the experimental values of V_{oc}, J_{sc}, and FF are compared in a ratio to theoretical SQ values of V_{oc}, J_{sc}, and FF based on the CdTe material bandgap. The cell fabrication year is also listed above.

The data in Figure 1-3 and Table 1-1 reveal that J_{sc} and FF for champion cells have improved to 90% of the theoretical Shockley-Queisser values. In the past few years, J_{sc} values of champion cells have improved due to the minimization of optical losses, including minimizing CdS absorption which does not contribute to

photocurrent. FF values have improved by an increase in 5%. A V_{oc} increase of 31 mV has led to a slight improvement in V_{oc}. Overall, the data suggests that champion devices have reached 90% and 85% of their maximum J_{sc} and FF Shockley-Queisser values respectively, but only 80% of the maximum Shockley-Queisser V_{oc} value based on available bandgap data.

With a 1.37-1.50 eV bandgap for CdTe, the V_{oc} Shockley-Queisser limit is 1.11-1.23 V. Yet, high quality thin film polycrystalline CdTe cells exhibit V_{oc} = 840-876 mV [8], [13], while for single crystal CdTe devices, the highest recorded V_{oc} = 1017 mV [14].

1.3 Path to Higher Efficiency for CdTe Devices: Critical Issues

It is therefore a major goal of CdTe research to develop a CdTe cell with V_{oc} approaching that of the Shockley-Queisser V_{oc} limit. A CdTe cell with 1 V which maintains high quality values of J_{sc}~30 mA/cm^2 and FF=80 %, results in a 24% efficient cell. In order to increase V_{oc} in p-type CdTe devices it is crucial to minimize minority carrier (electron) recombination. Two major types of limiting recombination mechanisms for CdTe devices are Shockley Read Hall (SRH) and back barrier recombination, the latter which arises from a non ohmic back contact.

1.3.1 Shockley Read Hall Recombination

In CdTe devices, recombination can take place within the CdTe layer due to midgap bulk donor defects (Shockley Read Hall or SRH) and at the CdTe/CdS or CdTe/back-contact interfaces due to interface defects (surface recombination). Relations between V_{oc} and recombination are discussed in greater detail in Chapter 3.

Recombination can be represented by minority carrier lifetime. The effective lifetime is

$$\frac{1}{\tau} = \frac{1}{\tau_{bulk}} + \frac{1}{\tau_{surf}} \quad (1\text{-}3)$$

Bulk lifetime is represented by radiative, Auger, and SRH recombination.

$$\frac{1}{\tau_{bulk}} = \frac{1}{\tau_{rad}} + \frac{1}{\tau_{SRH}} + \frac{1}{\tau_{Auger}} \quad (1\text{-}4)$$

Auger recombination is estimated to result in a lifetime τ_{Auger}>0.1 s, much larger than measured minority carrier CdTe lifetimes ≤500 ns for quality single crystal CdTe and ≤ 40 ns for quality polycrystalline CdTe [15] [16]. Hence, Auger recombination does not limit lifetime. V_{oc}-temperature measurements in polycrystalline CdTe thin film devices suggest that a dominant recombination mechanism is SRH [17] which can be influenced both by foreign and intrinsic donor defects [18].

For CdTe devices SRH recombination can either take place within the CdTe space charge region (SCR) or the neutral CdTe bulk. Theoretical modeling of voltage dependent collection current where $J_L=J_L(V)\leq J_{sc}$ [19] implies that SRH recombination occurs within the SCR of a CdTe device. The SCR is typically 1-3 μm at equilibrium conditions based on capacitance voltage measurements and is generally greater than the region of light absorption/photogeneration of 1 μm where over 95% of AM 1.5 photons with energy ≥1.5 eV are absorbed. Figure 1-4 shows a biased thick CdTe device under illumination with a space charge and diffusion region.

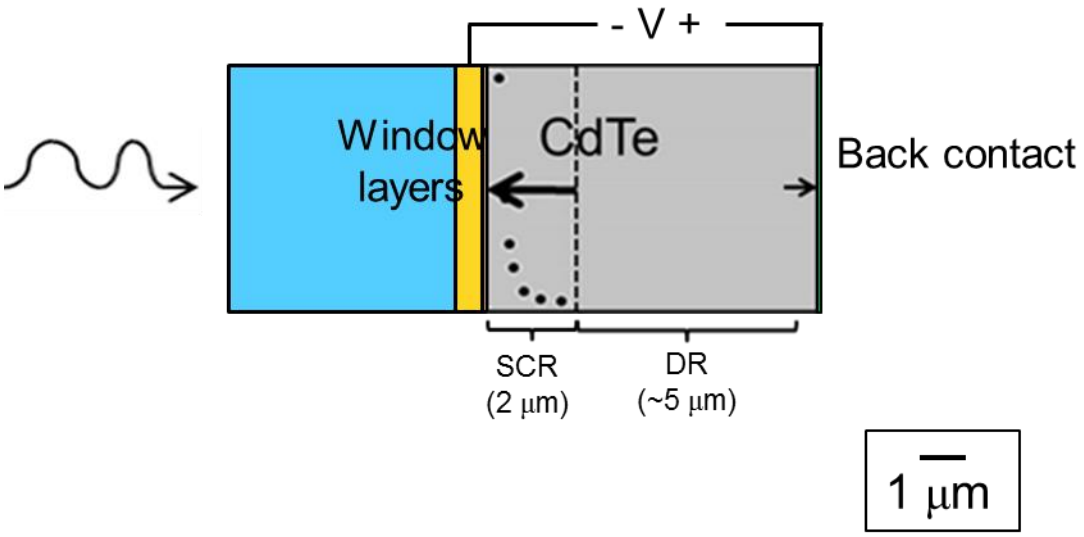


Figure 1-4: Thick CdTe device showing illumination on a 7 μm CdTe device, with an associated exponential absorption of light (black dots) in the CdTe space charge region and the space charge and diffusion region of CdTe. Left/right arrows represent the electric field (primary p-n and secondary back contact junctions respectively). Note that the width of the glass is actually on the order of mm and therefore not to scale. Key: SCR=space charge region, DR=diffusion region.

1.3.1.1 Doping

This section addresses how CdTe doping affects device operation and can be used to increase V_{oc}.

Present approaches to raise V_{oc} beyond the current 876 mV (polycrystalline) and 1017 mV (single crystal) involve the use of improving the CdTe bulk properties to minimize SRH recombination by reducing bulk defects, while increasing the CdTe hole concentration by doping the CdTe bulk which lowers the CdTe Fermi level E_F and subsequently increases the CdTe p-n junction built in field. If Boltzmann statistics are assumed at 300 ºK with kT=0.026 eV<<E_F, the relation between the hole concentration p and Fermi level E_F is given by

$$p = N_v \exp(-\frac{E_F - E_V}{kT}) \quad (1\text{-}5)$$

with E_v as the valence band energy, and N_v as the CdTe hole density of states. At 300 ºK, N_v is on the order of 10^{-19}/cm^3 assuming an effective CdTe hole mass ratio of 0.37-0.8 [20], [21], [22]. A polycrystalline CdTe device with V_{oc}=800-840 mV is typically doped with a hole concentration of 10^{14} holes/cm^3 which, using Eq. (1-5) implies a Fermi level difference E_F-E_v~300 meV.

A critical issue of doping CdTe to raise the hole concentration above 10^{14} holes/cm^3 is the formation of compensating donor defects which can lead to SRH recombination, and which form due to the defect chemistry of CdTe [23]. The formation of compensating donor defects can limit the CdTe hole doping to p~10^{14} holes/cm^3 and hence pin the Fermi level E_F-E_v~300 meV at 300 ºK. Recently though, progress was achieved in doping single crystal CdTe to 10^{16} -10^{17} holes/cm^3 which led to the record V_{oc}=1017 mV device [14]. The single crystal CdTe is free of the CdTe grain boundary defects associated with thin film polycrystalline CdTe and the CdTe bulk was doped to 10^{16} -10^{17} holes/cm^3. Using Eq. (1-5), a hole concentration of 10^{16} -10^{17} holes/cm^3 implies a Fermi level difference E_F-E_v~100-200 meV and hence ~100-200 meV lowering of E_F. While such methods have resulted in a 140-180 mV V_{oc} increase compared to polycrystalline CdTe with V_{oc} = 840-876 mV, further increasing the CdTe doping to further lower E_F and increase V_{oc} is a difficult task due to the defect chemistry of CdTe.

An alternative approach to increase V_{oc} is to reduce SRH recombination by reducing the CdTe defect/recombination volume. This involves developing a thin CdTe layer less with a CdTe thickness less than the space charge width i.e. $t_{CdTe} \leq$1

μm. However, the influence of the non-ohmic CdTe back contact becomes the limiting recombination mechanism controlling V_{oc}.

1.3.2 Non-Ohmic Back Contact

This section discusses the effect of a non-ohmic vs ohmic back contact on recombination. Previous experiments on developing thin ($t_{CdTe} \leq 1$ μm) CdTe devices with a non-ohmic Cu contact are also discussed where a V_{oc} decrease was observed with decreasing CdTe thickness, suggesting a back contact influence on recombination.

With a 1.5 eV contact and electron affinity of 4.3-4.5 eV [24], [25], the CdTe valence band is between 5.8-6.0 eV. A Cu_2Te back barrier forms a $\Phi_b = 0.3$ eV blocking (Schottky) contact and associated work function of 5.5-5.7 eV. The physics of a blocking barrier are illustrated in Figure 1-5.

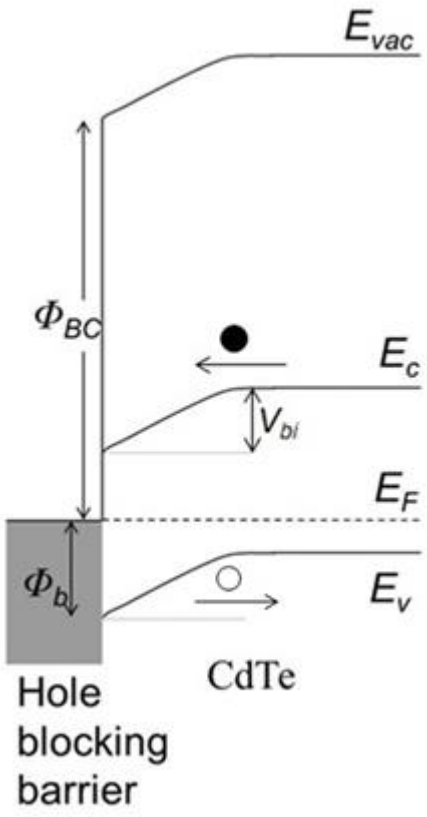


Figure 1-5: The energy levels of a CdTe/back contact representative of a blocking (Schottky) barrier. V_{bi} is the associated band bending. The black dot represents a recombining electron, while the white dot represents a blocked hole. Left/right arrows represent motion. Adapted from J. Singh, [26].

By examining the energy relations in Figure 1-5 between Φ_b, band bending V_{bi}, Fermi level E_F, CdTe valence band E_v, the following relation is obtained.

$$\Phi_b = E_{v,CdTe} - \Phi_{BC} \tag{1-6}$$

or

$$\Phi_{BC} < E_{v,CdTe} \tag{1-7}$$

Only hole carriers in the valence band with sufficient thermal energy can escape over the barrier. Electron minority carriers in the conduction band freely move from the semiconductor to the metal. For a CdTe p-n junction device with a blocking back contact, the electron minority carriers move, in the opposite direction to those of the primary p-n junction, thus forming a recombination current. For a sufficiently thick CdTe device ($t_{CdTe} \geq 4$ μm), a blocking contact will not affect V_{oc}. However, when CdTe devices are thinner than 1.5 μm, the blocking contact can have a strong influence on V_{oc} as shown Figure 1-6 for thin CdTe/Cu devices [27] [28] [29] [30].

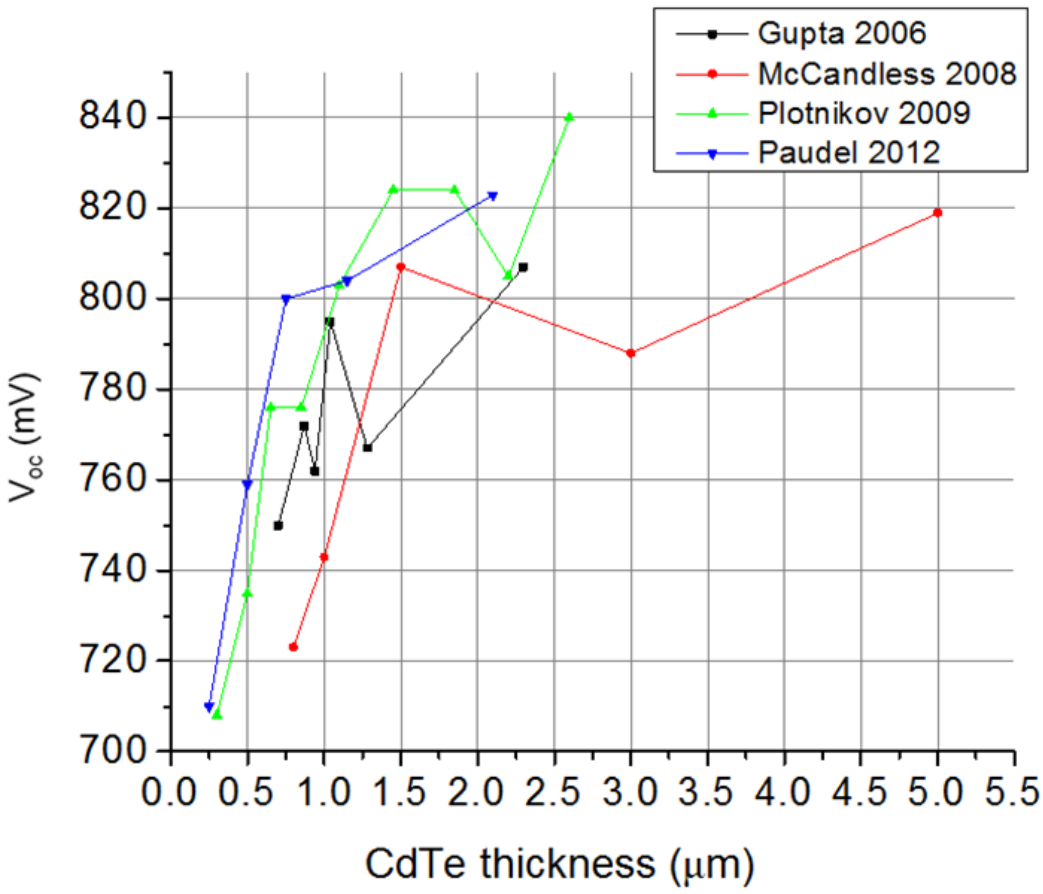


Figure 1-6: Experimental CdTe V_{oc} vs CdTe absorber thickness [27] [28] [29] [30].

If the decrease in V_{oc} with CdTe thickness shown Figure 1-6 is dominated by the barrier the Cu_2Te back contact, another solution to increase V_{oc} is to form an ohmic contact to a CdTe device. For an ohmic contact,

$$\Phi_{BC} \geq E_{v,CdTe} \tag{1-8}$$

The physics of an ohmic contact are shown in Figure 1-7 .

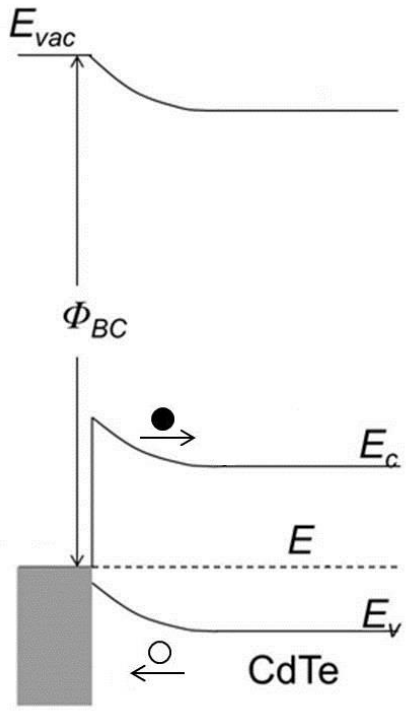


Figure 1-7: The energy levels of a CdTe/back contact which is ohmic to hole transport and blocks electrons. The black dot represents a blocked electron, while the white dot represents a hole which can move freely to the contact. Left/right arrows represent motion. Adapted from J. Singh, [26].

If the work function of the back contact satisfies Eq. (1-8, and if the back contact material exhibits a bandgap $E_{g,BC}$, an electron blocking barrier and subsequent V_{oc} increase should occur if [31],

$$E_{g,BC} > E_{g,CdTe} \tag{1-9}$$

and therefore a back contact material should exhibit $E_{g,BC}$>1.5 eV [31].

1.4 Thesis Statement

This goal of this research is to identify paths for increasing the open circuit voltage in thin film CdTe solar cells.

1.4.1 Objectives

Two critical objectives are identified for improving V_{oc}: reducing CdTe thickness and modifying the CdTe back contact.

1.4.2 Approach

The research, carried out at the University of Delaware's Institute of Energy Conversion (IEC), utilized an established baseline process for depositing the CdS and CdTe films and fabricating thin film CdTe solar cells with V_{oc}=800-840 mV and lifetime of 1-3 ns. The performance of these cells was fully characterized and 1-dimensional device simulations were carried out to evaluate the potential of the proposed work. The laboratory work carried out centered on three topics:

1. Evaluation of the V_{oc} relationship for CdTe thickness via the use of a liquid junction quinhydrone-Pt (QH-Pt) probe to a thinned window/CdTe stack and compare using device V_{oc} modeling based on CdTe thickness (Chapter 3, Chapter 5).

2. Evaluation of the V_{oc} performance of a CdTe/PCBM contact by characterizing PCBM morphological, optical, and CdTe device properties (Chapter 6).

3. Development of alternative contacts in reference to quality ($V_{oc}\geq$800 mV) CdTe baseline devices with the same window/CdTe processing but which utilize a Cu_2Te contact (Chapter 2, Chapter 4).

Chapter 2

EXPERIMENTAL

This chapter discusses the IEC baseline processing of CdTe devices as well as characterization techniques used to characterize completed devices. In addition, materials characterization techniques used to analyze CdTe and the carbon C-61 material PCBM are also discussed.

2.1 Device Fabrication: Baseline Device Structure

This section describes the IEC fabrication process of developing a CdS/CdTe superstrate device with a Cu_2Te contact. This process is used to develop baseline CdTe devices with $V_{oc} \geq 800$ mV and efficiency of 14% or higher. Fabrication steps in developing a CdTe device from the initial glass substrate to the final glass/CTO/ZTO/CdS/CdTe/Cu_2Te/Ni stack are described below.

2.1.1 Substrate/TCO (Sputtering)

A 4''x4'' 0.7-1.5 mm substrate of Corning proprietary glass, C065 or C165 are used and have the following properties: 1.) high light transmission, (92-93% transmission in the region λ>400nm for a 1.5mm sample [32]); 2.) low density of impurities; and 3.) a maximum working temperature up to 600 ºC. Both C065 and C165 glasses have the same chemical properties.

The glass is coated with Cd_2SnO_4, cadmium stannate (CTO), an n-type transparent conductive oxide. The CTO is deposited onto the glass substrate by radio frequency (RF) sputtering, to a thickness of 250-500 nm and then annealed in Ar/CdS

at 600 ºC forming a CTO layer with a resistivity of 10^{-4} Ω-cm and , bandgap of 3.6 eV, with a carrier density of $n_{CTO}>10^{20}$ cm^{-3} [33], [34]. This is followed by RF sputtering of a 75 nm highly transparent and resistive Zn_2SnO_4, zinc stannate (ZTO,) film on the CTO layer which is annealed for 550 ºC for 20 min in air to reduce film resistivity [35] resulting in a CTO/ZTO stack with a sheet resistance < 10 ohm/sq and measured 3.0 eV bandgap. The ZTO layer is necessary to prevent contact between the CdTe and CTO layers when applying a thin layer of CdS since a CTO/CdTe junction results in high interface recombination compared to that of CdS/CdTe [36].

2.1.2 CdS Growth

CdS films, with optical band gap E_G = 2.4 eV and typical thickness 60 nm, are deposited by a chemical surface coating deposition process that has been previously described [37] [27]. The films are deposited onto the glass/TCO/HRT stack and receive a $CdCl_2$ vapor heat treatment at 415ºC for 10 minutes in air [38]. The use of a $CdCl_2$ heat treatment of the CdS not only evaporates solvents left behind from the coating/solution process, but also recrystallizes the CdS film, increasing CdS grain size resulting in a higher crystalline quality (less defective) material [39]. This crystallographic change mitigates interdiffusion between CdS and CdTe which occurs after CdTe deposition and a secondary $CdCl_2$ heat treatment of CdS/CdTe, resulting in optical losses and reduced photcurrent [39].

2.1.3 CdTe Vapor Transport Growth

The IEC vapor transport (VT) deposition system is used to deposit the CdTe layer [40]. The deposition zone of the VT deposition system is schematically illustrated in Figure 2-1.

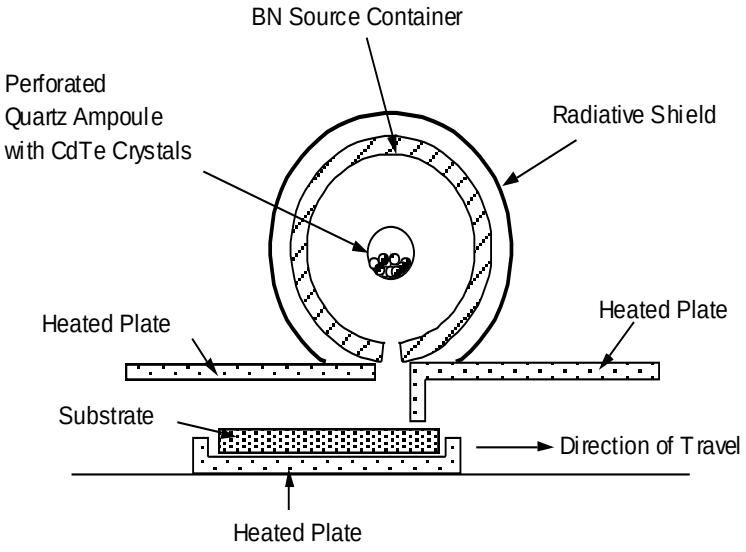


Figure 2-1: A vapor transport (VT) system is used to deposit elemental Cd and Te to a CdTe film. Used with permission from B. E. McCandless.

The basic operation of the VT system is as follows [40]. The perforated quartz ampoule holds CdTe crystals and the ampoule is enclosed in a BN source container. The container is heated, and the CdTe crystals sublime, forming a Cd and Te_2 vapor mixture according to the congruent and reversible equilibrium process: $CdTe \leftrightarrow Cd + 1/2Te_2$. A nitrogen ($N_2$) carrier gas is externally supplied into the perforated, heated ampoule, entraining the vaporized Cd and Te_2. The N_2:Cd:Te_2 vapor then flows out of the perforated ampoule and BN source container, onto a plate which holds the window stack substrate. The substrate is at a fixed temperature which can be varied between 500 and 630 ºC and translates horizontally beneath the source at a distance of 1.5 cm, while the N_2:Cd:Te_2 vapor flows over the substrate at a pressure of 20 torr. Since the vapor is at a temperature ~800 ºC and the substrate is held at the cooler temperature of 590-630 ºC, the now supersaturated vapor species condense and react on the substrate

to form a polycrystalline CdTe film. An O_2 background pressure of 0.5% O_2:99.5% N_2 is also added to the N_2:Cd:Te_2 vapor at a rate of 3 sccm to increase CdTe film density and minimize CdTe pinhole formation. CdTe deposition occurs at a rate of 8-10 µm/min and a 4-10 µm CdTe film is formed on the substrate.

A high deposition temperature of 590 ºC is needed to develop sufficient native Cd-vacancy defects to produce bulk CdTe p-type doping [3] and previous studies have shown that anneal temperatures of 550 ºC or above on polycrystalline CdTe films with a subsequent $CdCl_2$ treatment (section 2.1.4) can raise V_{oc} above 800 mV [41].

The thickness of CdTe is gravimetrically estimated for each run by measuring the CdTe mass, m_{CdTe} deposited on the glass/CTO/ZTO/CdS stack where m_{CdTe} is determined by the difference in the 4"x4" substrate stack before and after CdTe deposition. By knowing the density of CdTe, the volume of CdTe and hence thickness can be estimated. With typical thicknesses of 4-9 µm and typical roughness values of 500 nm, the CdTe volume can be approximated as a rectangular slab with $V_{CdTe}=A_{CdTe}t_{CdTe}$.

After CdTe VT deposition, samples from the 4" x 4" window/CdTe stack are cut into 2''x1'' or 1''x1'' pieces and given the numbering scheme VTm.n, where m is the VT run number and n=1-8 is the sample position (Figure 2-2).

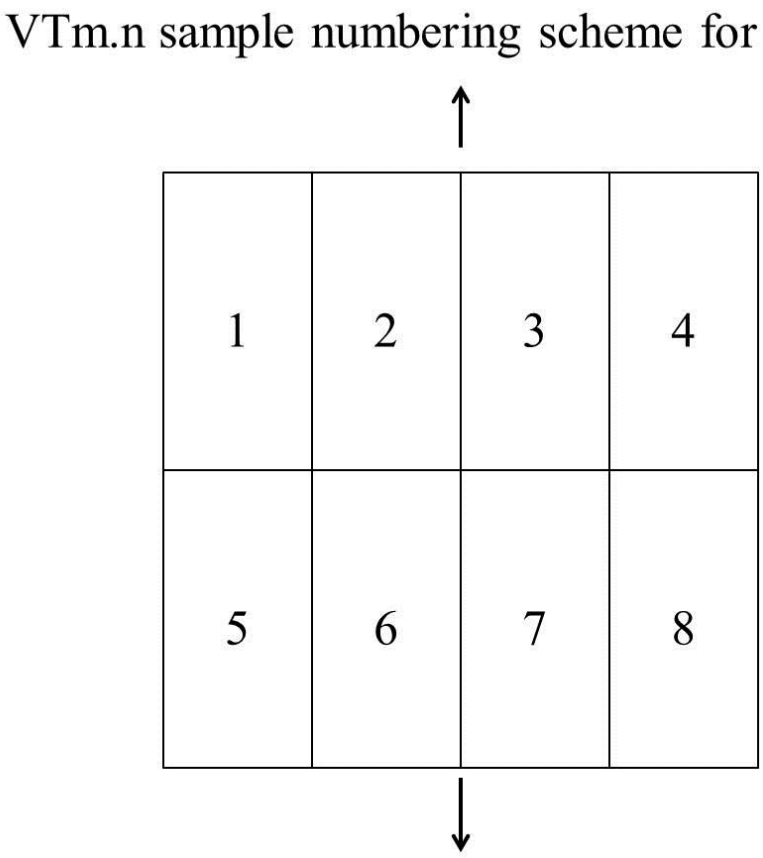


Figure 2-2: The position numbering n for a samples cut from a window/CdTe stack and given a run number VTm.n with n=1-8. Arrows indicate the direction of substrate travel during vapor deposition.

Due to imperfections in depositing CdTe uniformly, slight CdTe thickness non-uniformity exists at the edges of samples cut from the 1,5,4, and 8 positions. It is suspected that a CdTe thickness difference by as much as 20% exists between the center and edge thicknesses in the transverse direction to substrate travel [42].

Once the CdTe deposition process is complete and the sample has been cooled to room temperature, the resulting CdTe layer is highly defective with un-passivated

grains. These may consist of dislocations, twin boundaries, voids, etc. which imply a highly defective material with dangling bonds. In order to improve the quality of the CdTe film, the sample is given a subsequent high temperature anneal in $CdCl_2$ vapor as discussed in the next section.

2.1.4 $CdCl_2$ Treatment of CdTe

The use of the $CdCl_2$ heat treatment improves device quality as follows [18]. First, CdTe grains with reduced CdTe grain boundary defects are obtained by recrystallizing the CdTe layer, resulting in increasing CdTe grain growth. This occurs for films processed with or without oxygen present in the ambient. However, performing the treatment in air, the CdTe film becomes more p-type due to increased CdTe hole concentration by the formation of cadmium vacancies from the grain surfaces to the grain interiors. The $CdCl_2$ treatment also helps to passivate the interface between CdTe and CdS, as a result of interdiffusion of sulfur from CdS into CdTe along the polycrystalline CdTe grain boundaries and into the CdTe bulk crystals [43], while thinning the CdS layer to $t_{CdS} \leq 40$ nm [27].

The vapor $CdCl_2$ heat treatment was applied to the CdTe surface of the cut 2”x1” or 1”x1” samples based on an optimized process for the 4-9 μm thick CdTe [27]. First, 1% wt. solution of $CdCl_2$ in methanol is applied to the CdTe surfaces on the cut samples. Second, the samples are then dried and placed between two glass cover plates with 1 mm spacing between the CdTe sample and glass, before being placed in an oven from 422±2.5 ºC for an anneal time of 30 minutes. Within 5 minutes, the sample is heated to the oven temperature, and hence the annealing time is 25 min.

2.1.5 Cu_2Te Back Contact Structure

After the CdTe layer has been subject to $CdCl_2$ treatment and cooled down, the next steps involve: 1.) a 0.01 wt% bromine methanol (Br:Me) etch for 5-10 s to remove oxides developed during $CdCl_2$ treatment [27]; 2.) a viscous ethylenediamine/glycerin etch, in a 5:1 volume ratio, and subsequent 80 ºC heat treatment to develop a Te rich surface layer; 3.) electrodeposition of a ~5nm copper layer; 4.) electrodeposition of a 50nm nickel current carrying secondary contact; 5.) a 180 Cº Ar heat treatment for 30 minutes to develop a layer of Cu_2Te on the CdTe surface and diffuse Cu into the CdTe structure which improves CdTe bulk p-doping [44], and; 6.) a subsequent Br:Me etch for 2 s to eliminate excess metallic Cu and oxides which may form between Cu and Ni or on the Ni surface.

The work-function of Cu_2Te is as follows. Assuming 1.) 5.8 eV valence band for CdTe; and 2.) 0.3 eV blocking barrier for CdTe/Cu_2Te [4]; this suggests that the Cu_2Te layer exhibits a work function of 5.5 eV. Although the back contact consists of nickel with a lower work function of 5.15-5.35 eV [45], the electrical properties of the CdTe-back contact junction are dominated by the Cu_2Te layer and not by the contacting material [46].

After the back contact layers have been fabricated, the sample consists of 8 cells with areas of 0.36 cm^2. Before measurements can be done however, small portions of the sample are scratched off (taking care to avoid cell regions) and an indium solder is applied to the TCO layer. Figure 2-3 shows a cross sectional cell schematic of the completed device while Figure 2-4 shows with a top-down picture of the sample. A cell labeling schematic is shown in Figure 2-5.

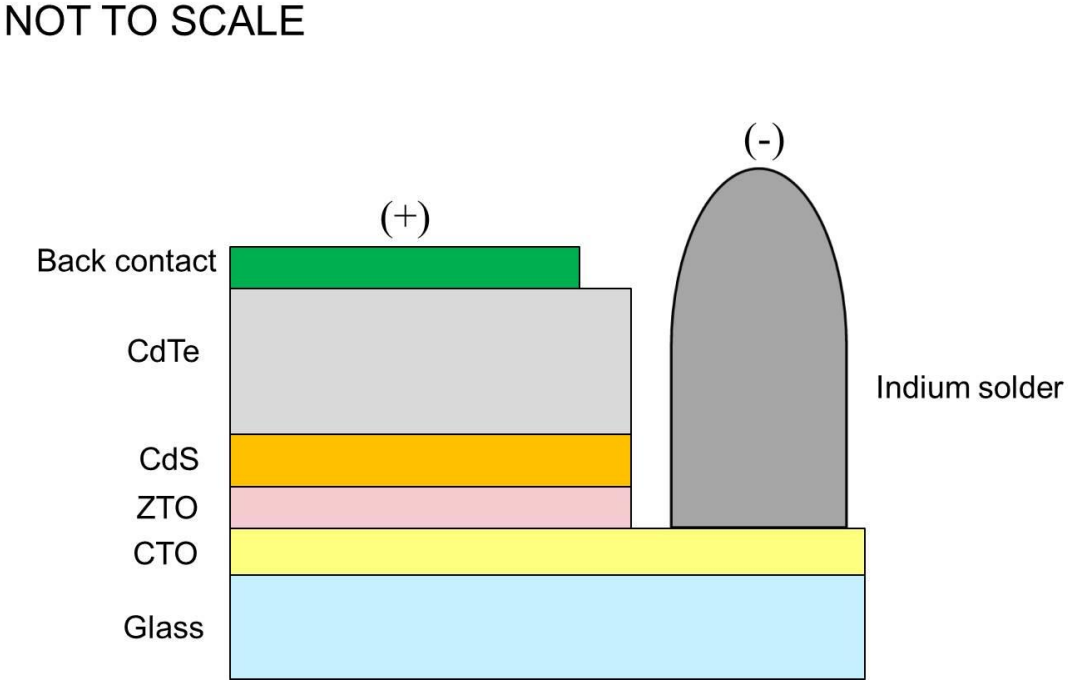


Figure 2-3: A cross sectional schematic of a final baseline device.

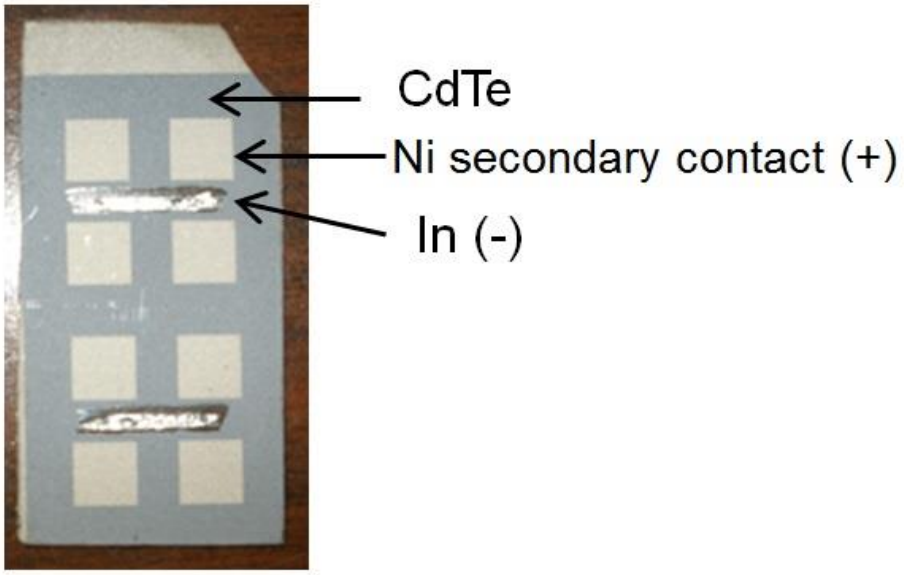


Figure 2-4: A top down picture from the back contact side of a 1”x2” CdTe sample. The silver streaks represent indium solder while the squares represent a 36 mm^2 cell. The surrounding darker gray area is CdTe, which although is coated with a thin layer of Cu_2Te, was not given Ni deposition. By isolating areas of the sample with nickel, this isolates the electrical properties of each cell.

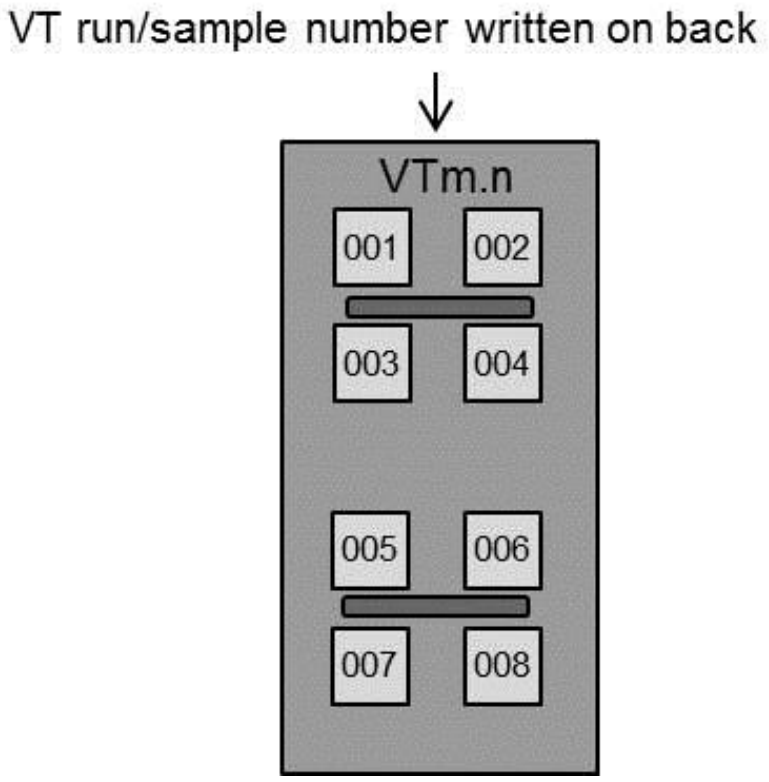


Figure 2-5: Cell labeling schematic for a CdTe sample.

2.2 Materials Characterization

This section discusses materials characterization which was carried out on CdTe devices and the CdTe alternative contact PCBM material. The growth and characterization of the PCBM contact materials is disrobed in Chapter 5.

2.2.1 FIB/SEM

Thickness measurements on CdTe and PCBM were performed using a Zeiss Auriga-60 CrossBeam workstation setup for focused ion beam (FIB) cross section SEM measurements.

For the SEM/FIB technique, the Auriga-60 setup involves imaging the sample of interest in an SEM vacuum chamber. The sample is then tilted 54 º to the SEM detector and aligned both to the SEM detector and a focused Ga ion beam which mills a small area of the sample (typical area<100 μm^2), exposing the sample cross section (Figure 2-6).

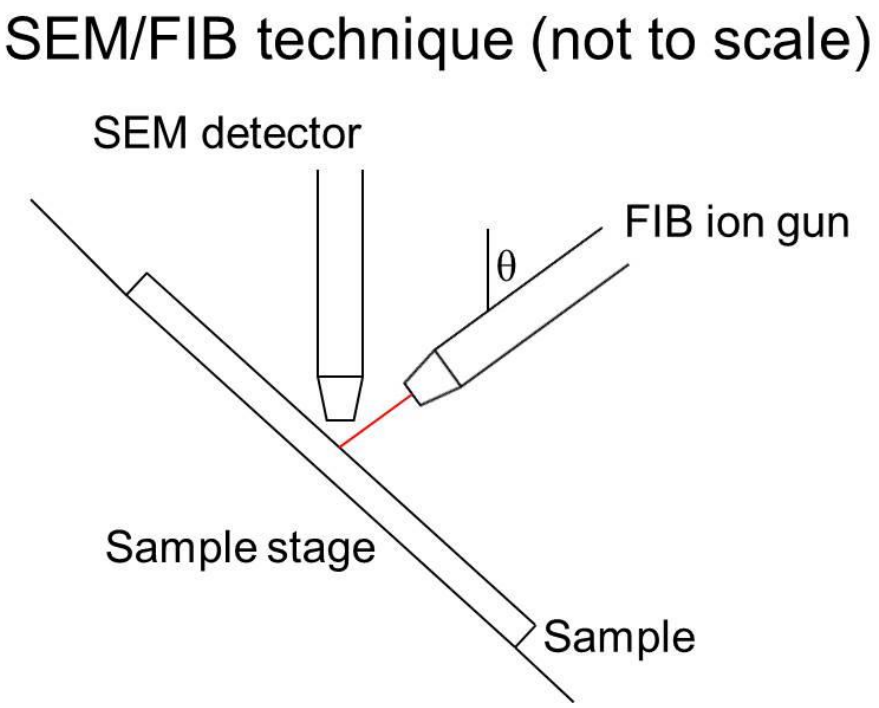


Figure 2-6: SEM/FIB technique. The sample is placed in a vacuum SEM chamber and tilted at an angle θ=54º so that the FIB ion gun is perpendicular to the sample. The red beam represents Ga ions which mill a cross section into the sample, visible to the SEM detector which is aligned to the milled cross section. For simplicity, the primary electron beam and resulting secondary electrons are not shown.

Morphology measurements on PCBM were performed using the Auriga-60 setup and a JSM-7400 SEM workstation. The Auriga-60 setup was used for backscattering image analysis on CdTe/PCBM samples to determine area coverage and the process is described in further detail in section 6.3.2).

2.2.2 Surface Profilometry

A Dektak 3 surface profilometer was utilized to characterize CdTe roughness. The profilometer scan was taken on the CdTe surface, over a 500 μm range using a 250 nm step size (N=2000 pts).

Using raw profilometer data of vertical position y vs horizontal position x, the vertical y-position was leveled through an MSE minimization procedure as follows: 1.) a linear function f=mx+b is introduced with an initial guess of m and b; 2.) a "corrected" vertical position y-f is calculated; 3.) MSE minimization using

$$MSE = \frac{1}{N}\sum_{i=1}^{N}(y-f)^2 \tag{2-1}$$

with N=2000 is the number of vertical y measurements. Then a plot of leveled vertical position y-f vs x can be analyzed.

2.2.3 T&R

The PCBM optical properties were evaluated by transmission and reflection (T & R) measurements on SLG/PCBM structures using a Perkin Elmer Lambda 750 spectrophotometer, from 400-800 nm.

2.2.4 Ellipsometry

This section discusses ellipsometry which was used to optically characterize PCBM.

2.2.4.1 Theory

Consider the reflection of electromagnetic light from a sample with an initial electric field plane wave as

$$\widetilde{\boldsymbol{E}}_{\boldsymbol{i}} = \widetilde{\boldsymbol{E}}_{\boldsymbol{s,i}}\hat{\boldsymbol{s}} + \widehat{\boldsymbol{E}}_{\boldsymbol{p,i}}\hat{\boldsymbol{p}} \tag{2-2}$$

and resulting in elliptical polarized plane wave after reflection

$$\widetilde{\boldsymbol{E}}_{\boldsymbol{r}} = \widetilde{\boldsymbol{E}}_{\boldsymbol{s,r}}\hat{\boldsymbol{s}} + \widehat{\boldsymbol{E}}_{\boldsymbol{p,r}}\hat{\boldsymbol{p}} \tag{2-3}$$

The tilde notation is used to show that the plane wave components are complex with an associated magnitude and phase. The **s** component of light is parallel to the sample surface while the **p** component is perpendicular and within the plane of incidence. This is illustrated in Figure 2-7.

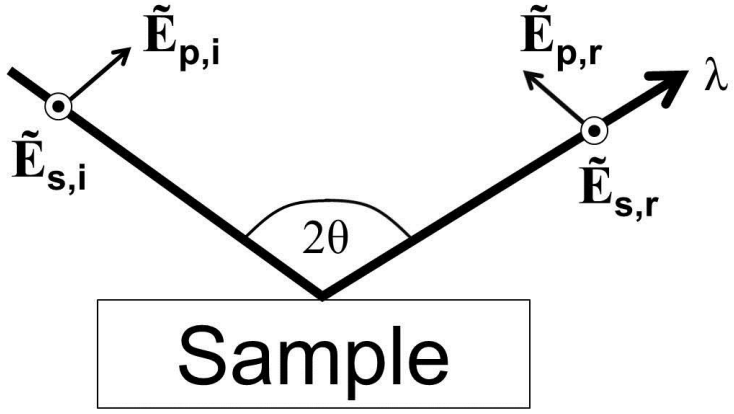


Figure 2-7: Reflection off of a sample for an ellipsometry experiment. Light at a specific wavelength λ, and angle of incidence θ reflects off the sample and is elliptically polarized after reflection. The **s** component of light is parallel to the sample surface (out of the page), while the **p** component of light is within the plane of incidence.

A complex quantity $\tilde{\rho}$ is introduced such that

$$\tilde{\rho} = \tan(\Psi)e^{i\Delta} \tag{2-4}$$

where

$$\tan(\Psi) = \frac{|\widetilde{R_p}|}{|\widetilde{R_s}|} \tag{2-5}$$

$$\widetilde{R_p} = \frac{\widetilde{E_{p,r}}}{\widetilde{E_{p,\iota}}} \tag{2-6}$$

$$\widetilde{R_s} = \frac{\widetilde{E_{s,r}}}{\widetilde{E_{s,\iota}}} \tag{2-7}$$

Hence, tan(Ψ) gives the amplitude of the **p** and **s** reflection coefficients, while Δ gives the phase difference between the s and p components of reflected light. The value of Ψ ranges from 0-90° while Δ ranges from 0-180°.

For an optical material, refraction and absorption can be described by a complex index of refraction $\tilde{n}$, defined as

$$\tilde{n}(\lambda) = n(\lambda) + ik(\lambda) \tag{2-8}$$

where k is the extinction coefficient, which is related to the absorption coefficient α by

$$k(\lambda) = \frac{\alpha(\lambda)\lambda}{4\pi} \tag{2-9}$$

The n and k optical values can be related to electric field components and hence Ψ and Δ via the use of Snell's law and Fresnel equations [47]. When the reflected light only has an **s** component (Figure 2-7), $\widetilde{R_p}$=0, and the angle θ at which this occurs is known as the Brewster angle θ_B.

2.2.4.2 VASE

Variable angle spectroscopic ellipsometry (VASE) [47] is a non-invasive (non-contacting) technique where an incident monochromatic beam of polarized light reflects of a multilayered sample on a rotating stage to obtain experimental Ψ^e, Δ^e data. The resulting optical constants n, k and material thickness are calculated through an MSE fit of Ψ and Δ. Experimental data is taken at or near the Brewster angle θ_B which allows the most accurate calculations of n, k, and thickness. For accurate measurements, sample roughness should be less than 10% of the wavelength of the probe beam [47].

The basic equipment operations for a VASE measurement are as follows: 1.) input polarizer emits a linearly polarized monochromatic beam at a specific wavelength λ with a known phase shift between the s and p components of light; 2. the beam reflects off a sample, becoming elliptically polarized; 3.) reflected light then passes through an analyzer used to determine the phase difference and amplitudes of the reflection p and s components of light and 4.); finally, light is detected using Si and InGaAs detectors and the detector signal is sent to a computer. The sample and detector angle are controlled by a goniometer. Equipment used to perform VASE measurements is shown in Figure 2-8.

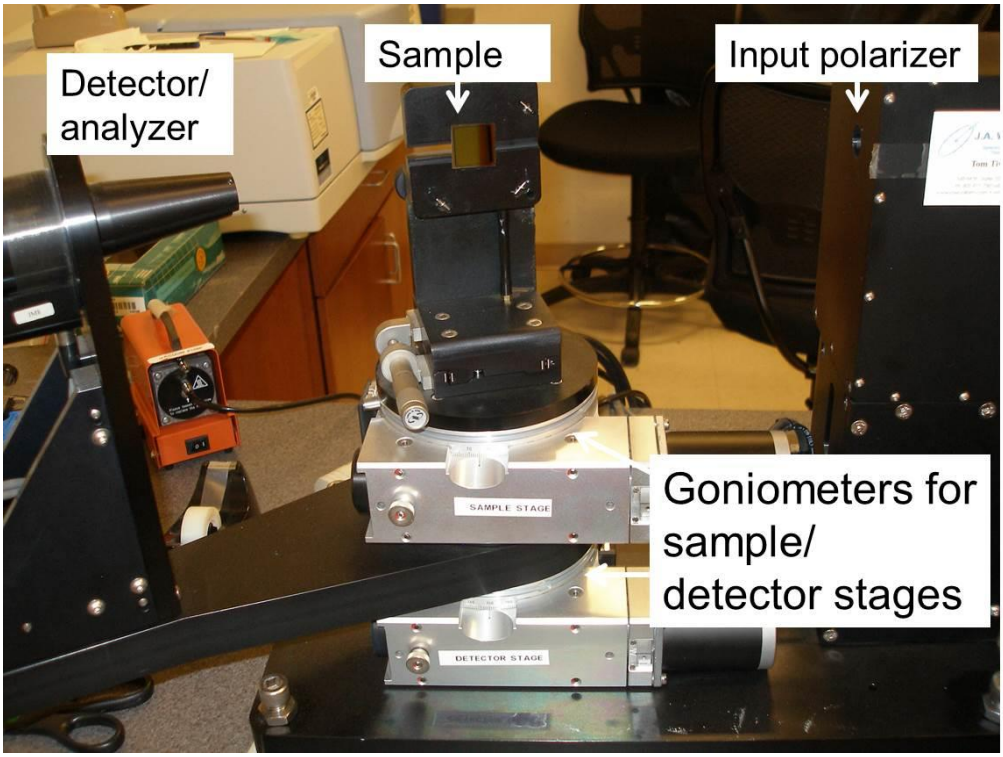


Figure 2-8: Ellipsometery equipment. Not pictured are a monochromator, and fiber optic cables used for the input beam, and external hardware used to control ellipsometry motion and the light beam.

Further details of the VASE equipment is described in reference [42].

The software used to collect Ψ^e, Δ^e measurements was WVASE32v.3.337b and WVASE32v.3.768. The procedure for data collection for a sample using VASE is the following.

1. Calibration of the sample angle of incidence θ and detector angle 2θ.
2. An ellipsometry measurement is carried out on a standard Si sample placed in the VASE holder to ensure that the equipment is calibrated. This involves beam alignment to maximize light collection at the detector.
3. The sample of interest is put in lieu of the Si sample and another beam alignment is performed to maximize light collection.
4. An ellipsometry measurement is performed to determine $\theta_B(\lambda)$, where Ψ is minimized and $\Delta=90°$.
5. Data collection of Ψ and Δ on Si/ITO and Si/ITO/PCBM samples is taken as follows.
    i. Constraining θ to the Brewster angle $\theta_B(\lambda)$ upper/lower limits so that Δ data is sensitive to film characteristics. Three values of θ are used with $\theta_B \pm \Delta\theta_B$, $\Delta\theta_B \leq 10^o$
    ii. λ = 400-900 nm with $\Delta\lambda \leq 10$ nm.

Using the CompleteEASE$^{(R)}$ software v.4.76. from J.A. Woollam, the Ψ^e, Δ^e data was fit using calculated models of Ψ^c, Δ^c which are generated by $n(\lambda)$, $k(\lambda)$ functions and input values of thickness [48]. Fitting calculations between Ψ^e, Δ^e and Ψ^c, Δ^c are performed by minimizing an MSE value using an algorithmic method where the MSE is defined as [48],

$$MSE = 1000\sqrt{\frac{1}{3n-m}\sum_{i=1}^{n}[(N_i^e - N_i^c)^2 + (C_i^e - C_i^c)^2 + (S_i^e - S_i^c)^2} \quad (2\text{-}10)$$

where n is the number of wavelengths (3n= number of experimental Ψ,Δ pairs), m is the number of model variable parameters, N=cos(2Ψ), C=sin(2Ψ)cos(Δ) and S=sin(2Ψ)sin(Δ). The larger the value of 3n-m, the larger the system of equations for the model. Hence, for multiple values of θ, and λ, 3n>m and the system of equations is overdetermined, allowing greater accuracy for n(λ), k(λ), and thickness.

The model used to generate optical Ψ^c, Δ^c functions to fit with optical Ψ^e, Δ^e data for Si/ITO/PCBM samples and determine the PCBM n, k optical constants is described as follows.

1. The Si layer is modeled as an infinitely thick with a top 1.5 nm SiO_2 oxide where the n and k optical constants for both layers are taken from a material database included in the CompleteEase software package software database.
2. The n, k ITO layer optical constants and thickness are modeled based on measured Ψ^e, Δ^e data taken on a Si/ITO sample prior to PCBM deposition as follows.
    a. An ITO general oscillator model is used from the CompleteEase software material database with predetermined input parameters to generate initial functions n(λ) and k(λ) and hence initial theoretical values of Ψ, and Δ using an initial thickness guess<200 nm.

b. Then, using iterative fitting calculations between theoretical and experimental values of Ψ, and Δ, n_{ITO}, k_{ITO} and t_{ITO} are determined with MSE<10.

3. After PCBM deposition (section 6.3.1), the n, k ITO layer optical constants and thickness are modeled as based on measured Ψ^e, Δ^e data taken on a Si/ITO/PCBM sample as follows.
    a. First, using a B-Spline model for PCBM with PCBM thickness and roughness based on FIB/SEM measurements, constraining generated $n(\lambda)$ and $k(\lambda)$ functions to be Kramers-Kronig consistent with k>0. Then MSE is minimized using the B-Spline model.
    b. Then the B-Spline model is converted to a Tauc-Lorentz general oscillator model used to generate $n(\lambda)$ and $k(\lambda)$. With PCBM thickness and roughness input estimates, n_{PCBM}, k_{PCBM}, and t_{PCBM} are calculated with MSE<10.

The B-Spline and Tauc-Lorentz oscillator models are used for films with light absorption characteristics, and are discussed in greater detail in reference [48].

2.3 Device Characterization

This section focuses on experimental techniques used to characterize CdTe device performance, doping and space charge width, photocurrent losses, optical properties, back contact properties, and recombination mechanisms.

2.3.1 Current Density vs. Voltage

JV measurements were taken on CdTe devices at standard test conditions, 1000 W/m2, 300 ºK, AM 1.5 spectra [49], using a four probe current/voltage setup,

temperature sensor, and Oriel solar simulator. For a J-V measurement, a Keithley 2400 Source Meter is used to source voltage and current values and write this information to a computer which converts the current to current density (J), where J = I/active area. The system is illustrated in Figure 2-9.

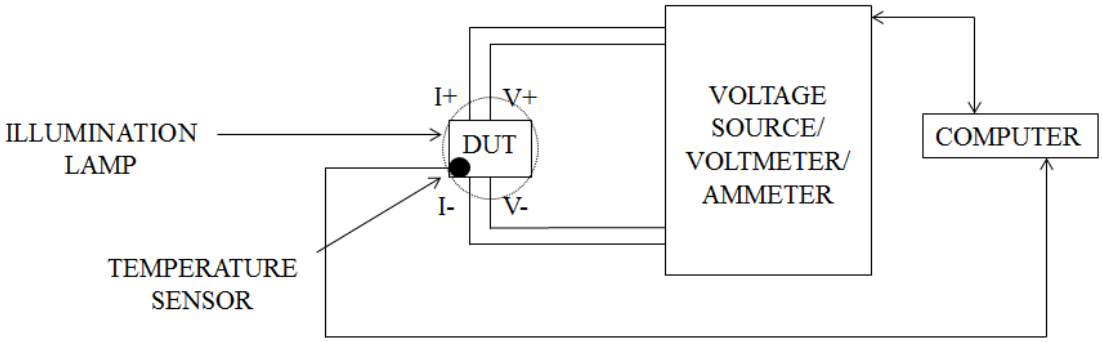


Figure 2-9: J-V cell testing schematic. The dotted circle represents the illumination lamp/solar simulator which is placed underneath the cell. The black dot represents a temperature sensor which is placed on the surface of the device. Further details of the setup and equipment are described in references [50] and [49].

Before J-V measurements are taken, the light source is calibrated to 1000 W/m^2 with a standard Si cell by adjusting the light to a previously measured J_{sc} value of the standard cell, which was taken at NREL under AM 1.5 conditions.. Then, the Si calibration cell is removed in lieu of a CdTe cell which is placed over the illumination lamp and contacted. Measurements are done in both the light and the dark using a 4 mV voltage increment. To evaluate the repeatability of device performance, a hysteresis evaluation of the device JV profile is also performed by sweeping from reverse to forward bias (up sweep) and then back from forward to reverse bias (down

sweep). Therefore, for each cell, four measurements (dark up, dark down, light up, light down) are taken. Typical reverse and forward bias voltage limits are -0.3 to 1.2 V. Once the current density reaches a value of 50 mA/cm^2, measurements automatically stop in order to prevent cell damage from I^2R dissipation.

2.3.2 Quantum Efficiency

A critical technique for interpreting the photocurrent of a solar cell is by measuring the quantum efficiency (QE). QE measurements are used to evaluate photocurrent losses spatially within the cell, and obtain optical properties of the cell layers. QE is a dimensionless ratio as a function of wavelength λ which measures the fraction of collected electrons to incident photons when the device is irradiated by a monochromatic beam.

$$QE = \frac{Number\ of\ electrons\ that\ exit\ the\ device}{Incident\ Photons(\lambda)} \qquad (2\text{-}11)$$

Assuming that the semiconductor has a single bandgap, by energy conservation, the number of electrons produced cannot exceed the incident number of photons. Hence,

$$0 \leq QE(\lambda) \leq 1 \qquad (2\text{-}12)$$

A QE of 1 implies that every photon and resulting photocarriers were collected. A QE less than 1 implies either 1.) an optical reflection or parasitic absorption loss 2.) photocurrent recombination loss, or 3.) an incomplete absorption of photons.

The QE as defined in Eq.(2-11) is also known as the external quantum efficiency QE_{ext}. The internal quantum efficiency is representative of only photocarrier generation and collection within CdTe and defined as

$$QE_{int} = \frac{Number\ of\ electrons\ that\ exit\ the\ device}{Photons\ absorbed\ within\ CdTe(\lambda)} \quad (2\text{-}13)$$

However, at short wavelengths where window layer absorption affects QE_{ext} (λ<600 nm), internal quantum efficiency is difficult to measure since determination of the photons absorbed within CdTe at a certain wavelength λ requires knowledge of the amount of photons at wavelength λ absorbed by the window layers. Due to internal reflections within the window layers, the fraction of light absorbed within the window layers and subsequent transmission of light into CdTe cannot be modeled with a simple Beer-Lambert law relationship. For this work, measurements of QE_{ext} are of greater relevance and the terms QE and QE_{ext} are used interchangably.

Quantum efficiency is affected by optical or photocurrent losses as illustrated in Figure 2-10.

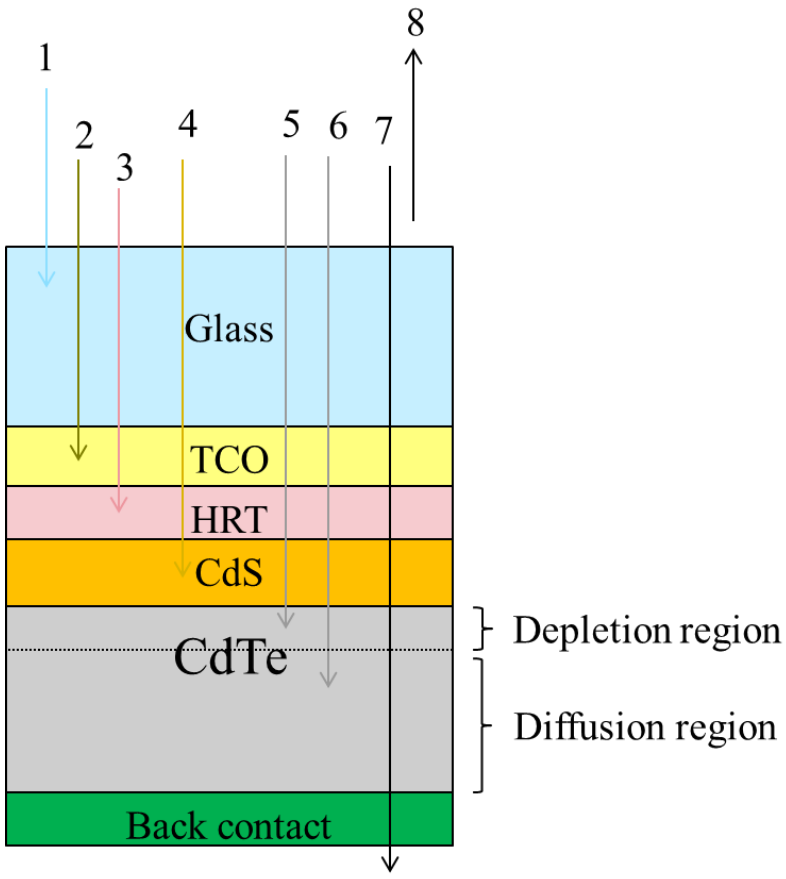


Figure 2-10: An illustration of photocurrent losses. 1.) Absorption in glass, 2). Absorption in the TCO layer, 3). Absorption in the HRT layer, 4). Absorption in the CdS layer. 5). Absorption in the CdTe depletion region which results in incomplete collection due to bulk or interface recombination, 6). Absorption in the CdTe diffusion region which results in incomplete collection due to bulk recombination. 7) Incomplete absorption. 8.) Reflection.

An example QE curve from experimental data is shown in Figure 2-11.

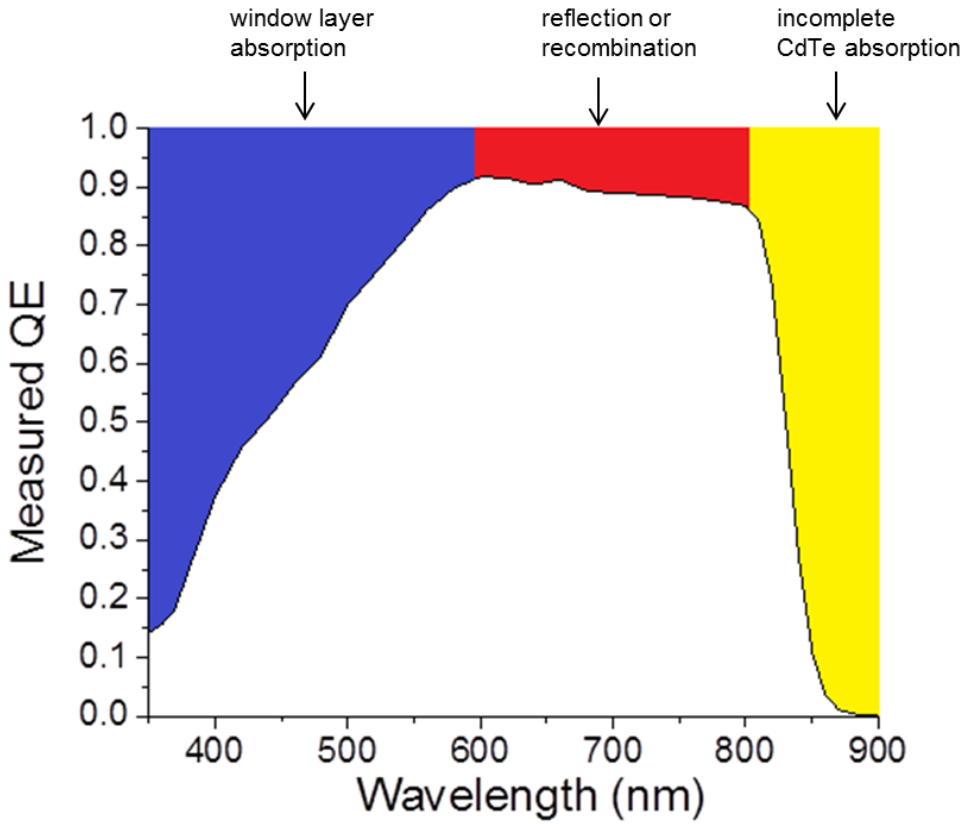


Figure 2-11: Experimental QE curve (black curve) illustrating dominant photocurrent losses resulting in QE<1. These photocurrent losses are discussed in greater detail in section 0.

A nonzero QE is obtained for wavelengths between 350-900 nm. For light with wavelength $\lambda<350$ nm, light intensity is insufficient and is also parasitically absorbed by the CdTe window layers and hence QE($\lambda<350$ nm)=0. Light above 900 nm is transparent to the CdTe absorber and hence QE($\lambda>900$ nm)=0.

An estimate of J_{sc} can be determined by integrating the product of the QE curve, at short circuit conditions, with available current in the AM 1.5 spectrum (Eq. (2-14)).

$$J_{sc} \sim IQE = \int_{350\ nm}^{900\ nm} QE(\lambda, V = 0) f_{AM1.5}(\lambda) d\lambda \qquad (2\text{-}14)$$

where $f_{AM1.5}(\lambda)$ represents the maximum current density allowable from the AM1.5 spectrum at wavelength λ, and IQE represents the integrated quantum efficiency, hence in units of mA/cm^2.

The use of a quantum efficiency (QE) setup [49], [50] was utilized to measure the CdTe bandtail absorption to obtain properties of bandgap and Urbach energy [51], the latter quantity which is useful to characterize CdTe crystal disorder [52]. The use of quantum efficiency to determine CdTe bandgap E_g and Urbach energy E_U is determined from the relation

$$\ln\big(QE(E)\big) = \frac{(E - E_g)}{E_U} \qquad (2\text{-}15)$$

which holds if the photon energy $E<E_g$. Hence measurements were taken in the infrared region $\lambda>820$ nm where photons are insufficiently absorbed in CdTe. A derivation of Eq. (2-15) can be found in Appendix B.

2.3.2.1 Quantum Efficiency: Basic Operations and Equipment

The basics of obtaining a QE measurement are described as follows. Using a halogen bulb light source, a monochromator produces a chopped light beam with wavelength λ (full width half max=10-15 nm) and frequency f (~71 Hz) which then illuminates a cell. The cell is connected at a bias voltage V, producing an AC photocurrent. The AC photocurrent is then converted to an AC voltage using transimpedance and amplified using a lock in amplifier which is referenced to the light chopper frequency. Then the amplified signal is read by a computer. The above

procedure is repeated N types over a wavelength range from λ_{min} to a maximum wavelength λ_{max} where

$$\lambda_{max} > \frac{hc}{E_g} \tag{2-16}$$

with E_g as the absorber bandgap so that at λ_{max}, a negligible amount of light is absorbed by the cell and QE(λ_{max})=0. In addition, a white 90 mW/cm^2 DC bias light (constant intensity with regards to time) can be used to illuminate the CdTe device. The combined use of voltage and light bias is useful for characterizing light or voltage dependent recombination mechanisms [17]. Equipment for the measurement is shown in Figure 2-12.

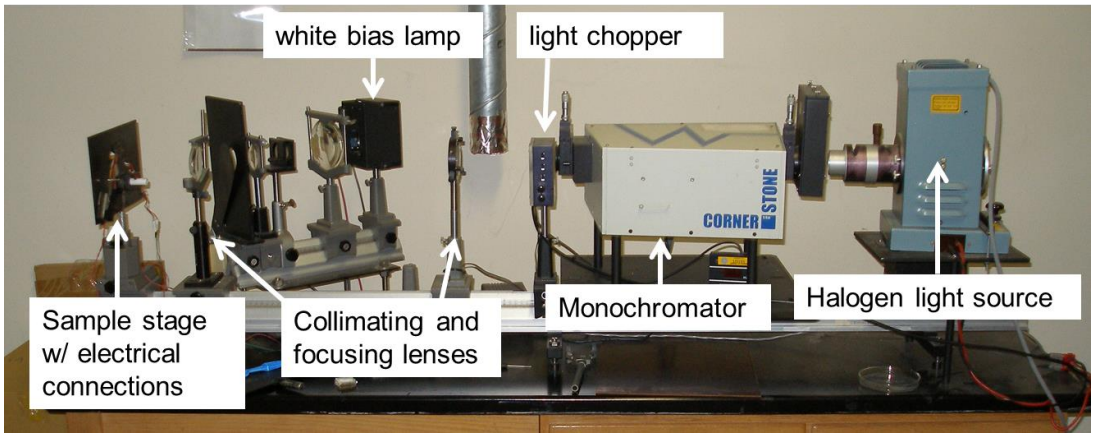


Figure 2-12: Optical equipment used for a QE measurement along with the sample stage. Not pictured is electrical equipment and computer used to convert the photocurrent to a voltage signal and resulting QE value [50].

Prior to QE measurements on a CdTe cell, a calibration with a silicon cell with a known AM 1.5 J_{sc} value is carried out from 350-1200 nm (E_g(Si)=1.1 eV). As long as the IQE obtained is within 1% of the reference IQE value for the cell which is based on an AM 1.5 J_{sc} measurement, then the light spectrum is correctly calibrated. However, spectral variations do occur over time due to aging of the halogen bulb or other systematic factors, which result in spectral variations greater than 1% of the reference IQE. Corrections then need to be performed on the CdTe QE after a QE measurement.

2.3.2.2 QE Measurement Procedure for CdTe Devices

Corrections performed on the raw CdTe QE data are performed as follows. For a raw QE value, the corrected QE is determined by

$$QE_{corr} = \frac{QE_{Si,ref}}{QE_{Si}} QE_{raw} \tag{2-17}$$

where $QE_{Si,ref}$ represents spectral response reference data for a Si calibration cell under AM 1.5 conditions and QE_{Si} represents the spectral response data taken using the Si calibration cell with the QE system halogen bulb and electronics.

For a general QE measurement, λ ranges from 350-400 nm in 10 nm steps and 400-900 nm in 20 nm steps. For a long wavelength QE measurement, λ ranges from 800-910 nm, typically in 10 nm steps. The monochromatic beam area which illuminates the CdTe cell is 4 mm^2 which is smaller than the area of the cell (36 mm^2) and hence the QE measurement is independent of beam size.

QE measurements on baseline CdTe cells are taken at 0V without white bias illumination and no difference in the QE(λ) response was observed with white light,

while previous J-V measurements on the cells showed maximum photocurrent at 0V (i.e. no voltage dependent photocurrent for V≤0 [19]).

2.3.3 J-V-T-I

This section discusses the experimental equipment, and procedure, used to obtain current-voltage-temperature-light intensity or JVTI data which was used to estimate diode recombination metrics activation energy E_A, and back barrier Φ_b.

Using the J-V model for an illuminated CdTe device with a primary CdS-CdTe pn junction, secondary light independent back contact junction, negligible shunt resistance (Figure 1-1, Eq. (1-1)), for J=0, an expression for V_{oc} is derived,

$$V_{oc} = -\frac{AkT}{q} ln \frac{J_0}{J_L(V_{oc})} \tag{2-18}$$

where the recombination current J_0 is given by [17], [53]

$$J_0 = J_{00} e^{\frac{-E_A}{AkT}} \tag{2-19}$$

and hence

$$V_{oc} = \frac{E_A}{q} - \frac{AkT}{q} ln \frac{J_{00}}{J_L(V_{oc})} \tag{2-20}$$

where J_{00} is a recombination current prefactor. If the approximation $J_L(V_{oc})$~J_{sc} is made, then V_{oc} is modeled as

$$V_{oc} = \frac{E_A}{q} - \frac{AkT}{q} ln \frac{J_{00}}{J_{sc}} \tag{2-21}$$

While in theory, the diode factor A could be calculated using Eq. (2-21) by varying light intensity, and determining A from a linear plot of V_{oc} vs ln(J_{sc}) at fixed temperature, the approximation $J_L(V_{oc})$~J_{sc} neglects voltage dependent collection

current, leading to questionable values of A using this method. Nevertheless, a linear relation with V_{oc} vs T can be observed for temperatures ranging from 220-300 ºK, allowing easy determination of E_A. To obtain values of activation E_A, measurements of V_{oc}, J_{sc}, and temperature were fit using Eq (2-21) over a temperature range of 220-300 ºK which was observed to be linear with regards to V_{oc} vs T with results given in Chapter 4 and Appendix A.

2.3.3.1 Light Measurements

For JVTI measurements, a temperature control chamber from Tenney Engineering Inc. is utilized as shown in Figure 2-13.

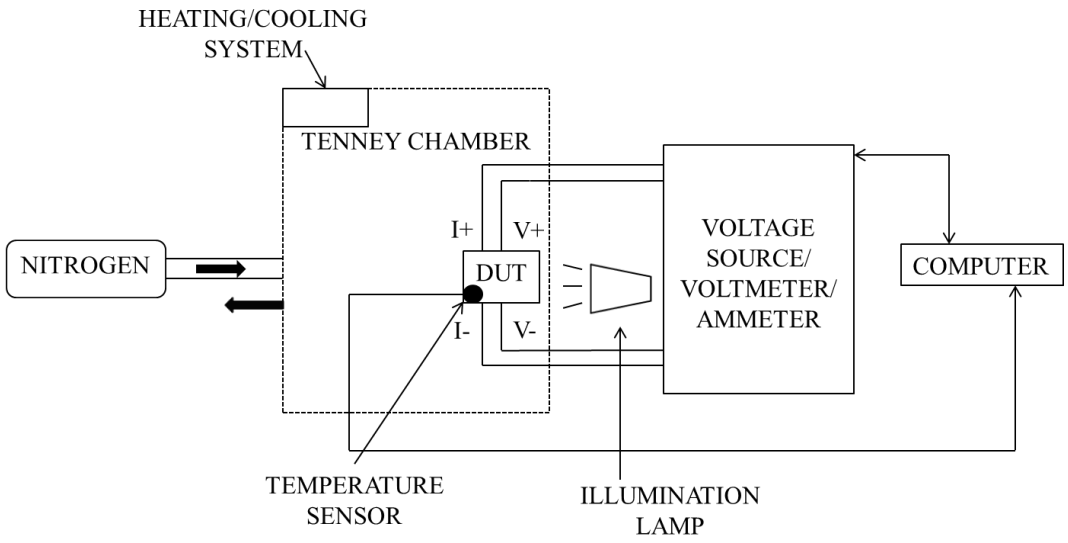


Figure 2-13: Schematic of the JVTI setup which is used to measure J-V characteristics of CdTe cells. A heating/cooling system controls the temperature of the chamber where heating is performed via resistive elements or cooling via refrigeration. The black dot represents a temperature sensor which is placed on the surface of the device. Thick arrows indicate nitrogen flow.

The chamber itself contains equipment to do a four point measurement of a sample. For a J-V measurement, a Keithley 2400 Source Meter is used to source voltage and read voltage and current values. The chamber can be heated using resistive elements or cooled down to 220ºK by the use of a refrigeration system. To cool down the chamber, the chamber is first purged with nitrogen to keep water vapor from freezing and damaging the sample. A resistance temperature detector (RTD) element is placed on the sample surface and acts as a temperature sensor. On the outside of the chamber are ELH bulbs which illuminate the sample through a window in the door of the chamber. Light intensity can be adjusted by the use of one or more mesh screens, placed in front of the bulbs which act as a neutral density filter.

Current voltage measurements were taken from reverse to forward bias using starting reverse bias voltages <-0.2 V, and ending forward bias voltages V(J~50 mA/cm^2)>0.8 V using voltage increments of 5-7 mV. The light intensity was adjusted to 1000 W/m^2 by: 1.) measuring J_{sc} on an illuminated CdTe device under short circuit conditions and; 2.) adjusting the light intensity to match J_{sc} to a previously determined value at STC.

JVTI measurements on CdTe samples were then carried out as follows: 1.) measuring V_{oc} at a fixed light intensity and temperature; 2.) then, varying the light intensity via the neutral density filters (intensity<1000 W/m^2) at the fixed temperature and remeasuring V_{oc}; 3.) then, lowering the temperature to a specified value and repeating the V_{oc}, measurements at different light intensities. Temperature was varied between 220-300 ºK using temperature increments of 6-15 ºK. Samples were measured using light intensities of 140, 240, 490, and 1000 W/m^2.

Measurements of V_{oc} at 300 ° K, and 1000 W/m^2, illuminated using the ELH bulb intensity referred to as standard ELH or SELH conditions. Measurement results of V_{oc} at SELH conditions for the diode metrics are included in Section 4.4.3.

2.3.3.2 Dark Measurements

Dark JV-T measurements were taken to measure the CdTe back barrier, Φ_b. Dark JV-T measurements were taken either using the previously described Tenney chamber setup (Figure 2-13) or a Linkam cryostat. For the Linkam cryostat, the sample was placed on a mounting plate. The temperature of the sample was controlled, either by heating elements underneath the plate or a liquid nitrogen (LN_2) pump/dewar-system for cooling the sample chamber, and both heating/cooling elements were interfaced to a temperature controller. The temperature controller regulated the power to the heating plate and the nitrogen flow of the pump by receiving instructions from a computer, while the controller relayed temperature information back to the computer. By interfacing the computer to a Keithley 2400 Source Meter, current voltage measurements were performed across the device. A schematic of the cryostat system is shown in Figure 2-14.

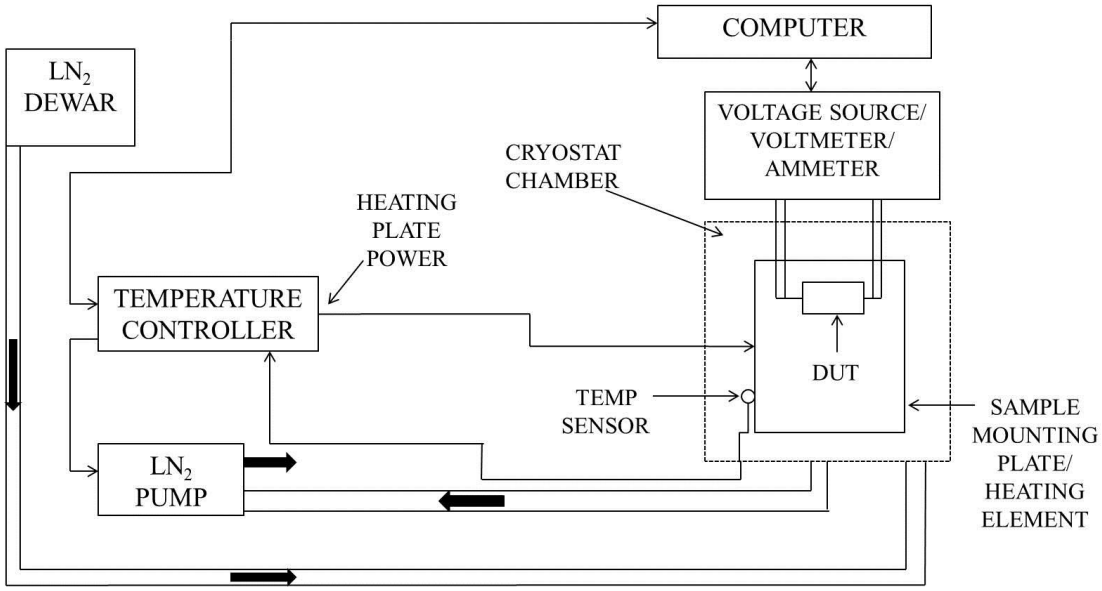


Figure 2-14: Schematic of a setup used for dark JV-T measurements which utilizes a cryostat. Thick arrows indicate nitrogen flow.

The use of dark JV-T measurements are utilized to measure the back contact barrier of a CdTe cell. For CdTe devices with a Cu_2Te back contact, devices were measured with in the Tenney chamber over a temperature range 220-300 ºK using temperature increments of 6-9 ºK. An upper temperature limit of 300 ºK was used to keep Cu from migrating from the back contact into the CdTe bulk/interface layers which can degrade device performance.

However for CdTe devices with a Cu free PCBM contact, this was less crucial and cells were measured in the cryostat setup using a higher temperature range of T=363-393 ºK was with temperature increments of 10 ºK.

2.3.4 CV and DLCP

This section describes the theory of capacitance-voltage (CV) profiling and drive level capacitance profiling (DLCP) which were used to estimate CdTe space charge width and bulk CdTe doping.

2.3.4.1 CV Theory

Consider a single diode model of a p-n junction device under a voltage bias V with a uniform charge density in the p-n depletion region, and neutral bulk region (Figure 2-15).

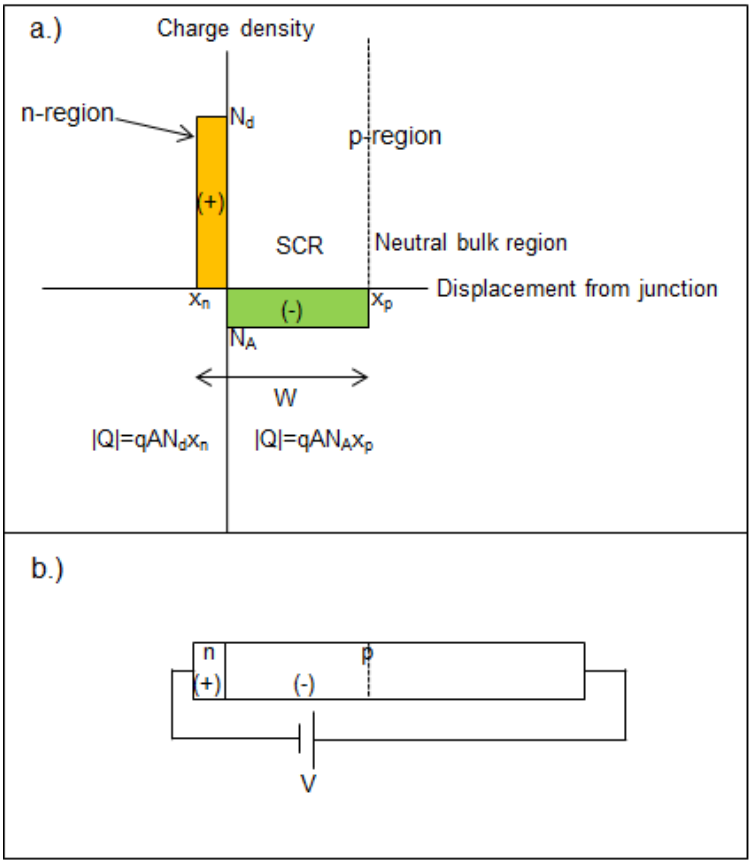


Figure 2-15: a.) Charge density and electric field at a voltage bias V for a single diode p-n junction device with uniform charge density resulting in a space charge region (SCR) of width W and neutral bulk region. b.) The p-n junction subjected to a voltage bias V.

For the p-n junction subjected to an applied voltage bias V, the charge Q which forms on each side can be written as

$$Q = qAN_d x_n = qAN_a x_p \tag{2-22}$$

or

$$N_d x_n = N_a x_p \tag{2-23}$$

where q is the elementary unit charge, A is the cross sectional area, N_d and N_a are the respective donor, and acceptor carrier concentration, and x_n and x_p are the respective depletion lengths on the n and p sides of the junction. The junction width W can be written as

$$W = x_p - x_n \tag{2-24}$$

If the donor density $N_d >> N_a$ as is the case for CdS/CdTe superstrate devices with $t_{CdS} << W$, then from Eqs. (2-23) and (2-24), $x_n << x_d$ and hence $x_p \sim W$ and

$$Q = qAN_aW \tag{2-25}$$

The capacitance of the p-n junction can be written as

$$\frac{dQ}{dV} = C \tag{2-26}$$

By using Poisson's equation to relate the charge density ρ to the potential Φ(x) of the junction,

$$\frac{d^2(\Phi(x))}{dx^2} = -\frac{\rho}{\varepsilon} \tag{2-27}$$

with ρ = 0 in the neutral bulk region, $\rho = 2qN_d$ for the n-type depletion region, and $\rho = -2qN_a$ for the p-type depletion region. The potential across the p-n junction is

$$\Phi(\infty) - \Phi(-\infty) = V - V_0 \tag{2-28}$$

with x=∞ and x=-∞ respectively representing the far right (p+) and left (n-) sides of the junction, and where V_0 and V are respectively the built in voltage and applied voltage across the p-n junction. It can be shown [54] that the relation between the depletion width to the potential and applied voltage V is represented as

$$W = \sqrt{\frac{2\varepsilon(V_0 - V)}{qN_a}} \tag{2-29}$$

Then, using Eqs. (2-25)-(2-29) the capacitance C can be written as

$$C = \varepsilon A \sqrt{\frac{qN_a}{2\varepsilon(V_0 - V)}} \tag{2-30}$$

By using Eq. (2-29) for W,

$$C = \frac{\varepsilon A}{W(V)} \tag{2-31}$$

An equation for N_a can be written in terms of applied bias V and capacitance C as follows. First, via the use of Eq. (2-30) with

$$(\frac{A}{C})^2 = \frac{2(V_0 - V)}{\varepsilon N_a} \tag{2-32}$$

which implies,

$$\frac{d}{dV}(\frac{1}{C})^2 = \frac{-2}{\varepsilon N_a} \tag{2-33}$$

By using Eqs (2-32) and (2-33) with N_a=N_{CV}

$$N_{CV}(V) = \frac{-2}{q\varepsilon A^2}\left[\frac{d\left(\frac{1}{C^2}\right)}{dV}\right]^{-1} \tag{2-34}$$

The above equations for space charge width and doping (Eqs (2-31) and (2-34)) assume that charge density only varies at the depletion edge, and that the depletion edge dominates the response of capacitance with voltage. However, deep

defect levels within the CdTe bulk or at the interface can also affect capacitance and these also need to be considered for a capacitance measurement.

2.3.4.2 DLCP Theory

When there is a significant density of defects in the depletion region, an applied AC bias results in an additional capacitance response. This is illustrated for a single defect (Figure 2-16).

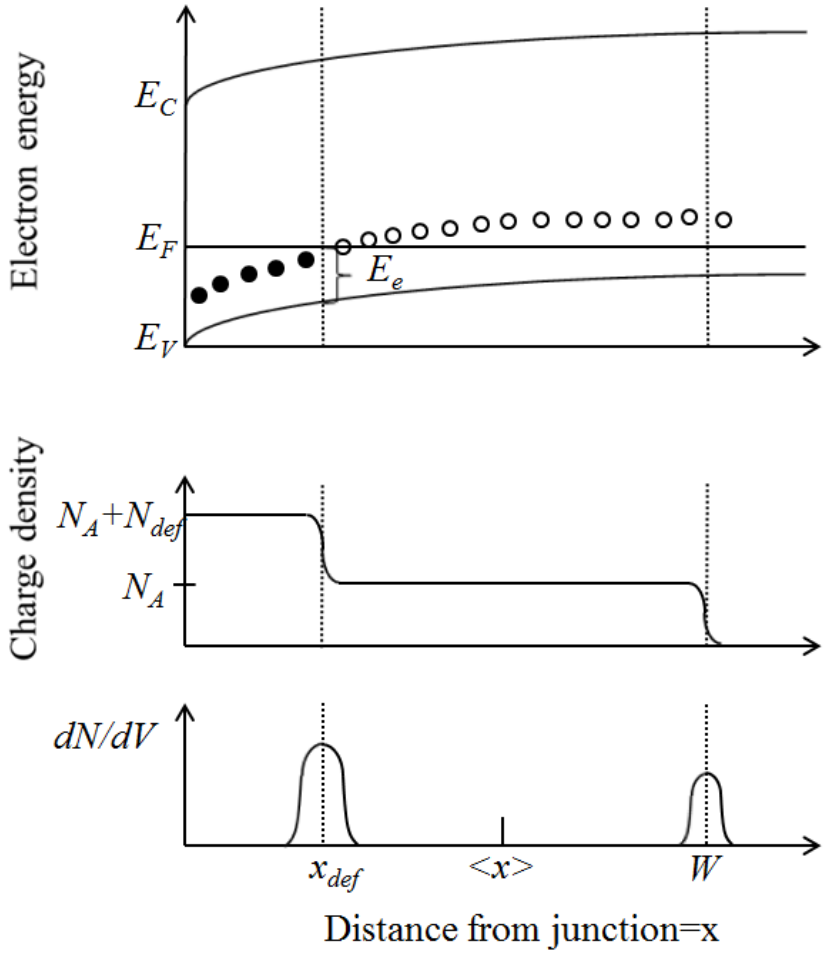


Figure 2-16: Response of a device with a single defect under at a fixed frequency f and temperature T resulting in a defect response demarcation energy E_e. The band bending is influenced by the applied DC and AC bias V_{AC}. This is shown for the p-side of an n^+-p junction. Adapted from Heath, Cohen, and Shafarman, [55].

Here, N_A and N_{def} represent the dopant and defect density respectively while x_{def} represents the position of the defect, and <x> is the first moment of charge response, given as

$$< x >= \frac{\int_0^\infty x\delta\rho(x)dx}{\int_0^\infty \delta\rho(x)dx} \quad (2\text{-}35)$$

where δρ(x) is the variation of charge density due to the applied AC signal [55]. For the case of a single discrete defect, located at a distance x_d from the interface,

$$< x >= \frac{N_{def}x_{def} + N_A W}{x_{def} + W} \quad (2\text{-}36)$$

As a result, the capacitance response becomes,

$$C = \frac{\varepsilon A}{< x >} \quad (2\text{-}37)$$

where for CdTe, $\varepsilon = 10^{-12}$ F/cm.

For the free carrier density to originate only from the depletion edge, the free carrier relaxation time τ needs to be small enough compared to the applied AC frequency f so that $\tau \leq 1/f$ [56] [55]. Hence, in order to obtain the best accuracy of space charge width W, (minimal value of $|<x>-W|$), and doping, the highest frequency f should be chosen to minimize the effect of defect states on the measurements. Furthermore, the response of the defect also depends on temperature T. The energy E_e in Figure 2-16 is the demarcation energy and conceptually represents the energy where the occupation of the defect state can change so that $\tau \sim 1/f$.

$$E_e = -kTln(\frac{f}{\nu_0 T^2}) \quad (2\text{-}38)$$

The quantity $\nu_0 T^2$ is called the thermal emission prefactor and is equal to

$$\nu_0 T^2 = N_\nu(\mathrm{T}) < \mathrm{v}_p > \sigma_h \quad (2\text{-}39)$$

where $N_v(T)$ is the effective valence density of states, $\langle v_p \rangle$ is the hole thermal velocity, and σ_h is the capture cross section of the hole defect state [55]. For $\langle v_p \rangle = 10^7$ cm/s, $\sigma_h = 10^{-15}$ cm^{-2}, and $N_V = 10^{19}$ cm^{-3} [57] T=300 ºK, and f=1 MHz, a demarcation energy E_e=0.3 eV, equivalent to the CdTe Fermi level (based on Boltzmann statistics with $N_V = 10^{19}$ cm^{-3} and a hole doping of 10^{14} cm^{-3} [18]).

The ionized gap state energy includes those states that can be measured by the demarcation energy E_e, which can include both free carrier and defect states. For a p-type semiconductor, the measured defect density N_{meas} can be written as [55]

$$N_{meas} = p + \int_{E_F^{\infty}}^{E_e+E_v} g(E, x_e) dE \tag{2-40}$$

where p is the free carrier density, E_F^{∞} is the value of the Fermi energy in the bulk (far away from band bending), and $g(E,x_e)$ represents the density of states at the spatial location x_e. Hence, N_{meas} includes both shallow acceptors and deeper defects up to the demarcation energy E_e.

Increasing frequency f results in a decrease of demarcation energy E_e (Eq. (2-38)) resulting in a lower defect response (decreased $\delta\rho(x)$, (Eq. (2-35)) and resulting increase of $\langle x \rangle$ (Eqs. (2-35)). If frequency f were to increase to a limiting value f_0, so that $E_e(f_0) \sim 0.2$ eV (free carrier V_{Cd} and Cu_{Cd} defect energies [18]) , then $\langle x \rangle \rightarrow W$. In reality, $\langle x \rangle$ will be less than W since the experimental equipment utilized for capacitance measurements generates a maximum AC frequency of 1 MHz $< f_0$.

In drive-level capacitance profiling (DLCP), for an applied voltage V across a device, the AC voltage amplitude δV= peak-to-peak voltage =V_{pp} varies in addition to the DC voltage V_{DC} such that

$$V = \frac{1}{2} * V_{pp} + V_{DC} = constant \tag{2-41}$$

and hence

$$\frac{\delta Q}{\delta V} = C \approx C_0 + C_1 \delta V + C_2 (\delta V)^2 \tag{2-42}$$

$$= C_0 + C_1 V_{pp} + C_2 \left(V_{pp}\right)^2$$

This is further illustrated in Figure 2-17.

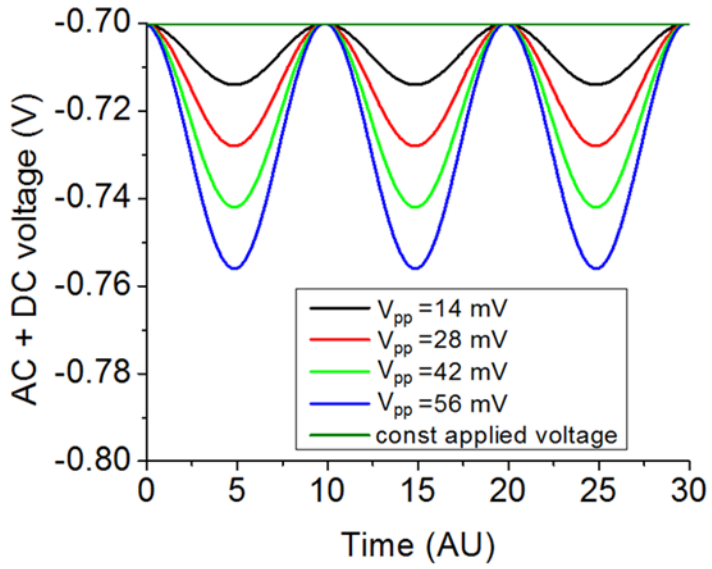


Figure 2-17: For a DLCP measurement, the peak-to-peak AC voltage and applied DC bias are changed in such a way that the applied voltage V is constant. The individual curves represent the AC signal increasing during a DLCP measurement (V_{pp} increases), while the DC signal decreases in such a way that the applied voltage is constant.

For a DLCP measurement, the value of the measured defect density N_{meas} (Eq.(2-40)) is given the notation N_{DL}. Given the above constraints on δV, it can be shown that the measured defect density is equal to the following [55] [58].

$$N_{DL} = \frac{-C_0^3}{2q\varepsilon A^2 C_1} \tag{2-43}$$

2.3.4.3 CV and DLCP Measurements

The experimental setup used to take capacitance measurements is shown in Figure 2-18.

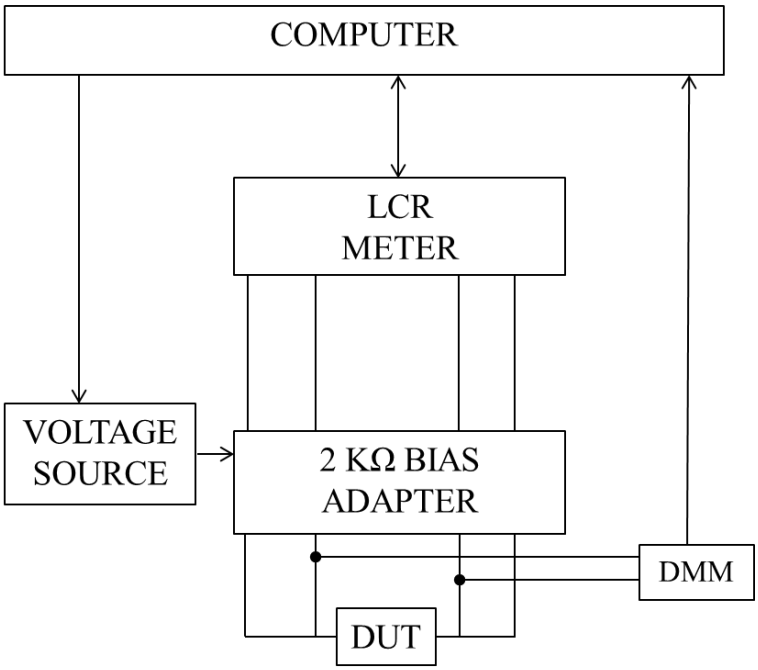


Figure 2-18: A schematic diagram of the C-V system used to take measurements at 300ºK. Key: DUT=device under test, DMM=digital multimeter, LCR meter =inductance, capacitance, resistance meter. The LCR meter generates an AC voltage and measures a resulting capacitance [59]. The equipment for the measurements are described in greater detail in references [60] and [50].

Functions of the computer are to write DC voltage values to a voltage source , read impedance information from the LCR meter (Agilent Technologies model 4284A), read and write frequency and peak-to-peak voltage from the LCR meter, and read DC bias information from the DMM. The LCR meter uses an AC voltage with frequency f to measure the complex impedance Z of the device [59] and subsequently determine the capacitance from Z by assuming a model of a CdTe device with a resistance R and capacitance C in parallel [61] where,

$$\frac{1}{Z} = R + j(2\pi f C) \tag{2-44}$$

The LCR meter generates a maximum generated AC frequency of 1 MHz, and is protected from excessive voltage and current by a 2 kΩ bias adapter in series with the device. However, the bias adapter also limits the current across the CdTe device such that the CdTe device impedance>2 kΩ, and hence limiting the maximum forward bias voltage across the device to 0.5 V.

CV measurements were taken at T=300 ºK and f=1MHz using a DC voltage sweep from -1V to 0.5V and voltage increment of 0.1V. The AC voltage was fixed at 25mV.

DLCP measurements were also taken at T=300 ºK and f=1MHz. For each applied bias voltage V, the peak-to-peak AC voltage V_{pp} was swept from 14 mV to 280 mV in 27 mV increments, resulting in 10 AC measurements per applied voltage. The applied bias voltage was swept from -1V to 0.5V with increments of 0.15V, resulting in 10 applied voltage measurements per DLCP run. Therefore a total of 10x10=100 measurement pairs of AC and applied voltage were taken per DLCP run.

To estimate doping using DLCP, the minimum value of $N_{DL}(V)$ was taken over the range of applied voltage. $N_{DL}(V)$ was determined using Eq. (2-43)) by solving for C_0 and C_1 at a fixed applied voltage V and variable AC sweep. To solve for C_0 and C_1, a 2nd order polynomial fit was performed using Eq.(2-42) over the range of V_{pp} values to solve for C_0, and C_1 so that the fit has an adjusted coefficient of regression R_{sq} of 0.98 or greater, excluding C-V_{pp} data with a resultant fit R_{sq}<0.98. From the calculated value of C_0, the space charge width is estimated as the moment of charge response, <x>, when f → f_0, where <x> is given by

$$< x >= \frac{\varepsilon A}{C_0} \tag{2-45}$$

with $\varepsilon = 10^{-12}$ F/cm as previously stated.

Chapter 3

CDTE DEVICE SIMULATION

3.1 Introduction

In this chapter, a 1-D numerical simulation of an idealized CdTe device is introduced as a means to qualitatively predict V_{oc} as a function of thickness using the SCAPS software 3.0.01. The SCAPS software has been used for a simulation of a front-contact/CTO/ZTO/CdS/CdTe/back-contact superstrate structure. This model will be used to compare an experimental relation of V_{oc} vs CdTe thickness in Chapter 5.

3.2 Device Modeling Software

This section discusses the types of software which can be used to model CdTe solar cells, the specifics of the SCAPS software, and results of CdTe solar cell simulations using SCAPS.

3.2.1 Available Software for Modeling

Listed below are several common available software packages which are used to simulate the operation of solar devices. Software packages involve the user inputting material parameters as well as AM1.5 operating conditions. Device physics is modeled using Poisson's equation and continuity equations for electrons and holes, typically by the use of discrete mathematics where the cell length is divided into N

intervals (1D simulation) or through the use of a spatial mesh (2 or 3D simulations). The resulting output includes simulated JV curves and hence device performance.

3.2.1.1 ADEPT

The software "A Device Emulation Program and Toolbox" or ADEPT was developed at Purdue University by J. Gray [62]. The software allows for simulation for either 1D, 2D, or 3D spatial dimensions by solving the semiconductor equations on a discrete spatial mesh. This software has been previously utilized to model CdTe device performance by simulating 2D CdTe grains [63]. However, in the past 20 years, published literature on ADEPT CdTe simulations has been scarce if available, and a more commonly used 2D or 3D CdTe device simulation program is Sentaurus.

3.2.1.2 Sentaurus

Sentaurus is a software package developed by the Synopsys$^{(R)}$ company allowing for the simulation of electronic devices in 1, 2, or 3 dimensions [64] and is widely used for the simulation of solar devices. Sentaurus has been used to simulate photoluminescence of CdTe devices and compare with experiment in order to estimate the relations between V_{oc} vs CdTe lifetime and surface recombination velocity [65], and to quantify the CdTe recombination mechanisms [66]. Sentaurus is also useful for analyzing next generation 3D CdTe structure devices such as CdTe nanopillar devices [67].

3.2.1.3 NSSP

The "Numerical Solar Cell Simulation Program" or NSSP is a 1D simulation program which uses a lifetime model for bulk layers and interfaces as well as the specification of surface recombination velocity [68], [69]. This program was utilized

by N. Amin et al. ([68], [69]) to simulate CdS/CdTe device performance vs thickness for a non-ohmic back contact, the results of which imply a V_{oc} CdTe thickness dependence for $t_{CdTe}<2$ μm consistent with the theoretical (SCAPS) and experimental findings of the author (Chapter 5). Aside from a surface recombination velocity of 10^8 cm/s at the back interface, no additional information on the back contact is given and aside from these studies, it is not apparent that other published literature on this simulation program is available.

3.2.1.4 WxAMPS

WxAMPS is a 1D solar cell simulator program created by A. Rockett and Y. Liu at the University of Illinois at Urbana-Champaign [70]. It is based off the program AMPS-1D which was created by Fonash et al [71] at Pennsylvania State University through the support of the Electric Power Research Institute, but is superior to the former program in terms of computational speed and the incorporation of tunneling phenomenon. However, for a given set of input, calculated JV curves and hence device performance is identical to SCAPS simulations both for CIGS [70] and CdTe.

3.2.1.5 SCAPS

A numerical device simulation program, SCAPS 3.0.01 is applied to CdTe devices. SCAPS is a 1-D solar cell program developed by M. Burgelman at the Department of Electronics and Information Systems at the University of Gent, Belgium. This program is designed to model polycrystalline devices such as CIGS and CdTe.

SCAPS works by solving Poisson's equation and the continuity equations for electrons and holes by 1.) subdividing the total cell length L into N intervals, not necessarily of equal length, and solving for 3N equations through the use of iterative solution techniques. For precise calculations, N>200. Solution methods are described in greater detail in references, [72], [73], and [74]. The user inputs information regarding material layers and properties, and defects, material absorption coefficients $\alpha(\lambda)$, front and back contact barrier properties, choice of illumination spectrum, temperature, and a simulated voltage sweep.

The action panel user interface which is used to set input values and execute output simulations is shown in Figure 3-1.

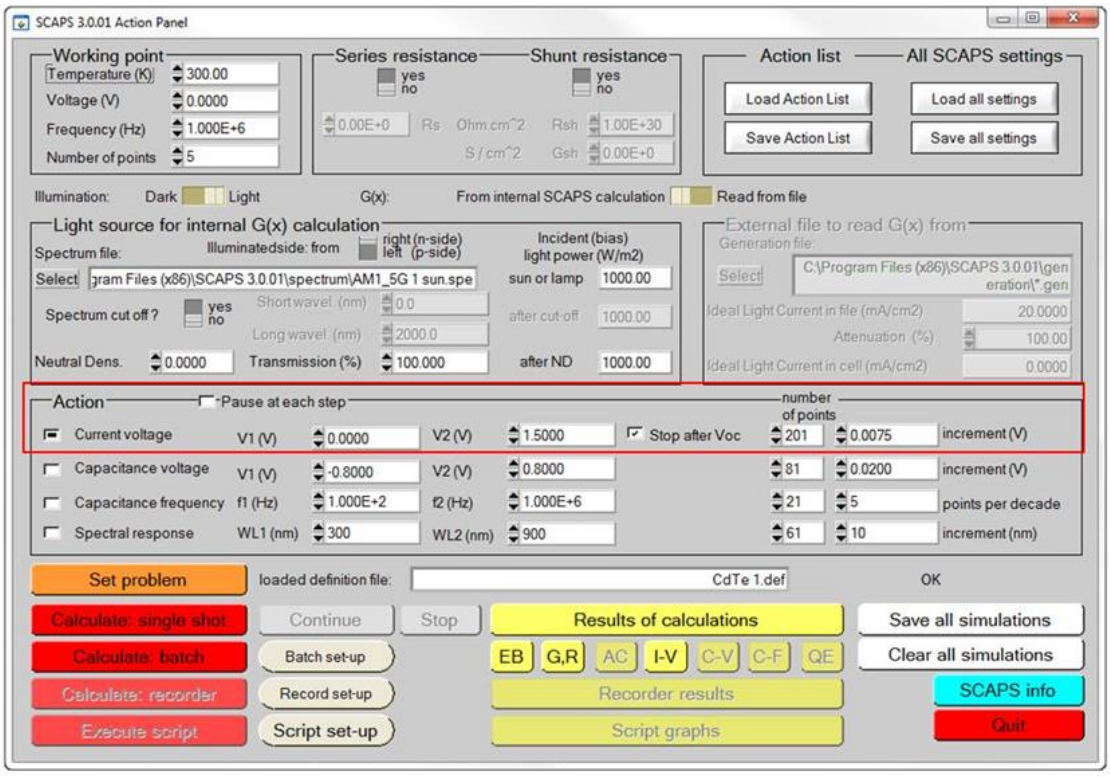


Figure 3-1: SCAPS action panel graphical user interface used to execute output current voltage simulations (boxed in red). The capacitance voltage, capacitance frequency and spectral response output calculations are not relevant for this work.

To input layer and defect properties for the device structure, this is done through the "Set problem" icon (Figure 3-1, lower left corner). The input layer interface is shown in Figure 3-2.

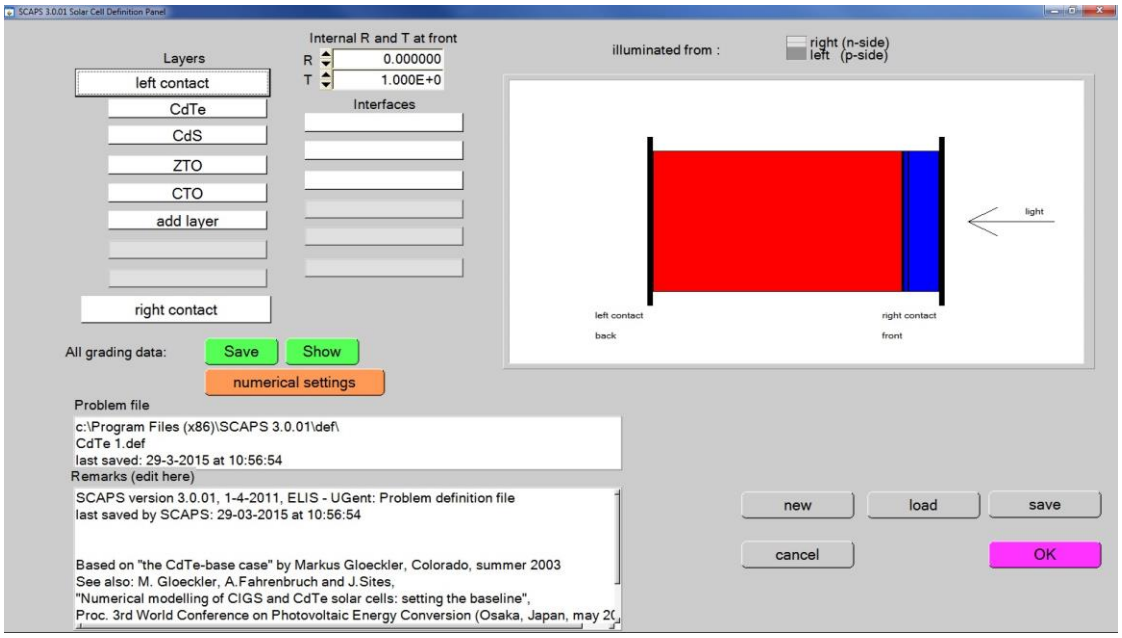


Figure 3-2: Input layer graphical user interface.

By clicking on the layer, contact, and interface boxes, material and defect properties can be input, (Figures 3-3, 3-4, and 3-5).

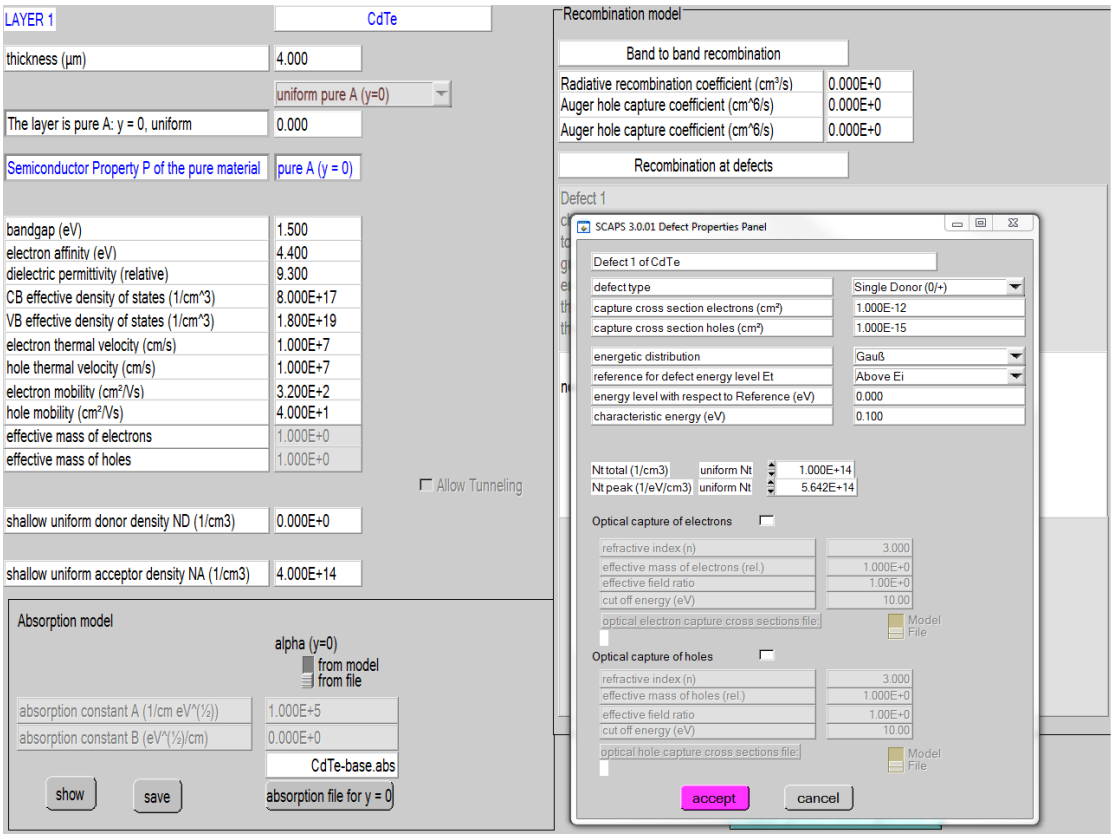


Figure 3-3: Layer properties graphical user interface.

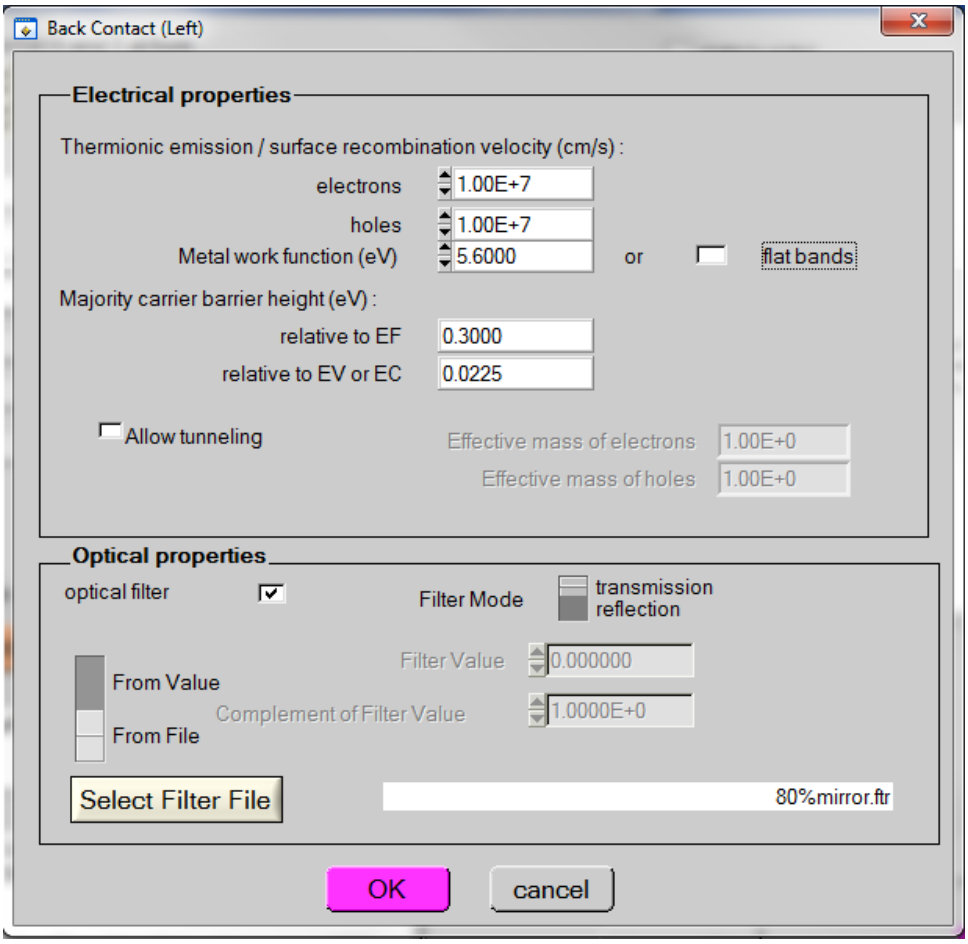


Figure 3-4: Contact properties graphical user interface.

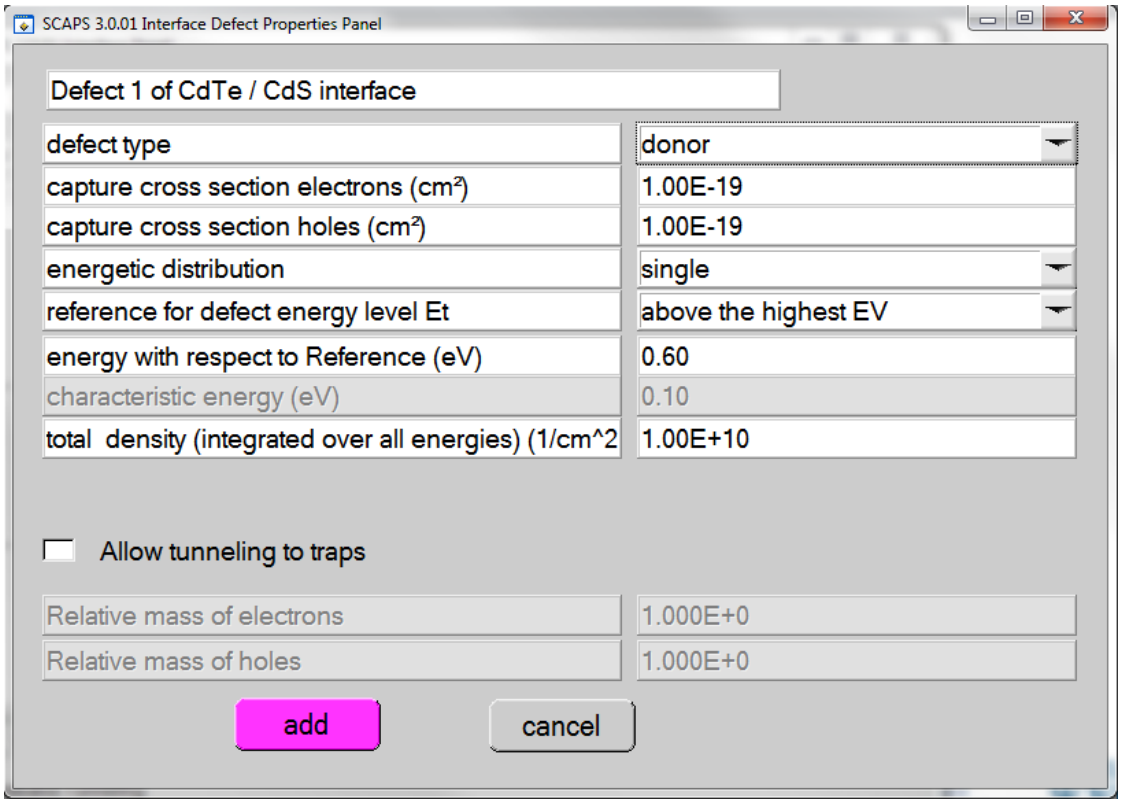


Figure 3-5: Interface properties graphical user interface

From the action panel (Figure 3-1), only the current voltage simulations were used for this work. Current voltage simulations using a simulated current voltage (J-V) sweep can be performed under dark conditions or AM 1.5 conditions, the latter which can be used to obtain simulated device performance.

Spatial properties of the energy bands can also be simulated using SCAPS. Of relevance are simulated band diagrams as shown in Figure 3-6.

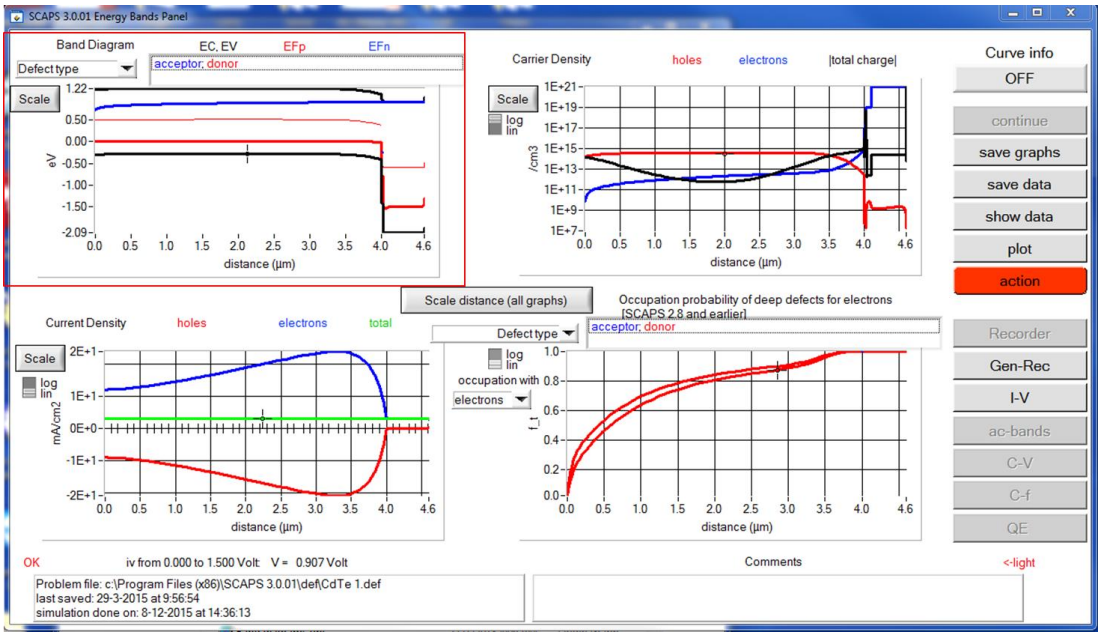


Figure 3-6: Spatial profiles of energy bands (boxed in red). The spatial profiles of carrier density, current density and occupation probability of electron deep defects are not relevant for this work.

SCAPS can run batch calculations from the action panel (Figure 3-1) which are used to calculate a series of input values and obtain resulting device performance metrics for each value without the repetitive use of manually inputting and calculating each value. Batch calculations were used to obtain V_{oc} vs CdTe thickness profiles as discussed in Chapter 5. The user interface for batch calculations is shown in Figure 3-7.

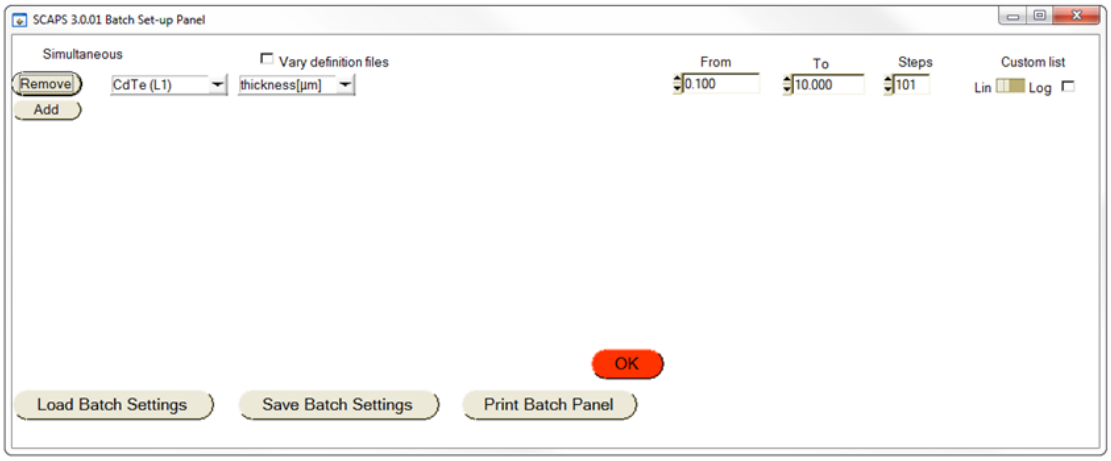


Figure 3-7: Batch calculation user interface shown for making 101 inputs of CdTe thickness from 0.1 µm to 10 µm which can be used to calculate V_{oc} as function of CdTe thickness (Chapter 5).

3.2.2 Why SCAPS

SCAPS is a user-friendly program which has the advantage of running batch calculations for rapid computation of simulated device performance and characteristics. However, the SCAPS model makes several simplifying assumptions for a CdTe cell. The model assumes: 1.) that the physics of carrier transport, generation, and recombination can be modeled one dimensionally; and 2.) the defect properties of the cell for layers or interfaces respectively correspond to an electronic volume or area). In reality, the CdTe layer consists of polycrystalline grain boundaries which may consist of structural bulk and surface defects which may only be adequately explained using a 2D or 3D transport/generation/recombination model. As will be discussed (Sections 3.2.4, 3.2.5), there is a 30-60 mV V_{oc} discrepancy between theory and experiment for simulation of Cu_2Te devices, and even higher (100-200 mV) for CdTe thickness profiling measurements (Chapter 5). However, for

the purposes of this work it is of greater relevance to evaluate the theoretical vs experimental change in V_{oc} vs CdTe thickness and this is discussed in Chapter 5.

3.2.3 Input Parameters of Constituent Layers

In order to model CdTe devices with V_{oc}>800 mV a baseline case for input parameters is used. The starting point for the device input was based on the assumptions of Gloeckler et al who used, a cell structure front_contact/SnO_2/CdS/CdTe/back_contact with light entering the front contact [57]. The device input was then modified to match baseline CdTe devices made at IEC, by replacing the SnO_2 model used by Gloeckler by a Cadmium stannate and Zinc stannate (CTO and ZTO) model, where device input parameters for CTO and ZTO were chosen as follows: 1.) based on thickness and optical measurements taken at IEC; 2.) external literature sources if measurements were not available; or 3.) assumed default to the Gloeckler baseline if literature sources were not known. Similarly, input for the CdS, and CdTe model, and front/back contact model were chosen based on IEC measurements, or assumed default to the Gloeckler baseline. Hence, the device model is not a perfect match to experimental baseline CdTe devices but instead an attempt to match the modeled input with baseline material properties.

The baseline case for the cell is shown in Table 3-1

Table 3-1: CdTe baseline case for simulations, modified for a FC/CTO/ZTO/CdS/CdTe/BC device.

General Device Properties				
	Front contact		Back contact	
Work function (eV)	4.6 [57]		5.9 (assumes no back barrier)	
Surface recombination electrons (cm/s)	10^7 (SCAPS default)		10^7 (SCAPS default)	
Surface recombination holes (cm/s)	10^7 (SCAPS default)		10^7 (SCAPS default)	
Reflectivity	0.065 [IEC internal]		0.8 [57]	
Layer Properties				
	CTO	ZTO	CdS	CdTe
Width (nm)	500 [IEC internal]	75 [IEC internal]	25 [57]	4000 [57]
Dielectric constant	4 [IEC internal]	4 [IEC internal]	6.1 [IEC internal]	9.3 [IEC internal]
Electron mobility $cm^2/(Vs)$	60 [75]	13 [76]	100 [57]	320 [57]
Hole mobility $cm^2/(Vs)$	25 [57]	2 [77]	25 [57]	40 [57]
shallow donor/shallow acceptor free carrier density N_D/N_A (cm^{-3})	$N_D=9.9*10^{20}$ [75]	$N_D=9.9*10^{18}$ [78]	$N_D=1.1*10^{18}$ [57]	$N_A=1-4*10^{14}$ (DLCP)
Bandgap (eV)	3.0 [IEC internal]	3.0 [IEC internal]	2.4 [57]	1.5 [57]
thermal velocity v_{th} (cm/s)	10^7			
Electron density of states N_c (cm^{-3})	10^{21} (based off free carrier density)	10^{19} (based off free carrier density)	$2.2*10^{18}$ [57]	$8*10^{17}$ [57]
Hole density of states N_v (cm^{-3})	$1.8*10^{19}$ [57]	$1.8*10^{19}$ [57]	$1.8*10^{19}$ [57]	$1.8*10^{19}$ [57]
Electron affinity (eV)	4.5 [57]	4.5 [57]	4.5 [57]	4.4 [24], [25], [79]

Table 3-1: continued

Defect Properties			
	CTO	ZTO	CdS
Type-	Gaussian donor	Gaussian donor	Gaussian acceptor
Density (cm^{-3})	10^{19} (1% of free carrier density)	10^{17} (1% of free carrier density)	10^{18}
Energy level relative to conduction band (E_c-E_T) (eV)	1.5 [57]	1.5 [57]	1.2 [57]
Energy width (eV)	0.1 [57]	0.1 [57]	0.1 [57]
Electron carrier cross section (cm^2)	10^{-12} [57]	10^{-12} [57]	10^{-17} [57]
Hole carrier cross section (cm^2)	10^{-15} [57]	10^{-15} [57]	10^{-12} [57]
Absorption Properties	IEC internal		[80]
Temperature- 300 K			

A constraint on the input is the relation between CdTe defect density N_{DD} and CdTe acceptor concentration N_A.

$$N_{DD} = \beta N_A \qquad (3\text{-}1)$$

In CdTe devices, the density of deep donors can be on the same order of magnitude as acceptors due to the formation of deep defects which may occur when doping CdTe p-type [23]. However, attempts to set $N_{DD} \geq N_A$ ($\beta \geq 1$) in SCAPS result in a completely depleted CdTe layer, which is inconsistent with measurements of the potential across

the CdTe device cross section for thin film CdTe devices [27]. A depleted CdTe layer is observed in the simulated band diagrams as the simulated CdTe layer becomes intrinsic with equal p and n type defects (β=1) or n-type with a greater donor defect density (β>1). The dimensionless parameter β is chosen to range from 0.25-0.5. A shallow acceptor density of 1-4*10^{14} cm^{-3} is based off of DLCP measurements on CdTe devices with V_{oc}=800-840 mV, and using the value of β implies N_{DD}=2.5*10^{13}-2*10^{14} cm^{-3} for CdTe.

The CdTe minority carrier lifetime τ is calculated by assuming that

$$\tau = \frac{1}{\sigma_e v_{th} N_{DD}} \tag{3-2}$$

where σ_e is the electron capture cross section, v_{th} = 10^7 cm/s is the electron thermal velocity, and N_{DD} is the midgap donor defect (trap) density. A CdTe lifetime of 1 ns, which is observed in polycrystalline CdTe devices with V_{oc}=820 mV [13], [81] is used with Eq. (3-2). to obtain σ_e= 5*10^{-13}-4*10^{-12} cm^2.

The back contact work function of 5.9 eV is calculated assuming an ohmic contact using a calculated CdTe valence band of 5.9 eV based on a 1.5 eV work function and 4.4 eV electron affinity based on CdTe electron affinity ranging from 4.3-4.5 eV [24], [25], [79].

3.2.4 Simulated Band Diagrams and Associated V_{oc} Performance vs CdTe Thickness and Back Barrier

This section examines the simulation effect of CdTe thickness and back contact on V_{oc} by assessment of generated band diagrams.

Based on Table 3-1, SCAPS simulated equilibrium and V_{oc} band diagrams, the values of V_{oc} are shown for four cases based on CdTe thickness and back contact (Figures 3-8 and 3-9).

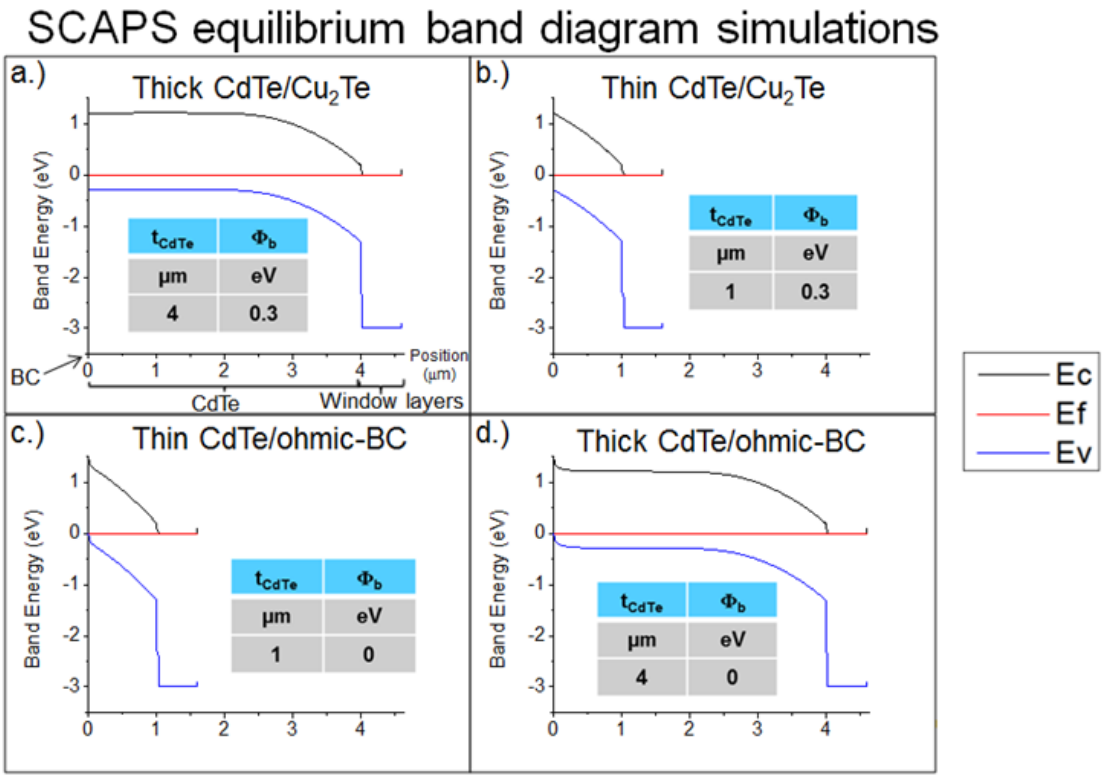


Figure 3-8: SCAPS equilibrium band diagram simulations for variations in CdTe thickness, back contact using the baseline case in Table 3-1 with CdTe shallow acceptor doping $N_A=4*10^{14}$ cm^{-3} and CdTe bulk lifetime of 1 ns.

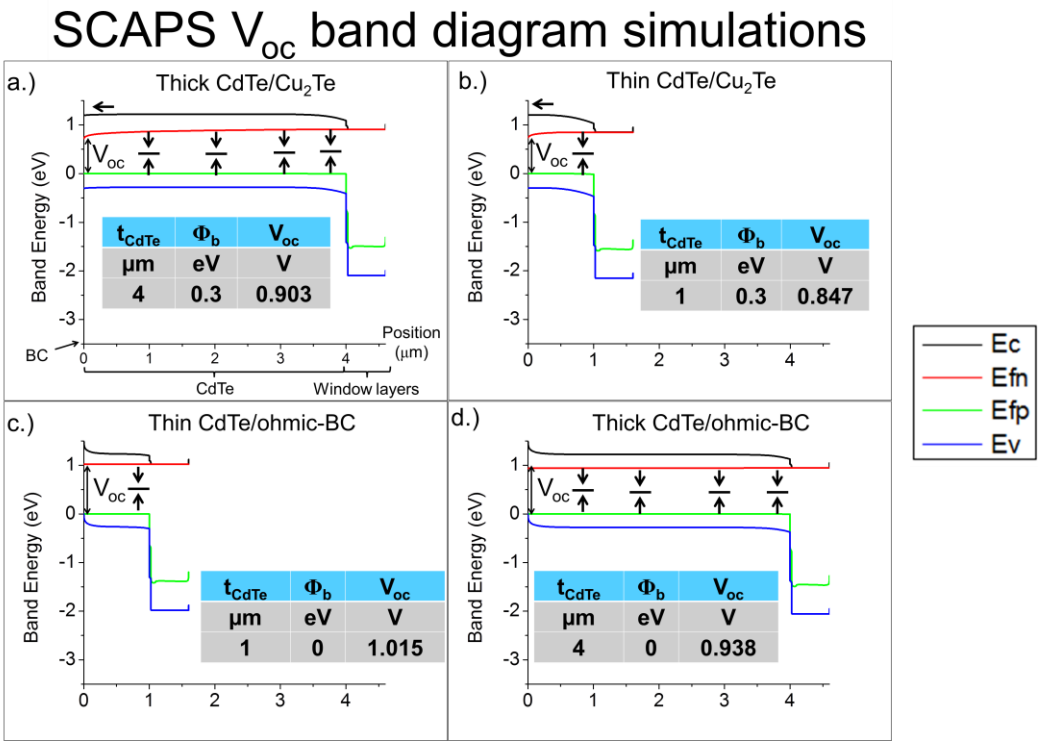


Figure 3-9: SCAPS V_{oc} band diagram simulations for variations in CdTe thickness, back contact using the baseline case in Table 3-1 with CdTe shallow acceptor doping $N_A=4*10^{14}$ cm^{-3} and CdTe bulk lifetime of 1 ns. The red/green curves respectively represent the electron/hole quasi-Fermi levels. Arrows indicate recombination mechanisms.

Case a. (Figures 3-8 a. and 3-9 a.), represents a baseline CdTe device with thickness 4 μm and a 0.3 eV Cu_2Te contact. A change in V_{oc} is observed with regards to thickness and contact. Case b. (Figures 3-8 b. and 3-9 b.), represents a thinner 1 μm device with a 0.3 eV Cu_2Te contact. While a thin 1 μm CdTe device has a smaller bulk CdTe recombination volume (reduced SRH recombination) compared to a thick 4 μm CdTe device, depending on the choice of contact, a V_{oc} decrease for the thinner device is observed (0.903 V→0.847 V). A thin CdTe device with a 0.3 eV hole

blocking contact allows for greater electron recombination at the back of the device (Figure 3-9 b.) In case c., (Figures 3-8 c. and 3-9 c.), an ohmic contact is applied, consistent with an upward curvature in the conduction band E_C near the CdTe/BC interface, as also previously shown in section 1.3.2 (Figure 1-7). Injected electrons are reflected from the back, decreasing back barrier electron recombination and resulting in a V_{oc} increase (0.903 V→1.015 V). For case d., (Figures 3-8 d. and 3-9 d.), an ohmic contact blocks electron recombination at the back contact, but suffers from greater bulk (SRH) recombination compared to a thin ohmic device, resulting in a smaller V_{oc} increase (0.903 V→0.938 V).

The above V_{oc} and band diagram simulations were generated using a highly simplified model of a CdTe device meant only to qualitatively show changes in V_{oc} with thickness and back contact. In real polycrystalline CdTe devices with $t_{CdTe} \geq 3$ μm, and V_{oc}~800 mV the CdTe diffusion length is small ($L_D < 1$ μm, [60]) and V_{oc}/photocurrent losses are dominated by SRH recombination in the space charge recombination near the CdS/CdTe junction [19].

3.2.5 SCAPS Simulations: V_{oc} Comparison to Fabricated CdTe/Cu_2Te Devices

This section discusses the V_{oc} discrepancy between theory and experiment, V_{oc} sensitivity to critical input parameters, and the simulated effect of CdS/CdTe interface recombination on V_{oc} and device performance.

A 60 mV V_{oc} discrepancy is observed for simulated baseline CdTe devices with a Cu_2Te contact with V_{oc}=903 mV (Figure 3-9 a.) and experimental devices with V_{oc}=840 mV. Hence, the above modeling is modified for the purpose of decreasing the V_{oc} discrepancy while matching the device performance to those of CdTe/Cu_2Te

devices. The input is constrained to exclude low quality device performance where J_{sc} < 23 mA/cm^2, and FF < 74%.

The sensitivity of V_{oc} is evaluated for variations in back barrier, CdTe thickness, doping, CdTe defect density, and a corresponding electron capture cross section using Eq. (3-2) with the constraint of τ=1 ns lifetime. Simulated results are illustrated in Figure 3-10.

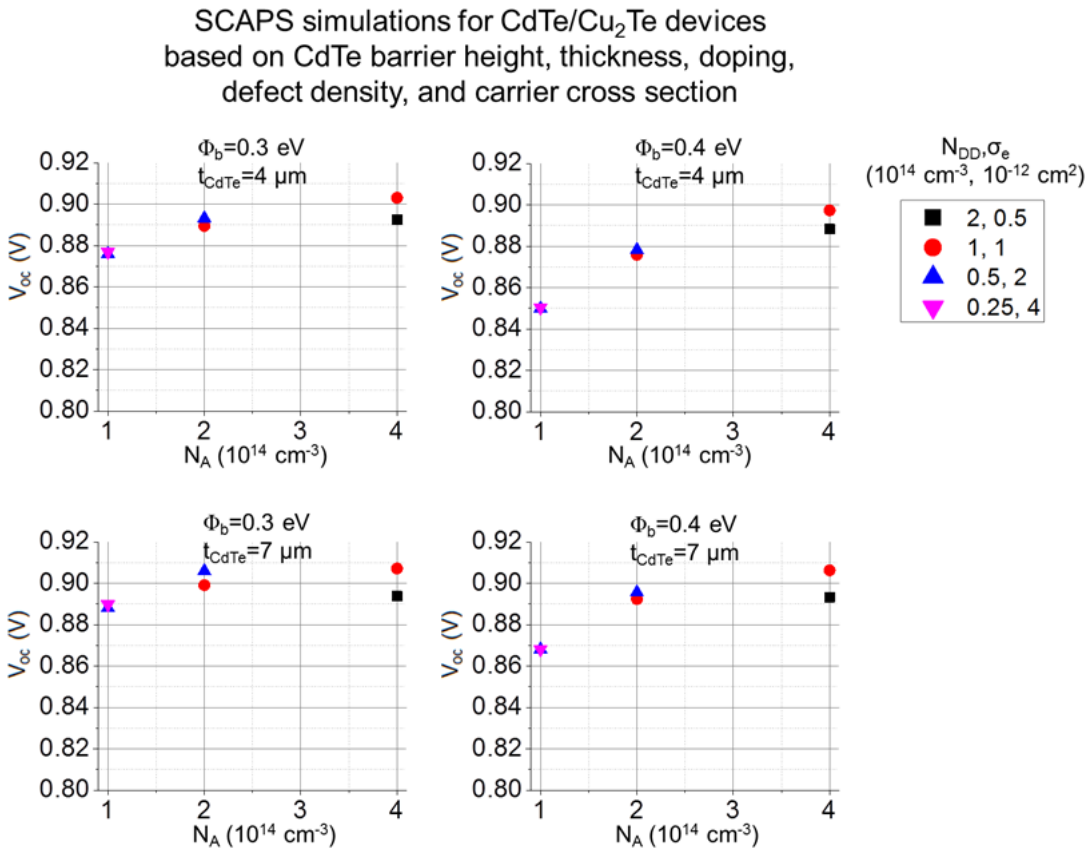


Figure 3-10: V_{oc} sensitivity to back barrier, doping, and defect density. A CdTe thickness of 4-7 μm, and 1 ns bulk lifetime is assumed. Simulations assume a CdTe doping of 1-4*10^{14} cm^{-3} based on DLCP measurements of CdTe devices with V_{oc}>800 mV, and a Cu_2Te back barrier Φb=0.3-0.4 eV ([4], Chapter 4, section 4.4.3), CdTe defect density ranging from 0.25-2*10^{14} cm^{-3}, and corresponding carrier cross section of 0.5-4*10^{-12} cm^2 based on 1 ns bulk lifetime.

By varying the thickness by 4-7 μm , back barrier from 0.3-0.4 eV, and doping and defect density by less than an order of magnitude a 30-50 mV V_{oc} decrease is observed. The simulations imply a lower V_{oc} with a smaller CdTe thickness which is expected as previously discussed. In order to test this relation experimentally, a set of window/CdTe/Cu_2Te devices would need to be developed which varied only in CdTe

thickness, but where all other material properties would be kept fixed. Such an experiment is beyond the scope of this work.

The inclusion of CdS/CdTe interface recombination was simulated in SCAPS using a device structure of a front_contact/CTO/ZTO/CdS/interface/CdTe/back_contact device. The simulation utilized the same input from Table 3-1, but with the additional input of a 2D interface layer between CdS and CdTe as illustrated in Figure 3-11 with the specific model parameters shown in Table 3-2.

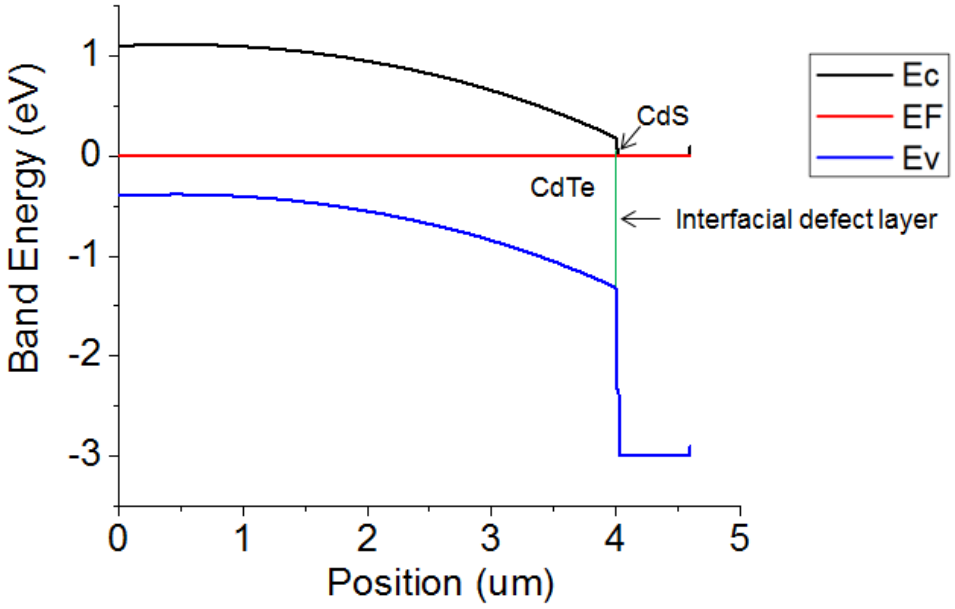


Figure 3-11: Defect model for a CdS/CdTe interfacial layer (green line) shown illustratively within a simulated equilibrium band diagram.

Table 3-2: SCAPS 2D CdS/CdTe interface input

Defect type	Uniform donor
Electron capture cross section, σ_e	10^{-17} -10^{-12}-cm^2
Hole capture cross section, σ_h	10^{-15} cm^2
Energy width	1.5 eV
Energy level relative to conduction band (E_c-E_T)	0.75 eV
Total defect density, N_{surf}	10^9-10^{14} cm^{-3}

The 2D CdS/CdTe interface is modeled to exhibit a defect distribution across the CdTe bandgap. Due to a lack of information on the nature of the CdS/CdTe defect distribution, the distribution is chosen as uniform.

A relation between the 2D defect density N_{surf} and carrier cross section σ_e is based on interface recombination velocity S

$$S = \sigma_e v_{th} N_{surf} \quad (3\text{-}3)$$

The thermal velocity is assumed as 10^7 cm/s. A recombination velocity of S=10^4-10^7 cm/s is chosen where the minimum value of 10^4 cm/s is based on cathodoluminescence measurements on CdTe polycrystalline films [82], and the maximum value of 10^7 cm/s is set equal to the thermal velocity. An upper limit of N_{surf}=10^{14} cm/s is chosen based on the CdTe dangling bond density at the terminating surface of a crystallographic CdTe plane [13], which results in a lower limit of σ_e of 10^{-17} cm^2 via Eq. (3-3). This lower limit of σ_e corresponds to a defect with a radius ~ 2 ºA which is on the order of a Cd or Te atomic radius [83]. An upper limit to σ_e of 10^-

^{12} cm^2 is chosen for the effective Coulombic carrier cross section for holes and electrons [57], and using Eq. (3-3), corresponds to a minimum surface density $N_{surf}=10^9$ cm^{-3}. The value of the hole carrier cross section σ_h is arbitrarily chosen as 10^{-15} cm^{-3} = σ_h(CdTe) based on a lack of available information.

However, by using the above model to simulate quality CdTe devices with J_{sc} < 23 mA/cm^2, and FF < 74%, a maximum 6 mV decrease in V_{oc} was observed and the lowest V_{oc} obtained was V_{oc}=845 mV for a t_{CdTe} = 4 μm device. Simulated JV curves are shown in comparison to an experimental 4 μm CdTe device (Figure 3-12).

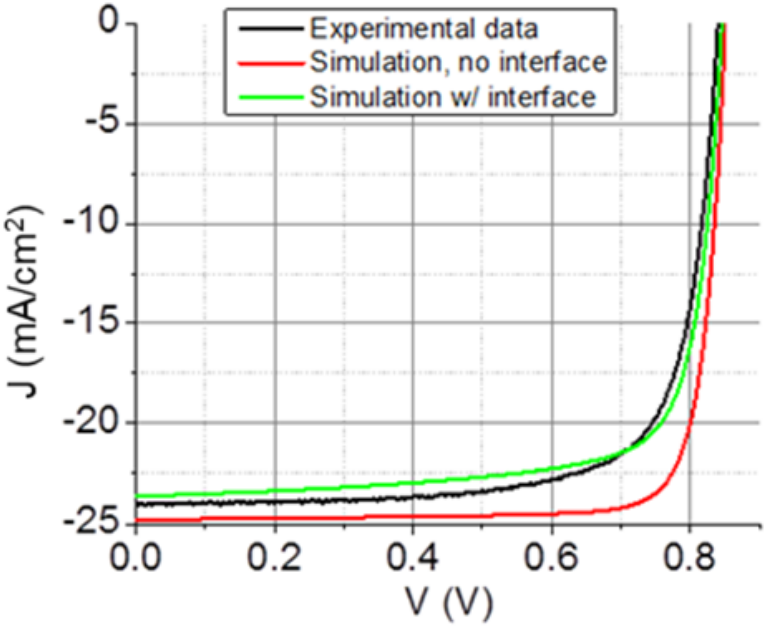


Figure 3-12: Simulated and experimental (VT481.6) JV curves for a 4 μm CdTe device. The simulated data utilized a 0.4 eV back barrier to CdTe with CdTe layer input of $N_A=10^{14}$ cm^{-3}, $N_{DD}=2.5*10^{13}$ cm^{-3}, and $\sigma_e= 4*10^{-12}$ cm^2. The interface layer input utilizes $\sigma_e= 10^{-14}$ cm^2 and Nsurf= 10^{12} cm^2.

Device performance is summarized in Table 3-3.

Table 3-3: Simulated and experimental JV device performance. Simulation input is listed above in Figure 3-12. Key: NI=no 2D interface simulation, I=Interface simulation.

Device	V_{oc}	J_{sc}	FF	G_{sc}
	mV	mA/cm^2	%	mS/cm^2
Experiment (VT481.6)	840	24.0	75.0	0.4
SCAPS- NI	850	24.8	83.5	0.3
SCAPS- I	845	23.6	76.4	1.1

While the interface simulation results in more precise JV behavior with a 5 mV discrepancy in V_{oc}, 0.5 mA/cm^2 discrepancy in J_{sc}, and 1.4% discrepancy in FF, the JV behavior from the interface simulation also shows an excessive voltage dependent collection current as represented by G_{sc}=1.1 mS/cm^2, not seen in the experimental data.

An alternative defect mechanism may be needed to represent device physics of CdTe/Cu_2Te devices. This could include a 2D or 3D bulk or interface defect which cannot be modeled by the 1D model SCAPS program. Simulations of these types of defects are beyond the scope of this work.

Chapter 4

CHARACTERIZATION OF CDTE DEVICES ON CORNING SUBSTRATE AND DIFFERENT TCO

4.1 Motivation

The development of high efficiency CdTe devices requires not only minimal recombination from the CdTe bulk and back contact, but also from the CdTe window layer interface. The ideal window layer for a CdS/CdTe superstrate device should 1.) allow for the efficient transmission of light into the CdTe layer; 2.) exhibit no interfacial strain which can otherwise cause CdTe interfacial defects; and 3.) should not diffuse impurities into the CdTe bulk.

Previous work at the Institute of Energy Conversion (IEC) has focused on the fabrication of glass/TCO/HRT/CdS/CdTe/Cu_2Te/Ni superstrate devices with particular emphasis on developing a transparent, low impurity glass/TCO/HRT (HRT=high resistance transparent layer) window layer [84]. The glass/TCO/HRT structure was developed to minimize interfacial strain with CdTe based on the use of a low impurity Corning glass with a well matched coefficient of thermal expansion (CTE) to CdTe, and high strain point temperature to allow for an increased deposition temperature of CdTe and subsequently maximize the CdTe p-doping [3].

This chapter provides background on the device performance and characteristics of superstrate glass/TCO/HRT/CdS/CdTe/Cu_2Te/Ni devices developed through a team effort between IEC and Corning where the developed window stack consisted of a low impurity Corning-glass/cadmium-stannate(CTO)/zinc-

stannate(ZTO). Efficiency for these devices typically ranges from 13-16%, and the device performance and diode characteristics are compared to alternative window layer CdTe devices with the same CdS/CdTe/contact processing. Quality CdTe devices (η=14-15%, V_{oc}=820-840 mV) based on the specialized Corning-glass/CTO/ZTO window layers, and used as a baseline to alternative contact CdTe devices are also characterized to determine device metrics which can influence recombination.

4.2 IEC/Corning Experiment

CdTe devices presented in this work were developed as an alternative to a baseline SLG/FTO/Ga_2O_3 structure with different glass/TCO/HRT structures as part of a collaboration with IEC and Corning to develop a window stack resulting in optimal efficiency. This was carried out as follows [84]: 1.) Glass layers chosen are a low iron SLG/700nm-FTO glass (TEC glass) from Pilkington, Corning glass C051, and Corning Glass C065; 2.) deposition of a 75 nm SiO_x barrier layer applied to the Corning glass to block impurity diffusion from the glass into CdTe which can occur during CdTe deposition or $CdCl_2$ heat treatment; 3.) 700 nm FTO layer or CTO (250-500 nm, 600 ºC anneal) onto the Corning glass structures; 3.) subsequent deposition of either Ga_2O_3 (40 nm Ga deposition and 550 ºC air anneal) or ZTO (50-75 nm, 550 ºC anneal); 4.) remaining CdS/CdTe/Cu_2Te/Ni fabrication steps to complete the device carried out as previously described (section 2.1) using 4-10 μm VT deposited CdTe and a $CdCl_2$ heat treatment of 422±2.5 ºC for 15-25 minutes.

Critical properties of the three types of glass used are shown in Table 4-1.

Table 4-1: Critical properties of glasses used in the IEC/Corning experiment [84] and CdTe CTE shown for comparison.

Glass type	Strain point (ºC)	glass CTE (10^{-6}/ºC)	CdTe CTE (10^{-6}/ºC)
SLG	503	9.2	5.9 [22]
C051	<600	3.2	
C065	627	4.3	

Note that the C065 glass exhibits the highest strain point (~630 ºC) and also the best matched coefficient of thermal expansion to CdTe.

4.3 Device Results

This section discusses the efficiency and device performance metrics (V_{oc}, J_{sc}, FF) from JV testing on CdTe devices based on different glass/TCO/HRT layers. In order to explain differences in device performance, specifically with V_{oc} and FF, previous characterization work using x-ray diffraction measurements to measure CdTe bulk stress [84] is discussed as well as a diode analysis (section 4.3.2), the latter of which was performed by the author. The effect of the $CdCl_2$ anneal time and CdTe deposition temperature on device performance are also discussed (sections 4.3.2, 4.3.3).

4.3.1 Effect of Glass/TCO/HRT Window Stack on Device Performance

JV curves taken on CdTe devices based on varying glass/TCO/HRT layers are illustrated in Figure 4-1.

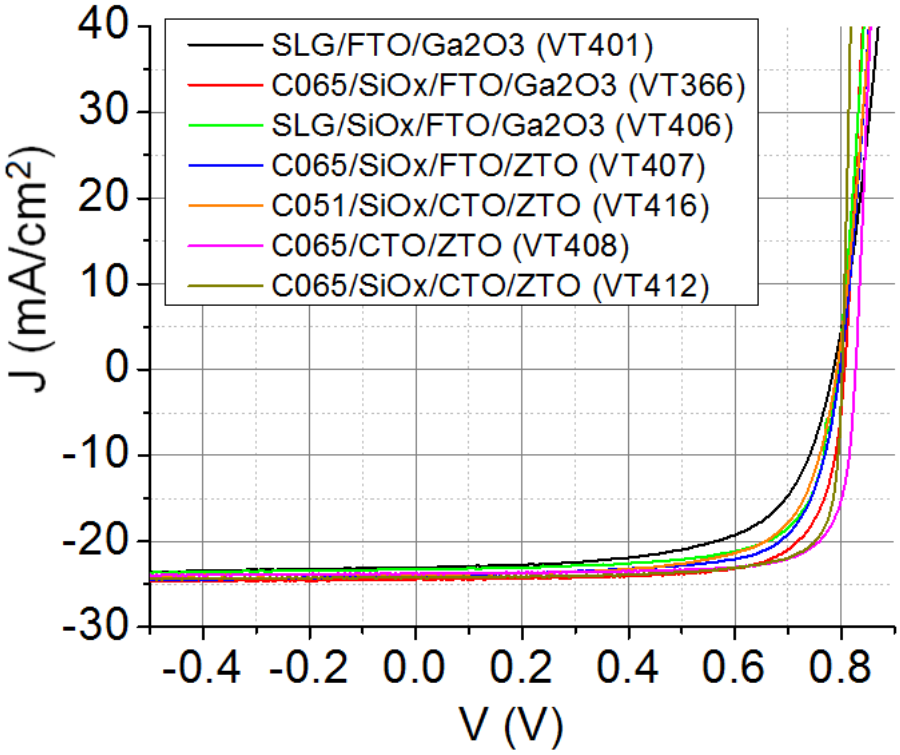


Figure 4-1: JV light curves of highest efficiency CdTe with a different glass/TCO/HRT layer, taken using VT T_{ss}= 550 ºC and a post CdTe deposition $CdCl_2$ anneal time of 15-25 minutes.

The device performance is summarized in Table 4-2.

Table 4-2: Performance of highest efficiency cells for CdTe devices with a different glass/TCO/HRT layer, taken using VT T_{ss}= 550 ºC and a post CdTe deposition $CdCl_2$ anneal time of 15-25 minutes. All devices exhibit negligible dark shunting as evidenced by values of $G_{sc,dark}$<0.2 mS/cm^2.

glass/TCO/HRT structure	V_{oc}	J_{sc}	FF	η	R_{oc}	G_{sc}
	mV	mA/cm^2	%	%	Ω-cm^2	mS/cm^2
SLG/FTO/Ga_2O_3	788	23.9	62.6	11.8	3.6	1.6
SLG/SiO_x/FTO/ZTO	793	23.2	71.6	13.2	1.7	0.9
C065/SiO_x/FTO/Ga_2O_3	806	24.4	74.9	14.7	1.0	0.6
C065/SiO_x/FTO/ZTO	797	24.0	72.1	13.8	2.0	1.3
C051/SiO_x/CTO/ZTO	792	23.8	69.7	13.1	2.6	0.4
C065/SiO_x/CTO/ZTO	801	24.2	79.6	15.4	0.5	0.3
C065/CTO/ZTO	827	23.8	79	15.5	0.8	0.5

All devices exhibit maximal current collection at short circuit conditions as evidenced by G_{sc}<2 mS/cm^2. From the set of CdTe devices with a different glass/TCO/HRT window stack, differences in device performance are listed as follows. Devices developed using SLG or C051 exhibited values of FF<72% and V_{oc}<800 mV. Devices made using C065 and FTO did achieve more moderate FF values of 72-75% suggesting reduced recombination with the use of the C065 glass. The highest efficiency devices were developed using the C065/CTO/ZTO stack which exhibit V_{oc}>800 mV FF~80%, and η>15%. This holds regardless of the use of a SiO_x impurity barrier. CTO devices also exhibit a low series resistance as evidenced by R_{oc}<1 Ω-cm^2, which may be due to the low bulk resistivity of CTO (ρ_{CTO}~10^{-4} Ω-cm [84]) or favorable window stack substrate to CdTe.

In order to understand the relation between the choice of glass/TCO/HRT and device performance, the use of x-ray diffraction was previously carried out by McCandless et al. in order to determine the bulk CdTe stress from measured strain [84]. Results are shown in Table 4-3.

Table 4-3: Measured bulk CdTe stress for different glass/TCO/HRT structure types taken by McCandless et al. [84]. XRD measurements were taken after a $CdCl_2$ treatment which relieves CdTe bulk and interface stress. Negative stress indicates in-plane bulk CdTe compression (tension normal to the substrate window). Positive stress indicates in-plane bulk CdTe tension (compression normal to the substrate window). Devices were developed using VT T_{ss}=550 ºC, a post CdTe deposition $CdCl_2$ anneal time of 15-25 minutes and V_{oc} and FF are shown based on the best efficiency cells/VT run.

VT run	glass/TCO/HRT structure	Stress (Mpa)	V_{oc} (V)	FF (%)
352	SLG/FTO/Ga_2O_3	-55	790	62.6
393	C065/SiO_x/FTO/Ga_2O_3	70	775	71.9
407	C065/SiO_x/FTO/ZTO	65	797	72.1
420	C051/CTO/ZTO	80	736	62.9
412	C065/SiO_x/CTO/ZTO	20	801	79.6

Hence, the bulk CdTe stress was minimal for the C065/CTO/ZTO device VT412 with the maximal FF=80%, while an increased magnitude of stress in the bulk CdTe layer is associated with a decreased V_{oc} and FF. An increase in bulk-CdTe stress may lead to the formation of unwanted defects either between the CdTe grain interfaces, or possibly between the window layer interfaces to CdTe. The C065 glass has the best matched CTE to CdTe as opposed to SLG and C051 (Table 4-1).

A comparison of J-V dark/light behavior for a high FF C065/CTO/ZTO device is shown in Figure 4-2.

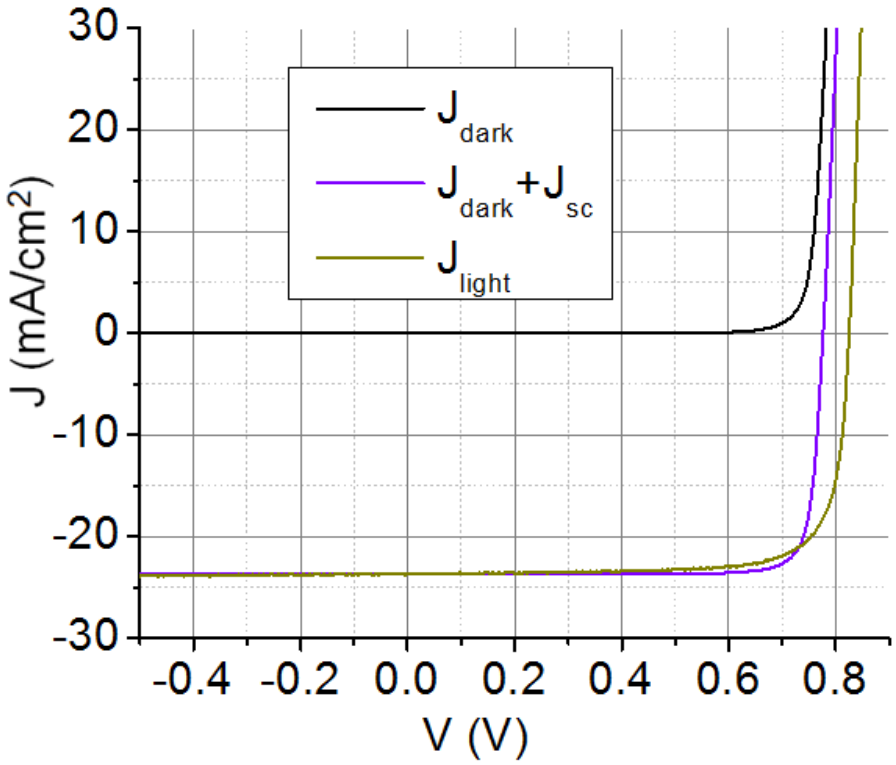


Figure 4-2: J-V dark/light behavior of a C065/CTO/ZTO device (VT408) with FF=79%.

A comparison of $J_{dark}+J_{sc}$ vs J_{light} shows that this type of device is associated with insignificant voltage dependent collection current ($G_{sc}\leq 0.5$ mS/cm^2) for V<0.5 V. The shift in V_{oc} between $J_{dark}+J_{sc}$ vs J_{light} is

$$\Delta V_{oc} = V_{oc}(J_{light}) - V_{oc}(J_{dark} + J_{sc}) \qquad (4\text{-}1)$$

For the device shown above, ΔV_{oc}~50 mV. This V_{oc} shift may be the result of a defect state resulting in recombination, but which is quenched by illumination. The use of dark/light QE at forward bias near V_{oc} on devices with a V_{oc} light shift has not been performed but may be useful in determining if the light collection mechanism resulting in the V_{oc} shift is related to a CdTe bulk or window interface recombination

mechanism. It should be noted that this comparison between $J_{dark}+J_{sc}$ vs J_{light} which results in $\Delta V_{oc}>0$ is not limited to the specific high quality polycrystalline CdTe device (VT408) but is also observed in other high quality solar cells such as single crystal GaAs.

4.3.2 Diode Analysis of CdTe Devices with Different Glass/TCO/HRT Window Stacks and $CdCl_2$ Anneal Time

In this section, a conventional room temperature J-V diode analysis of extracting diode factor A is performed for the various glass/TCO/HRT window stacks at different $CdCl_2$ anneal times (15 and 25 minutes) to gain insight on the dominant recombination mechanism. Using dark JV data at 300 ºK, a conventional JV diode analysis is used to extract the diode factor A and recombination current J_0 [17] with

$$\frac{dV}{dJ} = R_s + \frac{1}{(J + J_L - GV)}\frac{AkT}{q} \tag{4-2}$$

and

$$\ln(J + J_L - GV) = \ln(J_0) + \frac{q(V - JR_s)}{AkT} \tag{4-3}$$

to calculate A and J_0. For quality devices, the dark shunt conductance G<1 mS/cm^2 and hence J>>GV in forward bias. It is of interest to examine the recombination mechanisms in far forward bias for $V=V_{oc}$, where $J+J_L=0$. However, when attempting to fit JV data taken under illumination, a critical issue that arises is the phenomenon of voltage dependent collection current [19], resulting in values of $J_L(V)/J_{sc}$~0.5-1, and nonlinear dV/dJ vs $1/(J+J_L-GV)$ fitting for JV light data. Another complication in fitting using JV light data are the effects of light oscillations resulting in nonlinear behavior. Hence, for calculating A and J_0, dark JV measurements are more reliable.

To estimate the recombination mechanisms in far forward bias with $V \sim V_{oc}$, dark JV fitting is performed for $J \geq 0.01$ A/cm^2 or $1/J \leq 100$ cm^2/A.

For CdTe devices with various window stack layers, plots of dV/dJ vs 1/(J-GV) with associated fits used to determine the diode factor A are illustrated in Figure 4-3.

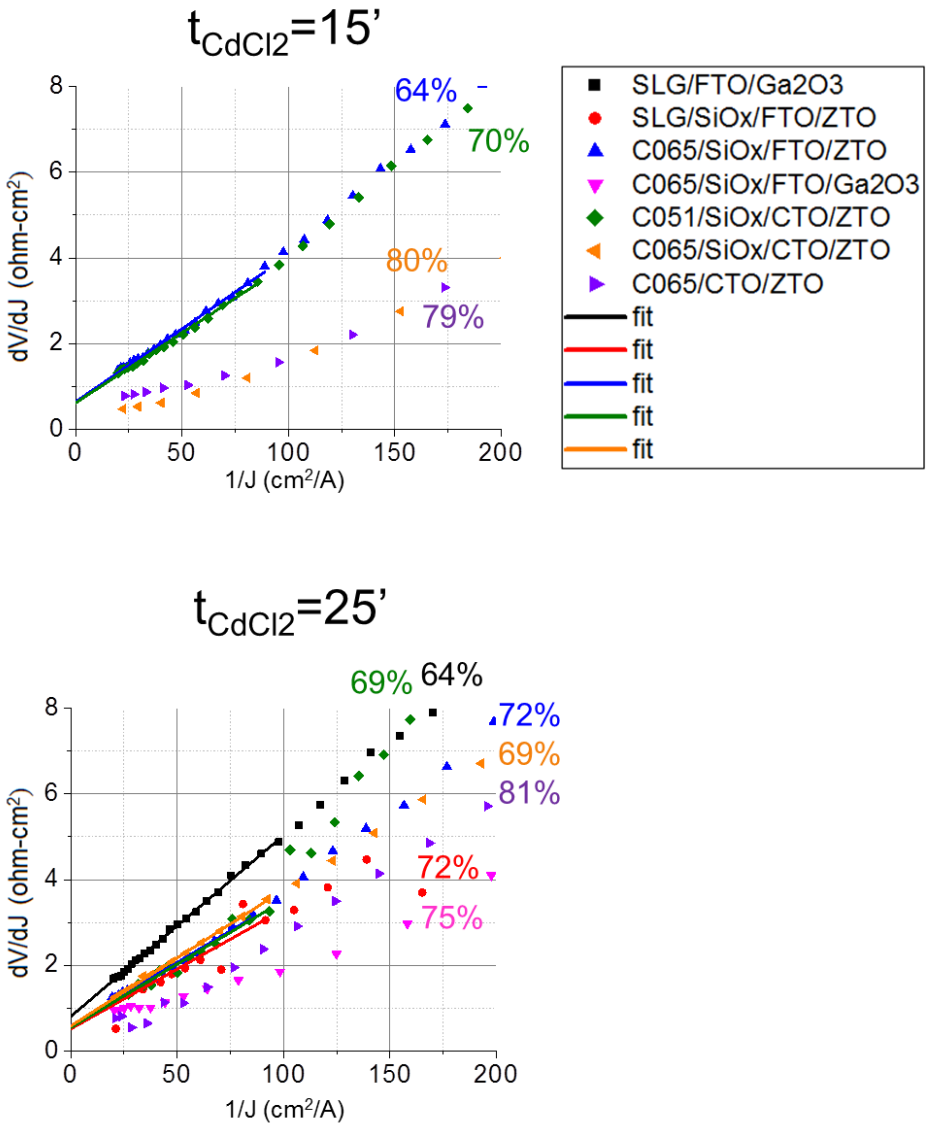


Figure 4-3: dV/dJ vs 1/(J-GV) using dark J-V data with associated FF (percent values) for the highest efficiency CdTe devices developed with various glass/TCO/HRT window stacks (VT T_{ss}= 550 ºC) for a 15 and 25 minute $CdCl_2$ anneal. A fitting analysis is performed using Eq. (4-2) for linear dV/dJ vs 1/(J-GV) data with J≥10 mA/cm^2. Cells with parasitic behavior exhibiting efficiency η<10%, R_{oc}>4 Ω-cm^2 (excessive series resistance), or G_{sc} > 2 mS/cm^2 (excessive voltage dependent collection current or shunting) are excluded from this analysis.

From the fitting analysis of linear data, series resistance R_s<1 Ω-cm^2 for all devices. However, for devices with FF≥75%, the value of dV/dJ appears to flatten with 1/(J-GV)<50 cm^2/A, suggesting that the blocking contact is influencing the J-V behavior. Attempts to fit the high FF devices for 1/(J-GV)<50 cm^2/A results in nonphysical values of A<1 while fits with 1/(J-GV)>50 cm^2/A result in nonphysical values of R_s<0. Hence, for high FF devices, meaningful linear fits to determine the diode characteristics cannot be determined from the dark JV data. If the apparent flattening in the dV/dJ curves is caused by the a blocking back contact, a more accurate estimate of diode factor A may be obtained by JV measurements at higher temperature (T>300 ºK) which could allow for greater current transport and less influence of the back contact on the JV device physics.

As previously stated (section 2.1.4), a $CdCl_2$ treatment is utilized to passivate CdTe grains, increase CdTe bulk p-doping, passivate the CdTe interface, and thin CdS to decrease parasitic CdS light absorption. However, an excessive treatment can also lead to formation of a CdTe/TCO junction resulting in a higher recombination current [41]. The optimal $CdCl_2$ treatment for a CdTe device is also dependent on the CdTe thickness which influences grain size [27]. The optimal treatment is probably also dependent on VT deposition temperature, and the underlying substrate, both of which influence the material properties of the CdTe bulk.

Table 4-4 summarizes the diode characteristics of the CdTe devices with various glass/TCO/HRT window stacks taken at different $CdCl_2$ anneal times.

Table 4-4: V_{oc}, FF and diode characteristics of the highest efficiency CdTe devices developed with various glass/TCO/HRT window stacks (VT T_{ss}= 550 ºC) but different $CdCl_2$ annealing time. A_1→diode factor derived from dV/dJ vs 1/(J-GV) (Eq. (4-2)). A_2, J_0→diode factor and recombination current derived from ln(J-GV) vs V-R_sJ (Eq. (4-3)). For each CdTe device, fitting for A_1 and A_2 was taken using the same J-V dataset with J>10 mA/cm^2. Values of A_1, A_2, and J_0 are listed as inconclusive if the dV/dJ or ln(J-GV) plots were nonlinear.

Sample VT#	Structure	t_{CdCl2}	t_{CdTe}	A_1	A_2	J_0	FF	V_{oc}
		min	µm			mA/cm^2	%	mV
401.1	SLG/FTO/Ga_2O_3	25	9.8	1.66	1.65	1E-7	64.2	785
406.2	SLG/SiO_x/FTO/ZTO	25	4.9	1.09	1.06	7E-12	71.6	793
407.3	C065/SiO_x/FTO/ZTO	15	4.0	1.34	1.33	3E-9	64.3	769
407.6		25		1.23	1.23	1E-9	72.1	797
366.6	C065/SiO_x/FTO/Ga_2O_3	25	5.5	inconclusive			74.9	806
416.5	C051/SiO_x/CTO/ZTO	15	7.3	1.28	1.27	5E-10	69.7	792
416.1		25		1.15	1.15	4E-10	69.0	768
412.6	C065/SiO_x/CTO/ZTO	15	5.7	inconclusive			79.6	801
412.2		25		1.24	1.25	3E-10	68.7	791
408.5	C065/CTO/ZTO	15	4.4	inconclusive			79.0	827
408.6		25		inconclusive			73.0	795
448.6		25	8.0	inconclusive			81.1	812

For each CdTe device, fits using Eqs.(4-2) (dV/dJ method) and (4-3) (semilog method) are taken over the same JV data and reveal no significant differences in the subsequent calculations of diode factor. The variation of A between 1 and 2 depends on the energies of defects within the CdTe bandgap [85] where A=2 implies recombination dominated by midgap defects (SRH) while A=1 implies radiative recombination or possibly an interface mechanism.

A CdTe device (VT401.1) developed with a SLG/FTO/Ga_2O_3 window stack exhibits relatively large values of recombination current (10^{-7} mA/cm^2) and values of A>1.6, implying a SRH trend with low FF~64%. Note however that the CdTe layer

for this device is considerably thick (10 μm) suggesting a larger CdTe grain size [27] and a 25 minute $CdCl_2$ treatment may be inadequate. When a SiO_x barrier is deposited on SLG, a ZTO layer is utilized, and the CdTe layer is thinner (4.9 μm) an 8 mV improvement in V_{oc} and 7% improvement in FF are observed and associated with a decrease in J_0 by 4 orders of magnitude and value of A~1.1.

The best efficiency CdTe devices developed with SLG and C051 glass are associated with FF=69-72%, V_{oc}=768-793 mV, A=1.0-1.3, and $J_0=10^{-11}$-10^{-9} mA/cm^2. While the values of diode factor A=1.0-1.3 suggest that SRH recombination is not dominant, FF and V_{oc} performance of these devices lag compared to devices developed utilizing the C065 glass. Devices developed with SLG and C051 may suffer from a possible CdTe interface strain leading to surface defects as a result of a large CTE mismatch between the glass and CdTe, and resulting bulk CdTe stress (Tables 4-1, 4-3) or glass impurity contamination. Many devices developed with C051 suffered from pinholes associated with contaminants from the C051 glass, possibly forming an unfavorable defect [84].

Table 4-4 suggests that for devices developed with identical processing conditions with exception to a 15 vs 25 minute $CdCl_2$ anneal time, with similar values of CdTe thickness, (4-6 μm) the best device performance may depend on the glass/TCO/HRT layer. The best device performance for C065/SiO_x/FTO/ZTO devices were developed with a 25 minute anneal time (VT407). However, for CdTe devices developed using C065 glass, TCO=CTO layer and HRT=ZTO layer and otherwise identical processing conditions with exception to the $CdCl_2$ anneal time (VT408 and VT412), the best device performance is observed for a 15 minute treatment with FF~80%, and V_{oc}=800-830 mV. High FF~80% devices with V_{oc}>800 mV however

have been developed with a 25 minute $CdCl_2$ treatment but with a thicker CdTe layer (8 μm). However, device performance data is limited for CdTe devices with a C065/CTO/ZTO window stack and fabricated at T_{ss}=550 ºC. An in depth fabrication study on device performance vs CdTe thickness and $CdCl_2$ anneal time for these types of devices is beyond the scope of this work.

For C065 devices with a TCO=CTO an HRT=ZTO layer, no difference is seen in the use of a SiO_x barrier and FF performance. Assuming that the barrier efficiently blocks glass impurities which result in parasitic defect states, the barrier may make no difference to affect recombination if the C065 glass impurity concentration was too low to degrade device performance.

4.3.3 Effect of VT Deposition Temperature on Device Performance

This section provides the results and discussion on the effect of CdTe efficiency and device performance metrics (V_{oc}, FF, J_{sc}) for the CdTe deposition temperature range T_{ss}=550-630 ºC. A more in depth characterization analysis of CdTe devices with T_{ss}=550-630 ºC is given in Appendix A.

The high strain point of the C065 glass (T_{strain}=627 ºC, Table 4-1) allows for higher VT processing temperature without fracture of the glass substrate as compared to the Pilkington SLG (T_{strain}=503 ºC, Table 4-1), which can fracture at temperatures above 550 ºC. CdTe devices with a C065/CTO/ZTO window stack have thus been processed at VT deposition temperatures T_{ss}=590 ºC- 630 ºC, where the maximum 630 ºC temperature was based off the C065 strain point. Each device consists of a 1”x1” or 2”x1” sample with 4 or 8 cells (0.36 cm^2) respectively.

The device performance metrics of C065/CTO/ZTO CdTe devices developed using a 25 minute $CdCl_2$ heat treatment, and VT deposition temperature T_{ss}=550-630 ºC is shown in Figure 4-4.

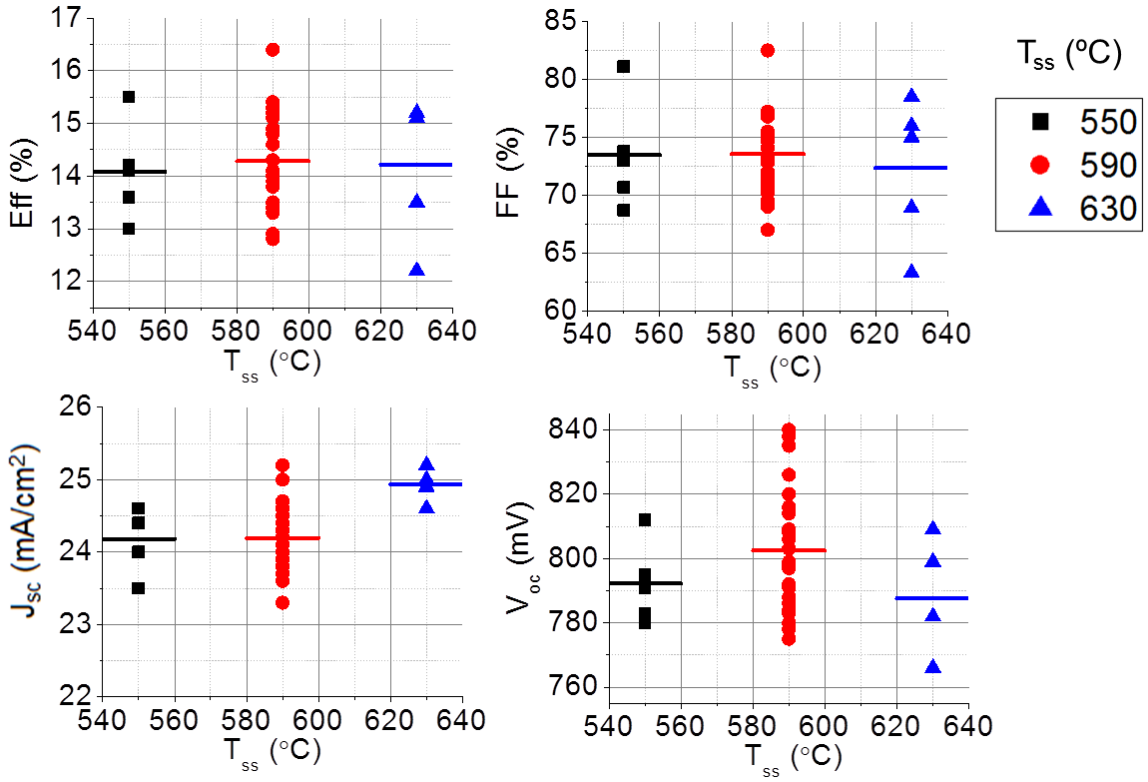


Figure 4-4: Device performance metrics of C065/CTO/ZTO best efficiency CdTe cells/sample with t_{CdCl2}=25 minutes, and T_{ss}=550-630 ºC. Samples are of size 1"x"1 or 2"x1". Solid lines represent statistical averages. Cells with parasitic behavior exhibiting efficiency η<10%, R_{oc}>4 Ω-cm^2 (excessive series resistance), or G_{sc} > 2 mS/cm^2 (excessive voltage dependent collection current or shunting) are excluded from this analysis.

Table 4-5 lists the average device performance based on VT T_{ss}.

Table 4-5: Average device performance metrics of best efficiency CdTe C065/CTO/ZTO cells/sample based on VT T_{ss}.

T_{ss}	V_{oc}	J_{sc}	FF	η
(ºC)	mV	mA/cm^2	%	%
550	792	24.2	73.5	14.1
590	803	24.2	73.6	14.3
630	788	24.9	72.3	14.2

A limited number of measurements have been taken on CdTe devices at 550 ºC and 630 ºC and a statistical comparison of device performance based on T_{ss} cannot be concluded. There may exist a trend for T_{ss} on V_{oc} (550-630 ºC) and J_{sc} (590-630 ºC). An increased CdTe deposition temperature may form a higher p-type material due to CdTe thermochemistry [3] resulting in a V_{oc} increase from 550-590 ºC. From 590-630 ºC , a competing recombination mechanism is increased impurity diffusion from the C065 glass into the CdTe at higher anneal temperatures which may result in the lower V_{oc} and FF for T_{ss}=630 ºC deposited films. The effect of CdTe doping with T_{ss} is discussed in greater detail in Appendix A.

A possible increase in J_{sc} may occur when varying T_{ss}=590-630 ºC. This is explained as follows. Increasing the CdTe deposition (anneal) temperature with a fixed $CdCl_2$ treatment results in depletion of sulfur from CdS into CdTe [18] and subsequent thinning of CdS. A thinner CdS results in a higher transmission of blue light into the CdTe layer which is absorbed and converted to photocurrent. This can be observed in quantum efficiency measurements and is discussed in greater detail in Appendix A.

No correlation was seen with CdTe thickness (4-10 μm) and device performance on the samples in Figure 4-4. The use of a 15 vs 25 minute $CdCl_2$ treatment on T_{ss}=590 ºC devices also does not show a device performance trend, but quality cell data is limited.

Baseline C065/CTO/ZTO/CdS/CdTe/Cu_2Te/Ni devices used in comparison to alternative contact devices exhibit V_{oc}=800-840 mV and are developed using a VT deposition T_{ss}=590-630 ºC. Alternative contact devices are developed using the same window/CdTe stack material as baseline devices. It would be more ideal to exclusively develop alternative contact CdTe devices using T_{ss}=590 ºC window/CdTe stack material that resulted in a higher V_{oc}(CdTe/Cu_2Te)=820-840 mV (Figure 4-4). However, the scarcity of quality window/CdTe stack material available for alternative contact CdTe device processing limits us to the use of both moderate quality window/stack material resulting in V_{oc}(CdTe/Cu_2Te)=800 mV and higher quality window/CdTe stack material resulting in V_{oc}(CdTe/Cu_2Te)=820-840 mV.

4.4 Characterization of High Quality Baseline CdTe Devices

This section provides background on the characteristics of quality CdTe devices with V_{oc}>820 mV which were used as a baseline to compare to alternative contact CdTe devices. Measurements are performed to estimate second order metrics which can influence recombination and hence open circuit voltage. These include bandgap, CdTe crystal disorder properties (Urbach energy), space charge width, doping, diode ideality factor, recombination current, activation energy of recombination, and back barrier. Baseline devices analyzed have been given a complete set of CV/DLCP, quantum efficiency (QE), and current-voltage-temperature-light intensity (JVTI) measurements. The focus is on baseline devices which exhibited high V_{oc}=822-840 mV and are used for comparison with alternative contact CdTe/PCBM devices (Chapter 6).

CdTe baseline samples were fabricated in a C065/CTO/ZTO/CdS/CdTe/Cu_2Te/Ni structure using the previously described

fabrication process (section 2.1) with 500 nm CTO, a VT deposition temperature of 590 ºC, 4.2-7.3 μm of CdTe and a post deposition $CdCl_2$ heat treatment of 425 ºC for 25 minutes anneal time. The completed CdTe cells vary only in thickness and therefore, slight CdTe grain size variations are also to be expected [27]

4.4.1 J-V and QE

J-V measurements are shown to characterize device performance, and analyze diode recombination, while QE measurements are shown to characterize photocurrent losses and CdTe bandtail absorption properties of bandgap and Urbach energy [51].

4.4.1.1 J-V Measurements and Device Performance

The J-V measurement curves and device performance of two high V_{oc} baseline CdTe devices is summarized in this section. Figures 4-5 and 4-6 show the J-V measurement curves and device performance metrics of the CdTe baseline cells.

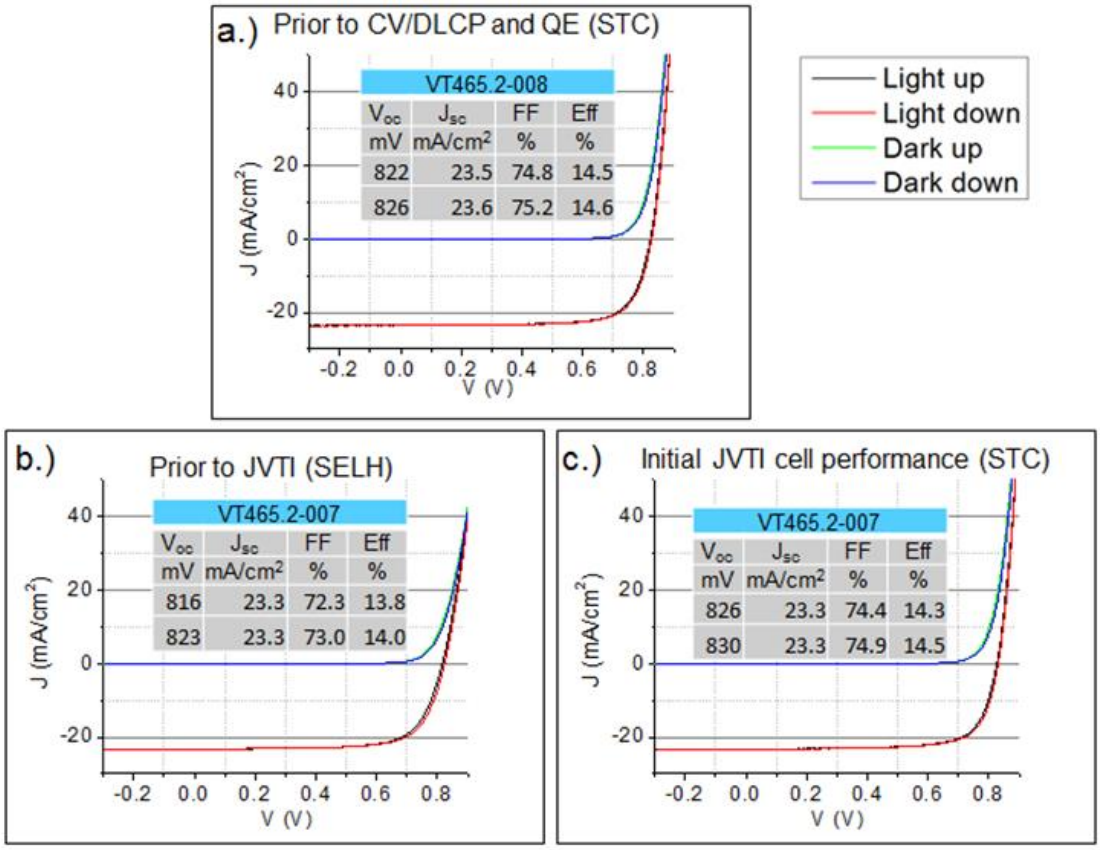


Figure 4-5: JV measurements for the baseline sample VT462.5, used for characterization measurements and taken at STC and SELH (SELH conditions: T= 300 ºK, 1000 W/m^2, and ELH bulb illumination) conditions. The first/second data rows respectively represent measurements taken using an up/down voltage sweep. SELH conditions are taken prior to cells which undergo JVTI testing.

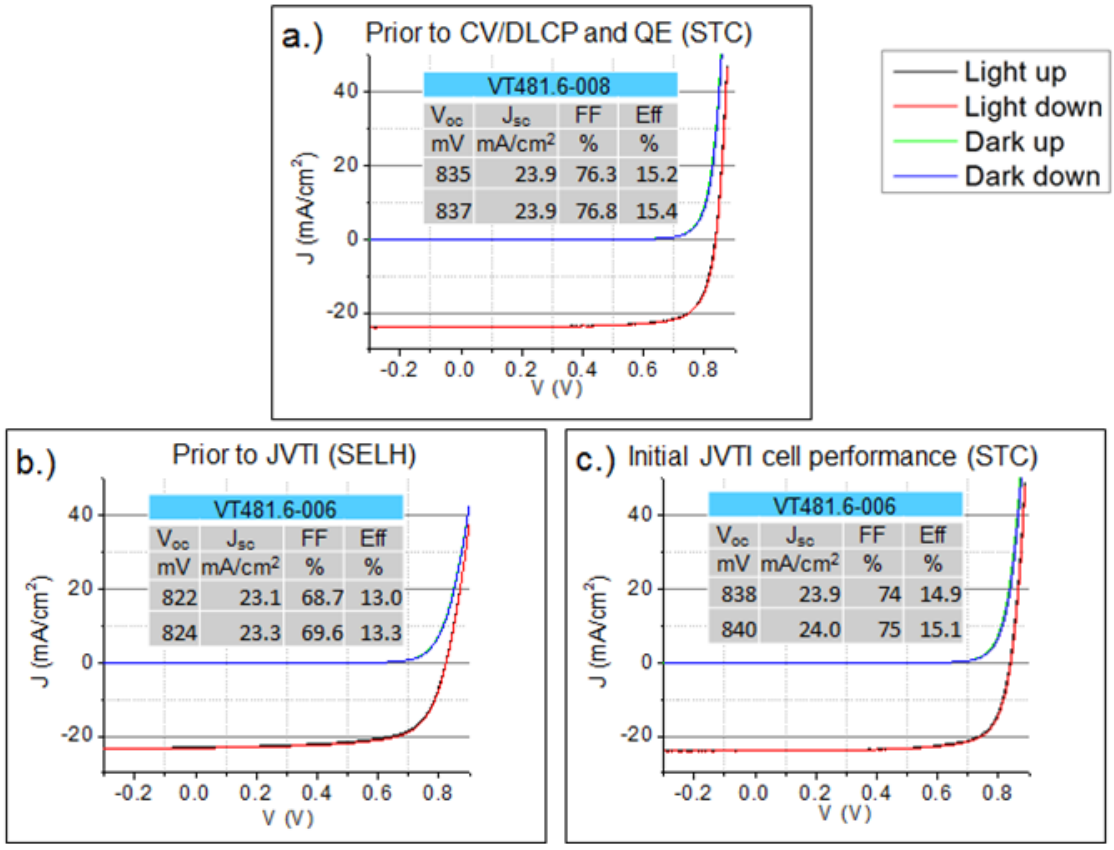


Figure 4-6: JV measurements for VT481.6, used for characterization measurements and taken at STC and SELH (T= 300 ºK, 1000 W/m^2, and ELH bulb illumination) conditions. The first/second data rows respectively represent measurements taken using an up/down voltage sweep. SELH conditions are taken prior to cells which undergo JVTI testing.

A summary of device performance metrics of the baseline CdTe devices is shown in Table 4-6.

Table 4-6: Device performance metrics of baseline CdTe devices.

V_{oc}	J_{sc}	FF	η
mV	mA/cm^2	%	%
816-840	23.1-24.3	68.7-76.8	13.0-15.4

J-V measurements on quality baseline characterization cells show the following: 1.) negligible dark shunting, $G_{sh,dark}$ <0.02 mS/cm^2 within the devices as shown by flat dark J-V measurements up to 0.6 V; 2.) stability/repeatability in the JV profiles as evidenced by negligible hysteresis between up/down voltage sweeps where $|V_{oc,up}-V_{oc,down}| \leq 5$ mV (see Table 4-6); and 3.) for chosen cells taken at AM1.5 standard test conditions (STC), repeatable device performance measurements between cells on the same sample, but used for different characterization techniques as evidenced by $\Delta V_{oc,STC,cells} \leq 8$ mV.

However, for cells utilized for JVTI testing (VT465.2-007 and VT481.6-006) initial JV testing at STC resulted in higher device performance, compared to a later retest of the cells taken under SELH conditions, where the SELH retests are performed prior to JVTI measurements. Retests of the JVTI cells reveal a slight increase in voltage dependent collection current as noted by J-V curvature in forward bias for light measurements. This suggests cell degradation or a mismatch between the AM1.5 and ELH bulb spectrum which results in increased recombination (lower photocurrent collection) and decreased V_{oc} and FF [19], resulting in η=13.0-14.0%. In addition, FF reductions in JV(SELH) retests also result from an increase of series resistance ΔR_s=0.6-0.9 ohm-cm^2 which may be attributed to uncontrolled lateral resistance

across the sample from excessively spaced positive and negative contacts during JV testing.

The characterization samples, thickness and V_{oc} with the corresponding cell for each characterization measurement are listed in Table 4-7.

Table 4-7: List of CdTe samples chosen for characterization with associated CdTe thickness and best cell V_{oc}. The V_{oc} range (in bold) is due to hysteresis in the measurement as observed voltage up/down sweeps during J-V measurements. Key: STC=standard test conditions, SELH=standard ELH conditions of 300 ºK and 1000 W/m^2 using an ELH bulb (JVTI measurements).

Sample	t_{CdTe} (μm)	best cell V_{oc}(STC) (mV)	V_{oc}(STC) (mV)		V_{oc}(SELH) (mV)
			CV/DLCP	QE	JVTI
VT465.2	7.3	**826-830** 007	**822-826** 008	**822-826** 008	**816-821** 007
VT481.6	4.2	**838-840** 006	**835-837** 008	**835-837** 008	**822-824** 006

Hence, the characterization device V_{oc} is within 16 mV of the best cell/sample V_{oc} measurement.

4.4.1.2 QE Measurements

In order to analyze photocurrent losses of the two baseline cells with variations in CdTe thickness (4-7 μm), and compare the resulting Urbach energy and bandgap, quantum efficiency (QE) measurements are taken. Quantum efficiency measurements of the two baseline CdTe devices are shown in Figure 4-7.

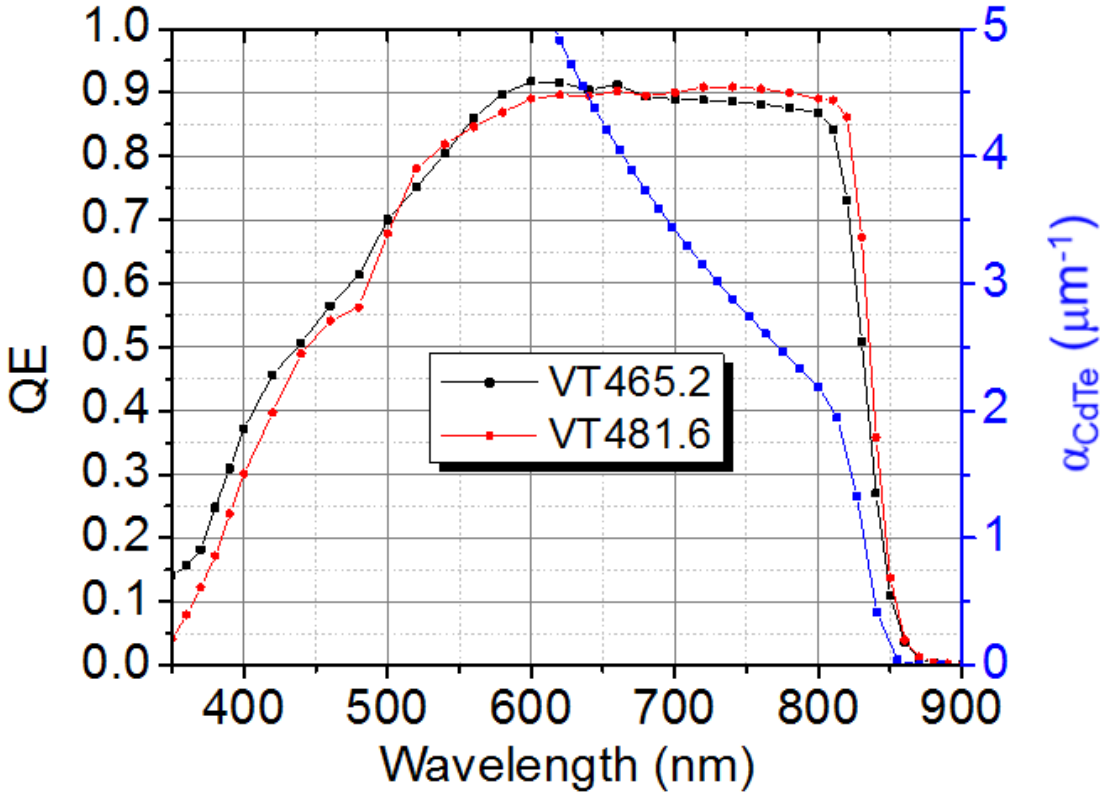


Figure 4-7: Quantum efficiency of the CdTe baseline devices, taken at equilibrium conditions (0V). The blue curve represents the CdTe absorption coefficient.

The quantum efficiency can be described as follows. For photons with wavelengths: 1.) $\lambda \leq 420$ nm, the CTO, ZTO, and CdS layers, absorb most light contributing to a photocurrent loss ~1 mA/cm^2; 2.) $420 < \lambda \leq 600$ nm the CTO and ZTO layers with a 3 eV bandgap transmit most of the light, while the CdS layer with a 2.4 eV bandgap absorbs light, and additional photocurrent losses possibly due to a Te rich CdS interface alloy ($CdS_{1-y}Te_y$) with a bandgap $E_{g,alloy} < 2.4$ eV [18], resulting in a photocurrent loss of 2-2.5 mA/cm^2; 3.) $600 < \lambda \leq 820$ nm, light absorption in CdTe and photocurrent collection limited only by light reflection and recombination losses; 4.)

λ>820 nm, inefficient light absorption in CdTe where photon absorption with energy <1.5 eV (λ>825 nm) could be influenced by a lowered bandgap sulfur rich CdTe film [18], and the presence of CdTe bandtail states [86], [87], resulting in an exponential decrease of the CdTe absorption coefficient and QE vs. photon energy (Appendix B).

The integrated quantum efficiency (IQE, section 2.3.2, Eq. (2-14)) is within 10% of the J-V measured short circuit current, J_{sc} as shown in Table 4-8.

Table 4-8: Measured IQE vs J_{sc}.

Sample	IQE (mA/cm^2)	J_{sc} (mA/cm^2)
VT465.2	22.7	23.6
VT481.6	22.8	23.9

Since the QE spectrum does not perfectly match with the AM 1.5 spectrum used to calculate J_{sc}, , a large 10% difference can be attributed to spectral mismatch [88] between the AM1.5 spectrum used to calculate J_{sc} and the QE optical spectrum used to calculate IQE. As previously mentioned in section 2.3.2.2, before QE measurements on a CdTe device are taken, QE measurements with a 1.1 eV bandgap Si calibration cell are taken from 350-1200 nm and the QE optical spectrum is calibrated such that integration of the photocurrent using the Si cell results in a small 1% difference between IQE and J_{sc}. Then, QE measurements are taken with a 1.5 eV CdTe device from 350-900 nm. Improvements on minimizing the IQE, J_{sc} difference for CdTe devices could include modification of the QE optical spectrum with a 1.5 eV bandgap calibration device prior CdTe cell measurements. However, such a difference in IQE should not be relevant for the purpose of using QE to evaluate CdTe optoelectronic properties of bandgap and Urbach energy which are related to the CdTe absorption coefficient, not the incident light intensity $I_0(\lambda)$. When applying an additional 90%

suns white bias light on the device, the IQE only changes by 0.5% or less, and this has no effect on calculations of bandgap and Urbach energy, which are discussed below.

The CdTe bandgap E_g and Urbach energy E_U are measured from long wavelength QE measurements (Figure 4-7) where band-tail light absorption is observed in the QE data ($E>E_g$=1.5 eV or λ>820 nm). Fitting was performed over λ=850-880 nm using

$$\ln\big(QE(E)\big) = \frac{(E - E_g)}{E_U} \tag{4-4}$$

and the fits are shown in Figure 4-8.

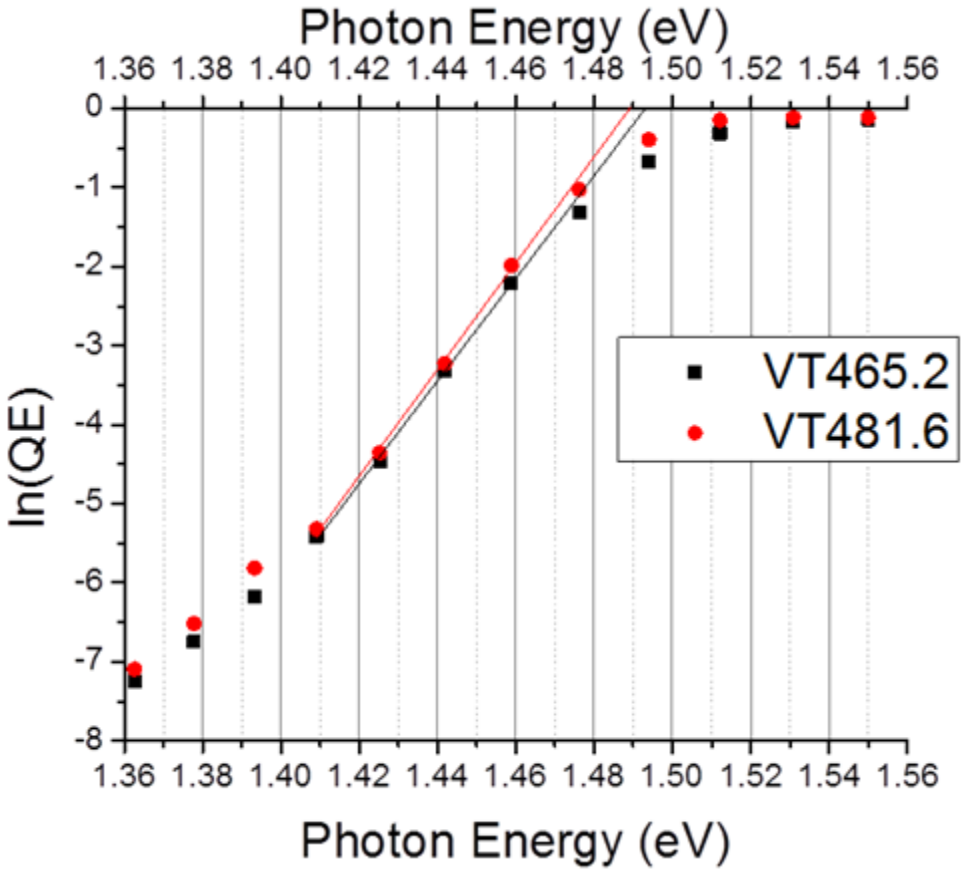


Figure 4-8: Experimental ln(QE) vs E data with fitting of ln(QE) vs E to determine the bandgap E_g and Urbach energy E_U. The best fit is found over 4 points from 1.41-1.46 eV (850-880 nm). Below 1.41 eV (880 nm), noise dominates the QE.

The theory of infrared wavelength QE measurements and the fitting method used to determine bandgap E_g and Urbach energy E_U from Eq. (4-4) is discussed in Appendix B. Results are shown in Table 4-9.

Table 4-9: Measured bandgap and Urbach energy

Sample	t_{CdTe} (μm)	V_{oc} (mV)	E_g (eV)	E_U (meV)
VT465.2	7.3	822-826	1.49	15
VT481.6	4.2	835-837		

The 1.49 eV bandgap of the samples is slightly lower than 1.5 eV observed for pure CdTe [89]. The presence of sulfur is expected from sulfur interdiffusion during the $CdCl_2$ treatment and may explain the lowered 1.49 eV bandgap [18], [43]. Based on bandgap modeling of $CdTe_{1-x}S_x$ alloys, a 1.49 eV bandgap suggests an alloyed $CdTe_{1-x}S_x$ absorber layer with a 2% (x=0.02) sulfur concentration [18].

For the polycrystalline baseline CdTe devices, E_U~15 meV. While the higher V_{oc} device (VT481.6-008) is associated with a lower Urbach energy, and possibly less crystal disorder [52], the use of x-ray diffraction (XRD) or atomic force microscopy (AFM) measurements would be needed to measure the crystal disorder by TEM measurements of CdTe intragrain structure possibly grain size distribution [27], [43]. This is beyond the scope of this work. In comparison, the use of transient photocapacitance measurements were previously used on VT deposited CdTe devices including the sample VT481.6 which resulted in an Urbach energy measurement of 20 meV [90]. Single crystal CdTe with less disorder has been observed to exhibit a smaller Urbach energy, E_U=7-9 meV at 300 ºK [91], [92]. Single crystal champion devices have also resulted in record V_{oc}=1017 mV [14] compared to champion polycrystalline CdTe devices with higher crystal disorder, possible bulk/grain boundary recombination and V_{oc}=876 mV [8]. This is all evidence that there is still opportunity for improving thin films by reducing intra-grain lattice defects.

4.4.1.3 Diode Analysis

In this section, a conventional room temperature dark J-V diode analysis of extracting recombination metrics A, J_0 is evaluated for the baseline cells, utilizing Eqs. (4-2) and (4-3). For CdTe cells used for JVTI measurements, values of A and J_0 taken using Eq. (4-3) are shown in Table 4-10.

Table 4-10: Values of A and J_0 for baseline cells (VT465.2-007 and VT481.6-006) utilized for JVTI measurements and taken using dark JV data at 300 ºK. Key: Initial=initial cell performance, retested=prior to JVTI analysis.

Sample	t_{CdTe}	A (Initial)	A (retested)	J_0 (Initial)	J_0 (retested)
	µm			mA/cm^2	mA/cm^2
VT465.2	7.3	1.36	1.50	$1*10^{-9}$	$9*10^{-9}$
VT481.6	4.2	1.31	1.39	$4*10^{-10}$	$2*10^{-9}$

For dark measurements, measured diode factors of the cells result in values of 1.3-1.5, and recombination current $J_0 \sim 10^{-9}$-10^{-8} mA/cm^2. When the cells are retested prior to JVTI measurements, a further increase in A and J_0 is observed which is probably due to cell degradation as evidenced by increased voltage dependent collection current with associated FF decreases of 2-5% and V_{oc} decreases of 7-16 mV (Figures 4-5, 4-6). The calculated diode factor values of A=1.3-1.5 are consistent with previous measurements on CdTe polycrystalline devices [17], and comparable to moderate FF (68%-73%) CdTe devices with different window and VT processing conditions (Figure 4-3).

4.4.2 CV and DLCP Measurements

This section presents the results of CV and DLCP measurements on the baseline cells used to estimate to estimate CdTe space charge width and doping. Measurements were taken at 300 ºK, 1 MHz, and from -1V to 0.5 V forward bias.

4.4.2.1 Estimated Space Charge Width

A lower limit of space charge width (W) was estimated by using the moment of charge response, <x> measured by capacitance measurements and calculated via Eq. (2-37) for CV measurements and Eq. (2-45) for DLCP measurements. Measurements of <x> as a function of applied bias are shown in Figure 4-9.

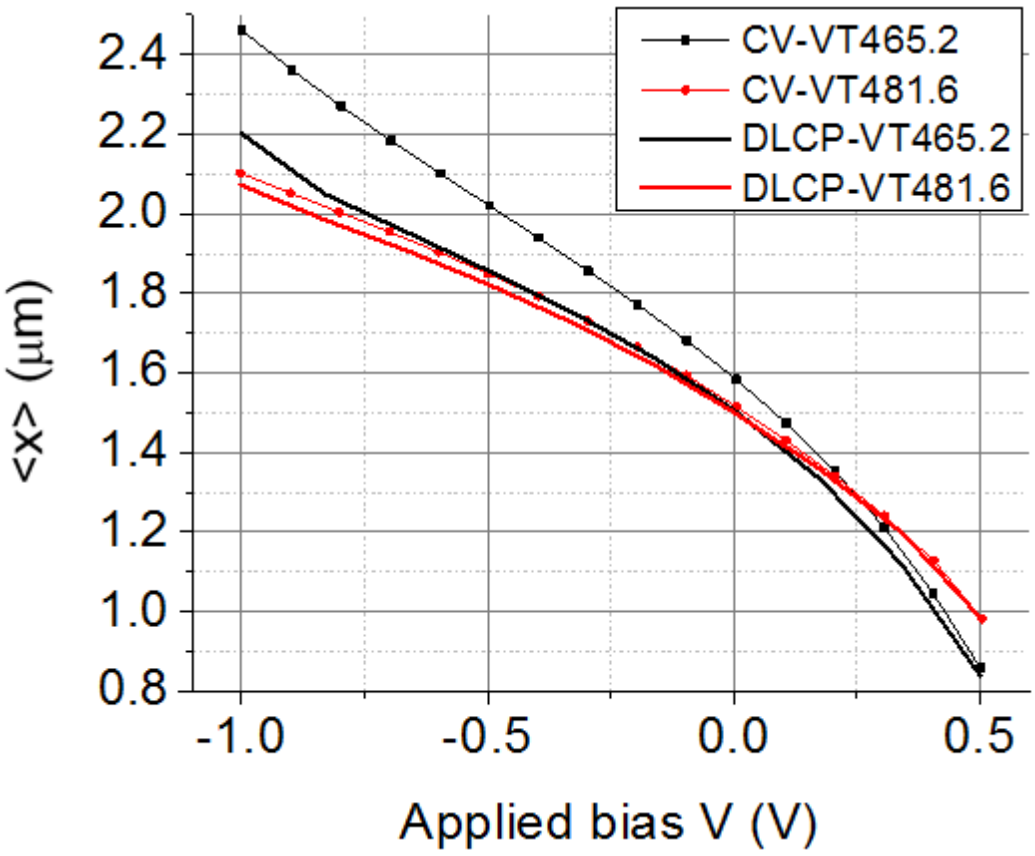


Figure 4-9: CV and DLCP space charge width estimates vs applied bias V of CdTe baseline samples chosen for characterization.

For both CV and DLCP measurements, the value of <x> decreases with applied bias across the CdS/CdTe p-n junction as increasing the bias shrinks the p-n junction space charge region, while agreement in <x> between CV and DLCP measurements is also observed to improve. This precision with increasing applied bias may be the result of a smaller volume of bulk defects which respond to the applied AC signal. However, the use of DLCP over CV is expected to be more accurate based on the sensitivity of bulk defect states, and hence exclusion of p-n junction interface states [55]. At a reverse bias of -0.5 V, <x>~2 μm, while at

equilibrium (V=0), <x>~1.5 μm. At a forward bias of 0.5 V, <x>~1 μm. Above an applied forward bias of 0.5 V, the impedance of the CdTe device is comparable to the 2 kΩ impedance of the bias adapter used to protect the LCR equipment during CV/DLCP measurements. The 2 kΩ external impedance is in series with the device, limiting any further increases in current and hence further increases in device voltage, thus limiting V_{device}~0.5 V.

In order to estimate the built in voltage V_0, fitting is performed on the DLCP <x> vs V data in Figure 4-9 using Eq. (2-29) with W→<x>.

$$< x >^2 = \frac{2\varepsilon(V_0 - V)}{qN_a} \tag{4-5}$$

V_0 is calculated by determining the values of the intercept $2\varepsilon V_0/qN_a$ and slope $-2\varepsilon V_0/qN_a$. The data is fit well over the range V=-0.5 to 0 V and shown in Figure 4-10.

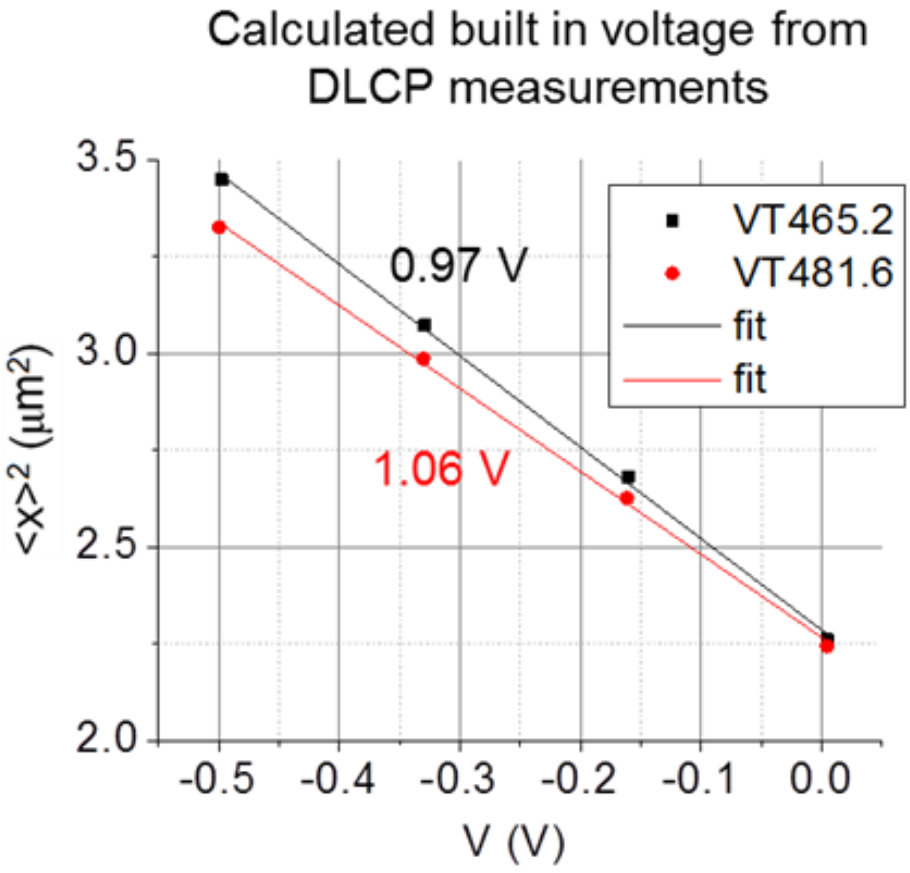


Figure 4-10: DLCP $\langle x \rangle^2$ data fit from -0.5 to 0V to Eq. (4-5) to determine built in voltage V_0 which is color coded to the specific sample.

The built in voltage of the baseline devices is determined to be ~1V which is consistent with previous findings on CdTe devices where built in voltage was measured from low temperature V_{oc}-T measurements [93].

4.4.2.2 Estimated Doping

An estimate of CdTe doping is taken by CV and DLCP by finding the respective minimum values of $N_{CV}(V)$ and $N_{DL}(V)$ (Eqs (2-34), (2-43)). However, by

comparing $N_{CV}(V)$ and $N_{DL}(V)$, the most reliable results of doping can be taken from DLCP (Figure 4-11).

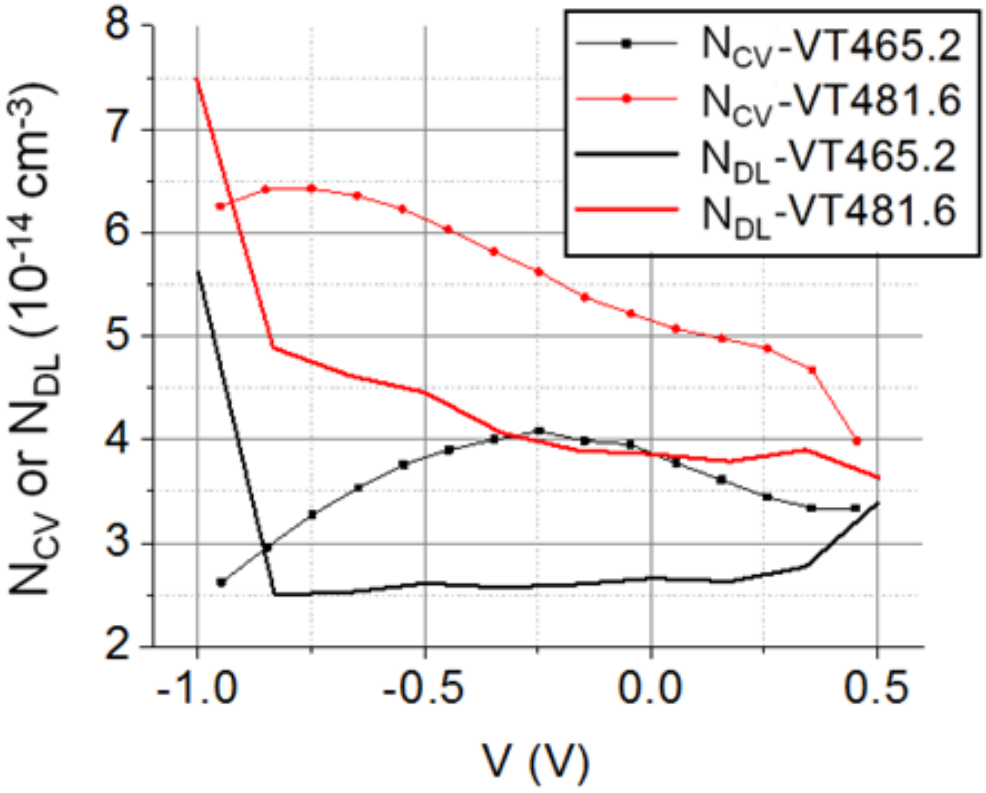


Figure 4-11: CV and DLCP measurements of N_{CV} (V) and $N_{DL}(V)$.

While the $N_{DL}(V)$ profile exhibits a U shape, this is not observed for $N_{CV}(V)$ which may be influenced by the p-n junction interface states or deep defect levels within but which does not give meaningful data of the free carrier concentration. At 300 ^{o}K, the upper limit to free carrier hole density is estimated by the minimum value of $N_{DL}(<x>)$ over the voltage and frequency range [61] [94]. Based on the minimum value of the U profile, DLCP measurements suggest CdTe doping on the order of 10^{14}

cm^{-3} which has been previously measured on thin film CdTe cells using the CV technique [18]. The increase in N_{DL} with forward and reverse bias has been argued to be influenced by the back contact of the device [61].

4.4.3 J-V-T-I

The use of current-voltage-temperature-light intensity (JVTI) measurements were utilized to obtain diode activation energy E_A using

$$V_{oc} = \frac{E_A}{q} - \frac{AkT}{q} ln \frac{J_{00}}{J_{sc}} \quad (4\text{-}6)$$

At temperatures around 240 ºK, nonlinear behavior of V_{oc} and T was observed. It is expected that as $T \rightarrow 0$, V_{oc} becomes independent of temperature, consistent with a maximum separation of quasi Fermi levels due to a dominant temperature independent recombination mechanism [93]. However, the relation between V_{oc} and T is linear in the temperature region 260-300 ºK which is used to extrapolate activation energy E_A. The best fits to the data were determined by separately determining values of E_A at each light intensity as opposed to the method of fitting V_{oc}-J_{sc}-T data using Eq. (4-6) with a single value of E_A, and least squares fit of $V_{oc}(E_A)$ The fits are shown in Figure 4-12.

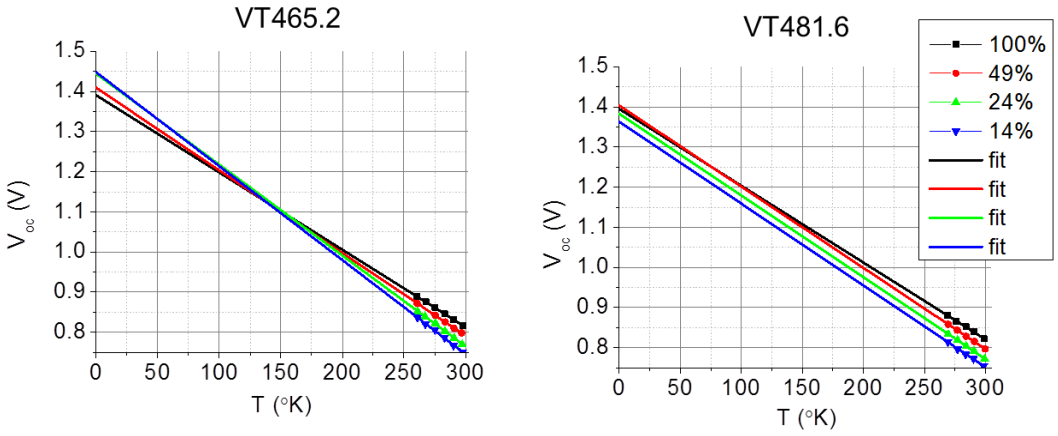


Figure 4-12: V_{oc} vs T taken at 100%, 49%, 24%, and 14% suns intensity for baseline cells with linear fits used to determine activation energy E_A.

For both samples, the activation energy E_A, taken as the intercept of V_{oc}-T (Eq. (4-6)) is summarized in Table 4-11.

Table 4-11: Activation energy E_A vs light intensity (100% = 1000 W/m^2) and CdTe thickness. SELH=1000 W/m^2, 300 ºK, ELH illumination.

Sample	t_{CdTe}	E_A (100 %)	E_A (49 %)	E_A (24 %)	E_A (14%)	V_{oc} (SELH)
	µm	eV				mV
VT465.2	7.3	1.39	1.41	1.44	1.45	816
VT481.6	4.2	1.39	1.40	1.38	1.36	822

For both samples, V_{oc}-T measurements taken from 490-1000 W/m^2 give consistent values of E_A=1.39-1.41 eV while E_A values at lower light intensities outside of this range may be the result of a light dependent recombination mechanism. For illumination intensity = 490-1000 W/m^2, the activation energy E_A on the CdTe devices is ~100 mV less than that of the 1.49 eV bandgap. If E_A=E_g, this would suggest that

V_{oc} was dominated by SRH recombination [85] [93]. However for $E_A<E_g$, this suggests the presence of another recombination mechanism influencing V_{oc}, possibly an interface mechanism [93]. It is possible that the magnitude of light intensity may vary the electric field profile across the device or at the interface. In order to measure the field profile as a function of light intensity, one approach would be the use of Kelvin probe force microscopy measurements across a CdTe device cross section [95] to analyze the electric potential of the device as a function of light intensity, where the device would be subjected to an illumination source of varying light intensity. This type of measurement is beyond the scope of this work.

A JV-temperature fitting analysis of the device VT465.2 device is performed using forward bias JV dark data and T<300 ºK to determine the back contact barrier between CdTe and Cu_2Te. The fitting analysis is described in Appendix C. A logarithmic/Arrhenius plot of $-\ln(J_t)$ vs 1/kT is performed with J_t as the turning or saturation current observed in CdTe devices during JV rollover [96]. Only meaningful data could be obtained from dark JV measurements since light measurements are complicated possibly by voltage dependent collection current. Figure 4-13 shows an Arrhenius plot of $-\ln(J_t)$ vs 1/kT.

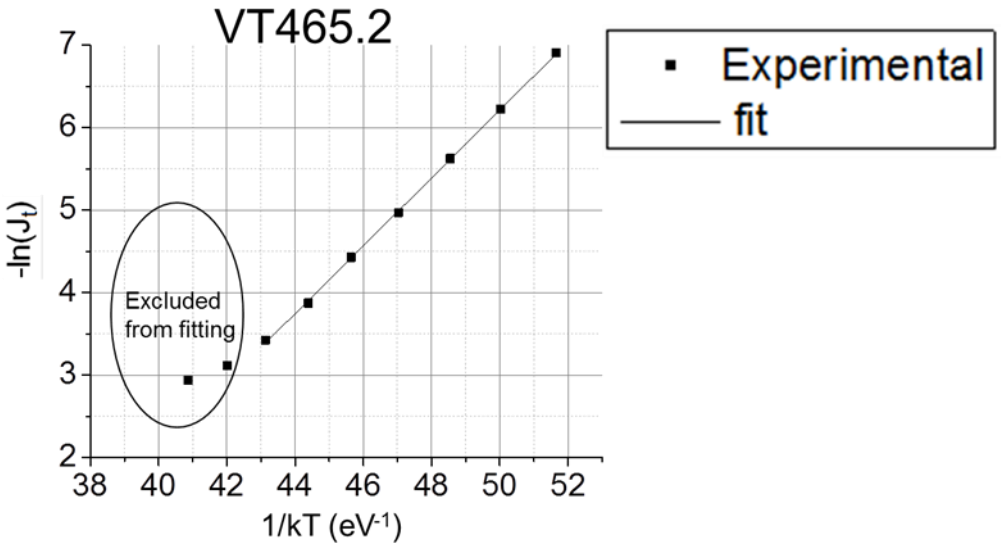


Figure 4-13: An Arrhenius plot of $-\ln(J_t)$ vs 1/kT used to determine the back barrier.

From the slope of the Arrhenius $-\ln(J_t)$ vs 1/kT plot in Figure 4-13, a 0.41 eV Cu back barrier is determined. This is consistent with previous measurements of the CdTe/Cu back barrier which have ranged from 0.3-0.5 eV [4], [97].

4.5 Conclusions

High efficiency 15% glass/TCO/HRT/CdS/VT-CdTe/Cu_2Te/Ni superstrate devices exhibiting FF>75% and V_{oc}>800 mV were previously developed in a joint effort by IEC and Corning by fabrication of a Corning-glass-C065/CTO/ZTO window stack. The C065 glass used for high efficiency devices exhibits the following crucial properties: 1.) low impurity; 2.) high strain point allowing for elevated VT CdTe processing temperatures up to 630 ºC; and 3.) well matched coefficient of thermal expansion to CdTe. Devices developed with a C065 glass exhibit diode factor performance A≤1.5 suggesting that the dominant recombination mechanism is not

SRH. In addition, the development of CdTe devices with a C065/CTO/ZTO window were previously found to exhibit minimal bulk CdTe stress compared to other alternatives of glass/TCO/HRT layers. CdTe devices with a C065/CTO/ZTO window stack exhibit optimal V_{oc} performance for VT processing temperature T_{ss}=590 ºC, resulting in V_{oc}=840 mV devices.

Two high V_{oc} performance C065/CTO/ZTO/CdS/CdTe/Cu_2Te/Ni devices (V_{oc}=820-840 mV) are characterized. Quantum efficiency measurements reveal a 1.49 eV bandgap and Urbach energy of 15 meV, where the 15 meV Urbach energy is larger than previous measurements of more highly ordered single crystal CdTe (7-9 meV) but similar to previous Urbach energy measurements on VT-CdTe devices (20 meV) through the use of a different measurement technique (transient photocapacitance). CV and DLCP measurements provide similar values of CdTe space charge width (~1.5 µm). DLCP measurements also suggest CdTe doping of ~10^{14} holes/cm^3, in agreement with previous polycrystalline CdTe CV measurements taken by external authors. However, the DLCP method, which utilizes higher order capacitance corrections due to deep defects as opposed to CV, appears to be more accurate in estimating bulk CdTe doping. The use of JVTI measurements suggests an interface recombination mechanism in CdTe devices with recombination activation energy E_A=1.36-1.45 eV < $E_{g,CdTe}$=1.49 eV. Dark JV-T measurements also imply a CdTe/Cu_2Te back barrier of 0.4 eV.

Chapter 5

THE EFFECT OF CDTE THICKNESS ON V_{OC}

5.1 Motivation

Theoretical modeling of CdTe devices predicts that if the CdTe bulk recombination volume is reduced by thinning the CdTe layer to a thickness comparable to the space charge width (1 μm), so that the back contact is the dominant recombination mechanism, then V_{oc} will be dependent on the back barrier (Chapter 3, section 3.2.4). The modeling predicts that if the device back contact is ohmic, a decrease in CdTe thickness should result in an increase in V_{oc}, providing that the material properties of the device are the same between a thin and thicker device. It is hence of interest to test this modeling by developing an experiment where V_{oc} can be tested on CdTe devices with fixed material properties, but which vary in CdTe thickness/recombination-volume, and which are contacted using an ohmic probe.

This chapter discusses the V_{oc} behavior of CdS/CdTe superstrate devices where the devices are thinned by etching the device in citric peroxide solution and the V_{oc} was evaluated as a function of CdTe thickness using a liquid junction quinhydrone-Pt (QH-Pt) probe [13]. Two different types of devices were characterized: those with Cu diffused into the CdTe bulk and those without a Cu treatment and the results are compared to theoretical simulations using SCAPS.

5.2 Experimental

This section describes the fabrication of thin CdTe devices and probing method.

5.2.1 Device Fabrication: Thinning and Cu Treatment

This section discusses the fabrication of thin CdTe devices with and without Cu where the CdS/CdTe deposition and $CdCl_2$ heat treatment was identical to that of baseline CdTe/Cu_2Te contact devices which had $V_{oc} \geq 800$ mV (section 2.1).

For one CdS/CdTe sample, the Cu diffusion step was eliminated from the baseline device process (section 2.1.5) which consisted of: 1.) a pre Cu bromine etch to remove oxides; 2.) deposition of 5 nm Cu; 3.) a heat treatment in argon at 180 ºC for 30 minutes. For the smple with the Cu treatment, and prior to V_{oc} probing, the Cu layer and an estimated 1 μm or less of CdTe was removed by etching in a citric peroxide (CPX) solution, consisting of 5% wt. citric acid to 15% hydrogen peroxide. The device was immered in the solution and wafted vertically for 10 s where the CPX solution is in kinetic motion to stoichometrically etch the CdTe layer. The CPX etching of CdTe has been previously documented as stoichiometric based on previous glancing angle XRD measurements taken on the CdTe surface before and after CPX solution etching where no differences in XRD peak positions were observed [98].

For both Cu free and Cu diffused CdTe devices, the thinning process of CdTe was applied between V_{oc} probing measurements. The samples were thinned as follows: 1.) a CdTe sample was placed on a horizontal surface and a 5 mm diameter drop of the citric peroxide (CPX) solution was placed on the CdTe layer for 5-30 s, in order to slowly etch the CdTe layer; 2.) then, the sample was then rinsed with deionized water and subsequently blow dried with argon. The slow CPX drop etch

was chosen over a kinetic vertical wafting etch to obtain numerous measurements of V_{oc} as a function of etch time.

Hence, the completed structures of baseline devices and devices used for CdTe thickness V_{oc} profiling are shown in Figure 5-1.

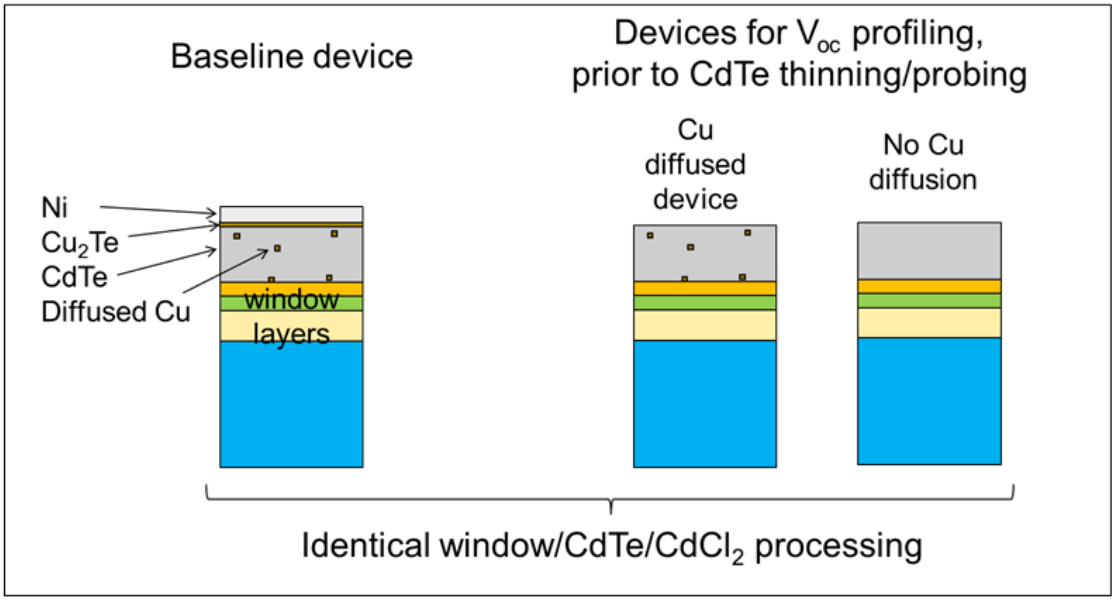


Figure 5-1: Device structures of baseline CdTe/Cu_2Te devices vs devices used for CdTe thickness V_{oc} profiling. The latter device structures are shown before CdTe thinning and V_{oc} probing.

Associated samples used for V_{oc} profiling are shown in Table 5-1.

Table 5-1: Samples with and without a Cu treatment used for V_{oc} profiling and baseline CdTe/Cu_2Te cell V_{oc}, as measured under AM1.5 conditions.

Sample	Cu treatment?	Baseline cell AM 1.5 V_{oc}(V)
VT438.7b	Y	803 (VT438.6)
VT461.8b	N	822 (VT461.6)

5.2.2 V_{oc} Probing: QH-Pt Testing

This section discusses the experimental quinhydrone-Pt probe technique and setup for determining V_{oc} of CdTe devices.

A liquid junction probe, instead of a solid-state contact, was employed using an aqueous solution of quinhydrone (PH=3-3.5) in contact with an inert Pt wire forms a non-reactive quinhydrone-Pt (QH-Pt) contact to CdTe. The aqueous quinhydrone solution is placed on the CdTe surface of a window/CdTe stack device. The QH-Pt contact to CdTe is a contact with + polarity. A contact with negative polarity is connected to the CdTe device indium/TCO contact. Both + and – contacts are connected to a voltmeter, and when the CdTe device is illuminated by an LED with 6 W/m^2 intensity, V_{oc} is measured. Because the quinhydrone probe results in an unstable measurement, for each probe/voltage measurement, the maximum voltage reading is taken within 3 seconds, after which the voltage reading is observed to decrease. The schematic of the QH-Pt setup is shown in Figure 5-2.

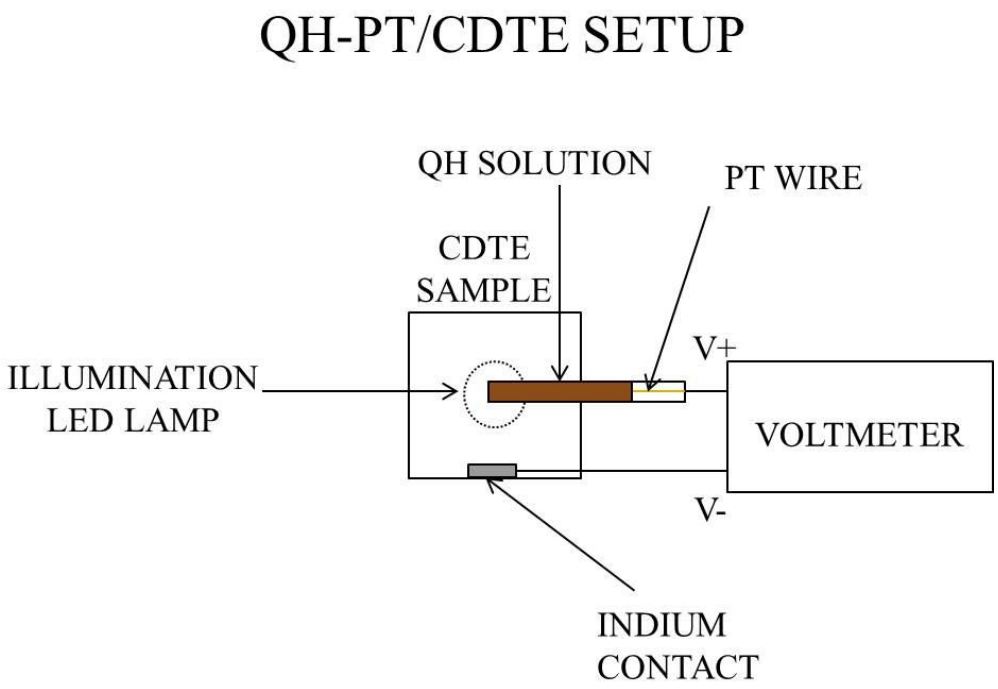


Figure 5-2: A schematic of the quinhydrone-Pt (QH-Pt) setup. The area of illumination on the CdTe sample is 1.1 cm^2, while the area of the QH-Pt probe in contact with the sample is 0.008 cm^2.

The effective area of the quinhydrone solution on the CdTe sample varies between the probe area (0.008 cm^2) and LED illumination area (1.1 cm^2). When light is applied to the CdTe sample, photocarrier generation occurs due to the CdTe absorber. Photogenerated carriers then transfer to the quinhydrone solution, which results in a redox reaction and subsequent charge buildup and voltage for the QH-Pt electrode. Assuming that the contact and bulk resistances of the voltmeter-Pt wire-quinhydrone solution are negligible, this results in V_{oc} which is induced at the CdTe/quinhydrone contact.

The advantages to the use of this method are: 1.) to measure V_{oc} without mechanically shunting the CdTe layer, and 2.) to repeatably measure V_{oc} before and after etching CdTe to determine the V_{oc}/CdTe thickness relationship without the complications of removing and reapplying a contact.

5.3 Results and Discussion

This section discusses the device V_{oc} results based on CdTe thinning for devices with and without a Cu treatment. The experimental V_{oc} for devices with thinned CdTe is also compared to theoretical SCAPS V_{oc} simulations based on CdTe thickness.

5.3.1 V_{oc} Based on CdTe Thinning and Cu Diffusion

This section discusses the results of V_{oc}(QH-Pt) profiling for Cu free and Cu diffused CdTe devices. Results are shown in Figure 5-3.

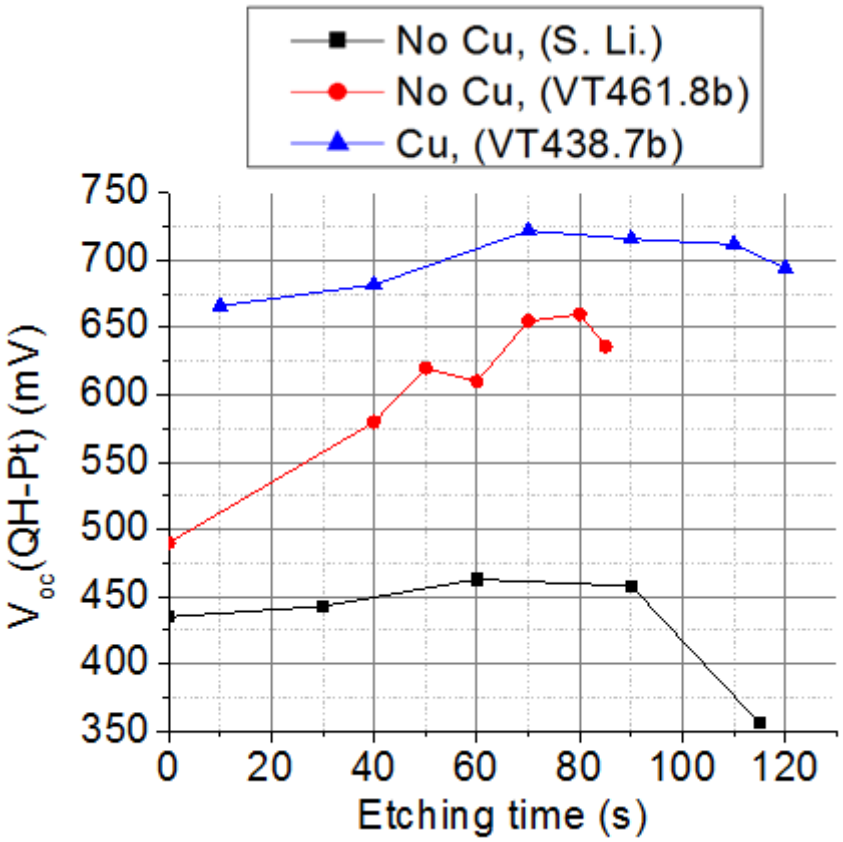


Figure 5-3: V_{oc}(QH-Pt) vs etching time of CdTe devices with and without Cu. For the sample VT461.8b, measurements of V_{oc} for 10s, 20s, and 30s are not included due to inconsistencies in collecting data from the unstable V_{oc} measurement. Since the sample VT438.7b was previously given a 10 s etch to remove the initial Cu layer, the initial value of V_{oc} is hence taken at 10 s.

Initial work on evaluating the effect of CdTe thickness on V_{oc} was performed on a Cu free CdTe sample by an undergraduate student, enrolled for research credits at IEC [99] where an optimal ΔV_{oc}=30 mV value was obtained. All measurements show an increase in V_{oc} with ΔV_{oc}=30-170 mV with the highest ΔV_{oc} taken from the Cu free sample VT461.8b.

For the Cu treated CdTe device, a higher initial V_{oc}(QH-Pt)=666 mV is observed, compared to that of Cu free thick CdTe samples with initial V_{oc}(QH-Pt)=490mV (5-3). This increase may be due to the CdTe doping of Cu, resulting in a more p-type CdTe bulk layer [44]. The optimally thinned Cu treated CdTe device exhibits V_{oc}(QH-Pt)=722 mV.

For the V_{oc} vs etching time profiles, a decrease in V_{oc} may suggest CdTe pinhole formation, a weak diode, or insufficient light collection within the CdTe absorber.

5.3.2 Estimates of Quinhydrone-Pt V_{oc} for AM1.5 Conditions

The best V_{oc}(QH-Pt) obtained for a thinned device is 722 mV, corresponding to the Cu diffused CdTe device VT438.7b. The baseline VT438.2 device exhibits V_{oc}(AM1.5)=803 mV in comparison. An estimate of the thinned Cu device V_{oc}(QH-Pt) at 1000 W/m^2 is calculated using

$$V_{oc} = \frac{AkT}{q}\ln(\frac{J_{sc}}{J_0}) \tag{5-1}$$

where

$$\delta V_{oc} = V_{oc}\left(1000\ \frac{W}{m^2}\right) - V_{oc}\left(6\ \frac{W}{m^2}\right) \tag{5-2}$$

$$\delta V_{oc} = \frac{AkT}{q}(\ln\frac{J_{sc,1sun}}{J_0} - \ln\frac{J_{sc,0.006suns}}{J_0}) \tag{5-3}$$

$$= \frac{AkT}{q}\ln\frac{J_{sc,1sun}}{J_{sc,0.006suns}}$$

where $J_{sc,1sun}$ and $J_{sc,0.006suns}$ are the respective values of J_{sc} measured at 1000 W/m^2 and 6 W/m^2. Assuming a linear dependence of J_{sc} with light intensity,

$$\ln\frac{J_{sc,1sun}}{J_{sc,0.006suns}} = \ln\frac{1000\,\frac{W}{m^2}}{6\,\frac{W}{m^2}} \approx 5.116 \tag{5-4}$$

Then,using Eqs. (5-3) and (5-4) and assuming room temperature conditions (300 ºK with kT/q≈0.0258 eV), the value of δV_{oc} is computed as

$$\delta V_{oc}(\mathrm{V}) = 0.132A \tag{5-5}$$

If A≥1, $\delta V_{oc} \geq 132$ mV. For the thinned Cu device (VT438.7b) the estimated V_{oc}(QH,Pt) taken at 1000 W/m^2 is

$$V_{oc}(Cu, QH-Pt, AM1.5) \geq 722mV + 132mV \geq 854\ mV \tag{5-6}$$

This is approximately 50 mV higher than the VT438.7b baseline V_{oc}(AM1.5,Cu_2Te)= 803 mV.

However, the approach of estimating V_{oc}(QH-Pt) for AM1.5 conditions using the model, Eqs. (5-1(5-6 is based on the assumptions of 1.) a dominant single diode p-n CdS/CdTe junction which may not hold for a nonplanar thinned CdTe device with various thickness regions (see section), and 2.) the absence of light dependent recombination which can affect the diode factor A and J_0. It would be of interest to perform a V_{oc}(QH-Pt) measurement on an optimally thinned Cu diffused CdTe device under AM1.5 conditions to test these assumptions. With a higher light intensity under AM1.5 conditons (1000 W/m^2 vs 6 W/m^2), such a measurement should result in a higher absorption of light into the thinned CdTe bulk, and subsequently higher V_{oc}(QH-Pt). The challenge however in performing V_{oc} probing at AM1.5 conditions on CdTe devices would be to illuminate and probe the device while controlling the

QH solution temperature to prevent evaporation of the liquid, or find another liquid junction contact.

While the CdTe layer is thinned, reducing the bulk CdTe recombination volume, the CPX etching produces a rough/nonplanar CdTe film. SEM/FIB measurements taken on a heavily etched sample (VT461.8b after 85 s etching time) reveal a CdTe film thickness ranging from 0 μm to the initial CdTe thickness (~6 μm). Hence, a meaningful value of CdTe thickness for an optimally thinned CdTe device cannot be determined.

5.3.3 Morphological Characterization of Thinned CdTe

The nonplanar behavior of CPX etching on various CdTe samples with resulting t_{CdTe} ranging from 0 μm to the film initial thickness (4-9 μm) has been observed regardless of the CPX etching technique utilized (kinetic vertical waft, ultrasonication, or horizontal drop) and may be related to smaller grains being etched at a quicker rate, compared to larger grains in the polycrystalline CdTe film. However, the method of placing a slow etching drop of CPX solution on the CdTe may also contribute to a nonplanar CdTe surface where t_{CdTe} is thicker near the outer radius of the drop than at the drop center.

The roughness of CdTe was characterized by surface profilometry and results are shown in Figure 5-4.

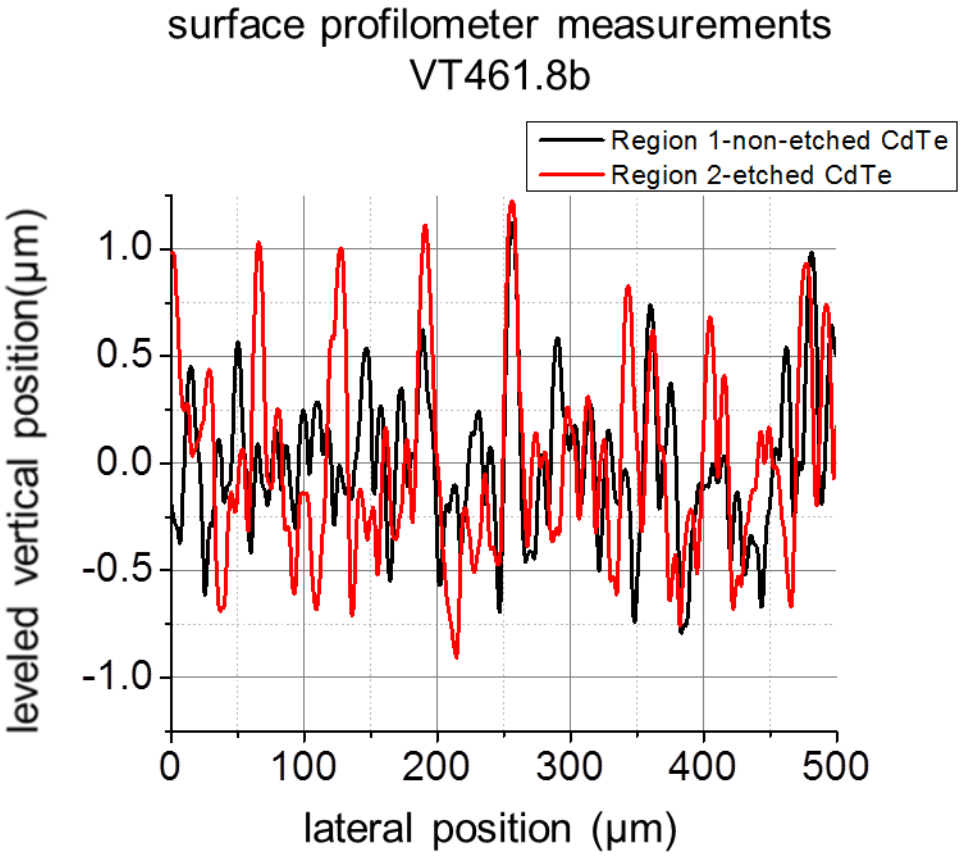


Figure 5-4: Surface profilometer measurements performed over non-etched and etched areal regions of the CdTe sample VT461.8b. The measurement taken on the etched CdTe region (region 2) was performed in the central CPX drop etched CdTe region (CPX drop region diameter≥1 cm).

The RMS film roughness is calculated as

$$RMS\ roughness = \sum_{i=1}^{N} R^2 \tag{5-7}$$

where R is the leveled vertical position and N is the number of measurements = 2000.

From surface profilometry scans, the CdTe RMS film roughness for the non etched

region (region 1) and etched region (region 2) is respectively 0.25 μm and 0.43 μm. While the higher RMS value for the etched CdTe surface (0.43 μm) is expected, the stylus tip diameter is probably on the order of several microns [100] and thus dominates the lateral resolution as opposed to the software lateral resolution of 250 nm. A more precise RMS measurement may be obtained with AFM.

5.3.4 SCAPS Simulations: Comparison to Experiment

SCAPS simulations of CdTe device V_{oc} vs CdTe thickness were performed using the baseline input parameters (Table 3-1) and the results are shown in Figure 5-5.

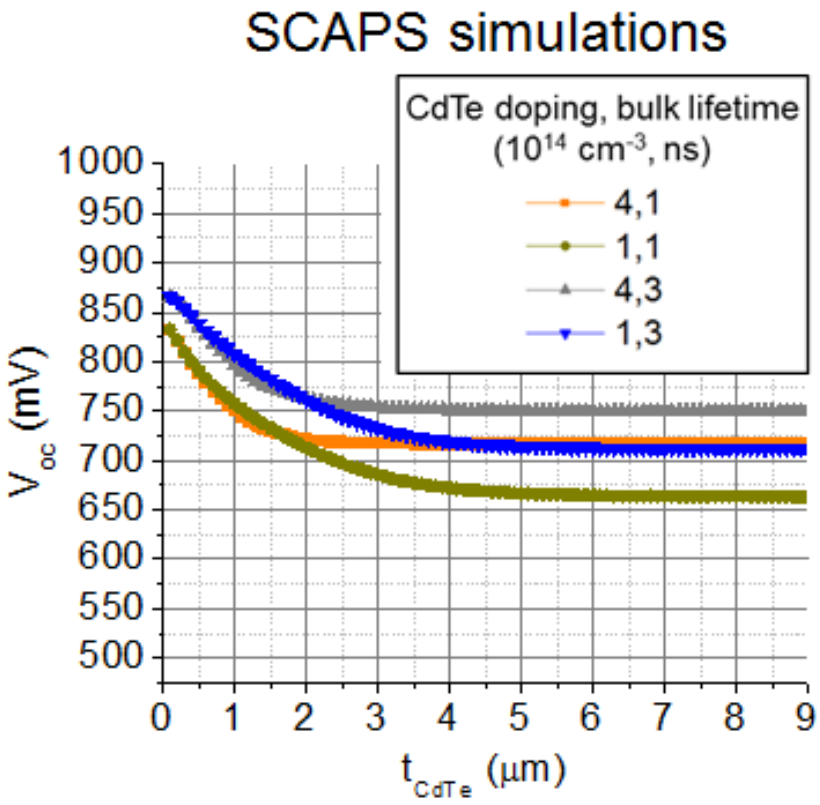


Figure 5-5: SCAPS simulations V_{oc} for single crystal CdTe devices with a well defined CdTe thickness. Simulations are chosen using a CdTe thickness ranging from 0.1-9.0 µm. For SCAPS simulations, an estimated CdTe doping of 1-4*10^{14} cm^{-3} is chosen, based on DLCP measurements of thick (t_{CdTe}=4-9 µm) CdTe devices V_{oc}>800 mV, while a 1-3 ns lifetime is observed in polycrystalline CdTe devices with V_{oc}=800-875 [13], [81]. A 6 W/m^2 illumination is based on the experimental apparatus used to probe CdTe V_{oc}, while back contact barrier Φ_b is assumed to be 0 eV.

The simulation predicts a V_{oc} increase of 120-170 mV for a thinned single crystal CdTe device with $t_{CdTe}\leq$3 µm. However, the simulated V_{oc} of the modeled CdTe devices is up to 150 mV higher than that of expcaerimental CdTe devices. The device transport and recombination physics of the modeling is different than that of experiment based for the following reasons: 1.) the actual CdTe devices, the CdTe

bulk layer is not only polycrystalline but also highly nonplanar with CdTe thickness ranging from 0 μm to the initial thickness (3-9 μm); 2.) the QH-Pt contact may not be purely ohmic if a voltage offset exists between CdTe and quinhydrone or quinhydrone and Pt. A 2-D model of the nonplanar CdTe film might be needed for more accurate V_{oc} simulations which could be accomplished by a software package such as Sentaurus but is beyond the scope of this work.

As the CdTe thickness $t_{CdTe} \rightarrow 0$, no decrease in V_{oc} is observed as might be expected from a decrease in CdTe light absorption/collection. A decrease in CdTe absorption results in the simulated collection current $J_{sc} \rightarrow 0$ as expected. However, at low intensity (6 W/m^2), as $t_{CdTe} \rightarrow 0$, the decrease in CdTe recombination volume and subsequent influence of the ohmic back contact dominates collection current losses, resulting in a V_{oc} increase. This is not observed for higher light intensity conditions of 1000 W/m^2 where $t_{CdTe} \rightarrow 0$ results in a higher influence of current collection (J_{sc}) losses on the V_{oc} vs t_{CdTe} behavior resulting in an optimally maximum simulated V_{oc} for $t_{CdTe} \leq 0.5$ μm, (not shown).

For weakly doped CdTe (doping=10^{14} cm^{-3} and lifetime=3 ns), the simulated V_{oc} vs t_{CdTe}=0.1-2 μm exhibits a linear trend. For experimental V_{oc} vs etching time data on Cu free CdTe (VT461.8b, Figure 5-3), a linear trend in the data is also suggested from 0-80 s etching time. While the doping of the Cu free VT461.8b sample is not known, a Cu free VT deposited CdTe film given a $CdCl_2$ treatment is expected to be weakly doped on the order of 10^{14} cm^{-3} [13]. However, an experimental relation between CdTe thickness and etching time cannot be determined due to the nonplanar CPX etch. In order to more accurately test the simulated SCAPS V_{oc} vs t_{CdTe} with experiment, a planar thinning CdTe method would be needed.

5.3.5 Attempt to Improve Thinned CdTe Devices: Photoresist Technique

A future experiment to improve on V_{oc} profiling of CdTe would be a method to develop a uniformly thinned CdTe layer prior to V_{oc}(QH-Pt) measurements where: 1.) the use of a planar etch of CdTe such as Br:Me is used to produce a thin/smooth CdTe layer ≤1 μm followed by; 2.) the use of polishing/removal of the resulting Te rich layer to form a CdTe surface and a subsequent; 3.) photoresist technique to plug resulting pinholes [101].

To date, the latter photoresist (PR) technique has not been successful at plugging pinholes on etched/thinned window/CdTe samples with CdTe thickness ~1 μm (structure= glass/CTO/ZTO/CdTe/PR/Ni). The photoresist treatment-test was applied as follows: 1.) deposition of 1 μm thick negative NR9g photoresist (spin speed=3000 rpm) on a CdTe surface, followed by; 2.) photoresist solvent evaporation using a 3 min, 110 ºC air anneal; then 3.) a dose of 300 mJ/cm^2 of 400 nm UV light, incident through the glass side of the CdTe, which is used to cure photoresist in the CdTe pinhole areas; 4.) a secondary photoresist bake of (3 min, 110 ºC air anneal) used to improve photoresist stability; 5.) removal of uncured photoresist on the CdTe surface which, due to the CdTe UV light absorption is unexposed to the UV light dose and is easily removed by immersion and agitated motion of the sample in a developer solution RD6 (10 s vertical waft); 6.) deposition of 50 nm Ni. When a CdTe-free glass/CTO/ZTO window structure is given the above photoresist treatment (steps 1-6), resulting in a glass/CTO/ZTO/PR/Ni structure, resistance measurements on the Ni contact result in no observable shunt conductance and hence the photoresist film is insulating. However, devices developed using the above photoresist treatment (steps 1-6), resulting in a glass/CTO/ZTO/CdTe/PR/Ni exhibit high shunt conductance G>>1

mS/cm^2, suggesting Ni shunting through the CdTe layer and partial pinhole filling as observed by SEM areal images of the CdTe film

5.4 Conclusion

The effect of CdTe thickness on V_{oc} has been evaluated in this work for Cu free and Cu diffused CdS/CdTe devices using a quinhydrone-Pt probe setup under weak illumination of 6 W/m^2. The V_{oc} increased in Cu free CdTe devices by 170 mV where the measured CdTe thickness varied from 6 to <1 μm due to the non-uniform etching of the CdTe. The thinned CdTe devices treated containing Cu had a higher maxium V_{oc}(QH-Pt)=722 mV and the change from non-etched V_{oc} to the maximum was 56 mV. However, while the CPX etch is stoichiometric, the etching solution and horizontal drop CdTe etching method results in a nonplanar CdTe film and such a technique is problematic for the purpose of obtaining a relation between t_{CdTe} and V_{oc}.

Chapter 6

CDTE SOLAR DEVICES WITH A PCBM BACK CONTACT

6.1 Motivation

C_{61}-butyric acid methyl ester or PCBM is an electron acceptor fullerene material used in bulk heterojunction organic solar cells, which separates photogenerated bound excitons at a polymer/PCBM interface and transfers electrons to a cathode. PCBM is a stable material which is easily deposited via spin coating, typically using a chlorobenzene (CBZ) solvent. While current literature on PCBM is often limited to experiments/discussions on its use as a polymer/fullerene mixture, physical property information on pure PCBM is available regarding, structural, thermodynamic, optical, and electrical properties. These have been recorded as shown in Table 6-1.

Table 6-1: PCBM physical properties.

Property	Value	Reference
Mass density	1.25-1.5 g/cm^3	[102], [103]
Crystal structure	Depends on blend type, anneal	[104], [105], [106]
Melting temperature	250-300 ºC	[107], [108]
HOMO-LUMO gap	2.0 eV	[109]
Absorption coefficient	$\alpha(\lambda=700\text{ nm})= 10^5$ cm^{-1}	[110]
Index of refraction	1.8-2.2 (λ=400-900 nm)	[111], [112]
Single crystal electron mobility	0.04-0.3 cm^2/Vs	[113]
Film electron mobility	10^{-3} cm^2/Vs	[114], [115]
recombination rate	$\leq 10^{-18}$ m^{-3}s^{-1} (PCBM powder)	[113]
Valence band energy	5.8 eV	[109]

As previously stated (section 1.3.2), an ohmic contact to CdTe requires a material with a work function

$$WF_{contact} \geq E_{v,CdTe} = 5.8 - 6.0 \text{ eV} \quad (6\text{-}1)$$

assuming a 4.3-4.5 eV CdTe electron affinity [24], [25], [79] and 1.5 eV bandgap. The contact material should also exhibit a bandgap

$$E_{g,contact} \geq 1.5 \text{ eV} \quad (6\text{-}2)$$

to reflect electrons photogenerated within the CdTe layer from recombining at the back barrier [31]. Hence, the electronic band properties of PCBM make it a candidate material to test as a contact to CdTe based on 1.) the 5.8 eV PCBM valence band, which would imply a 5.8 eV work function material if the PCBM film could be developed p-type and 2.) a HOMO-LUMO gap ≥ 1.8 eV which suggests a PCBM bandgap ≥1.8 eV.

In this work, the structural and optical properties of PCBM prepared using both chloroform (CFM) and ethylenediamine (EDA) blends are characterized and compared and are evaluated as a primary solid junction contact for CdTe solar cells. A device with a PCBM contact is compared to a baseline device utilizing a Cu_2Te primary contact.

6.2 Experimental

PCBM films were prepared from CFM or EDA solutions of PCBM by spin coating at speeds from 500 to 5000 rpm for 50 sec and were deposited on soda lime glass (SLG) with and without ITO, c-Si wafers coated with ITO and as a contact on CdTe device structures. The surface morphology and through film structure and thickness of the PCBM films were evaluated by SEM using a) JSM-7400 for PCBM and b) Zeiss Auriga 60 CrossBeam workstation for FIB cross section measurements. The optical properties of the films where characterized by transmission and reflection measurements using a Perkin Elmer Lambda 750 spectrophotometer and the index of refraction and extinction coefficient were determined using a JA Woollam variable angle spectroscopic ellipsometer (VASE) where the PCBM films were grown on a c-Si/SiO_2/ITO substrate. For the analysis, the thickness and n, k values for ITO were determined assuming an infinite Si layer and a 1.5 nm SiO_2 layer prior to the deposition of the PCBM film. The PCBM ellipsometry data was modeled using a B-Spline layer for thickness and roughness-approximated by 50 % void content and a Tauc-Lorentz general oscillator was used to make further refinements in determining the n, k values [48]. CdTe solar cells were prepared using a baseline vapor transport (VT) deposition process discussed previously (section 2.1.3) and had a structure of: C065/Cd_2SnO_4/Zn_2SnO_4/CdS/CdTe/contact. Prior to the contact formation, the CdTe

structure was annealed in $CdCl_2$, followed: 1) a bromine methanol (Br:Me) etch of the CdTe surface to form a Te-rich surface layer; 2) deposit 5 nm of Cu by e-beam; 3) 180 °C Ar heat treatment for 30 minutes to diffuse Cu into the CdTe layer; and 4) Br:Me etch to eliminate excess copper. For the baseline cells, a Cu_2Te/Ni contact was used and the typical efficiencies of the devices were over 15%. To evaluate the PCBM films the CdTe structure was prepared using the baseline process up to the contact. For PCBM devices, the CdTe surface was etched in a citric peroxide (CPX) solution to remove excess Cu which also reduces the thickness of CdTe by ~2 μm.

6.3 Results and Discussion

This section discusses the morphological and optical characteristics of PCBM as well as the performance of CdTe/PCBM devices.

6.3.1 Growth and Characterization of PCBM Films

PCBM films were deposited on SLG and SLG/ITO using EDA and CFM blends for fixed time at spin speeds of 1000 and 5000 rpm. For the growth of PCBM:CFM films, a saturated solution of 30 mg/ml was used and films were deposited at 5000 rpm on SLG and 1000 rpm on SLG/ITO since at slower speeds particle agglomeration of PCBM was observed in the films. The films were annealed at 100 ºC to remove the CFM and Figure 6-1 shows SEM images of the PCBM films deposited on both substrates where the thickness was estimated from the cross section. The structure of the films is independent of the substrate and the PCBM on the SLG/ITO substrate is ~70% thicker due to the surface tension and spin speed. For the growth of PCBM:EDA films, the concentration of the blend was varied from 3 to 100 mg/l with spin speeds of 1000 and 5000 rpm to try to control the film structure and

morphology. The films were in general non-uniform with a rough surface and highly porous independent of the growth conditions. The films were annealed at 100 ºC to remove the EDA and Figure 6-2 shows SEM images of the films using different growth conditions. The difference in the film structure between the CFM and EDA films is due to the higher viscosity and lower vapor pressure of the EDA over that of CFM which results in slower solvent evaporation after spin coating and drying.

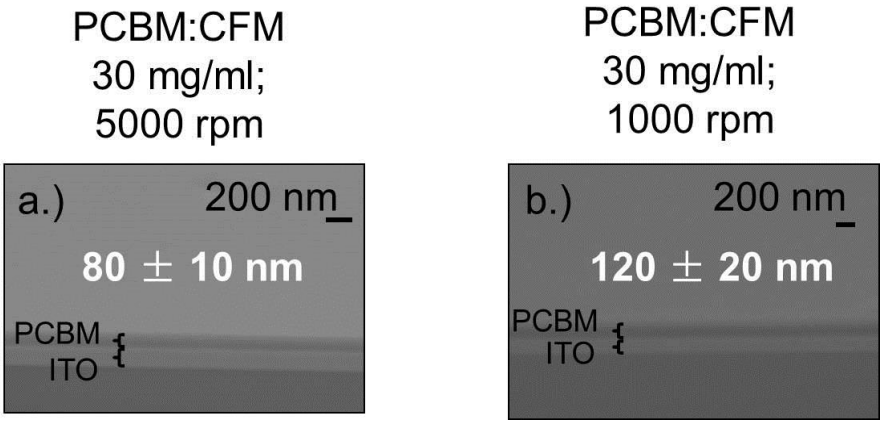


Figure 6-1: SEM images of PCBM:CFM deposited on ITO as a function of deposition conditions. PCBM thicknesses are shown in white. © [2014] IEEE [116].

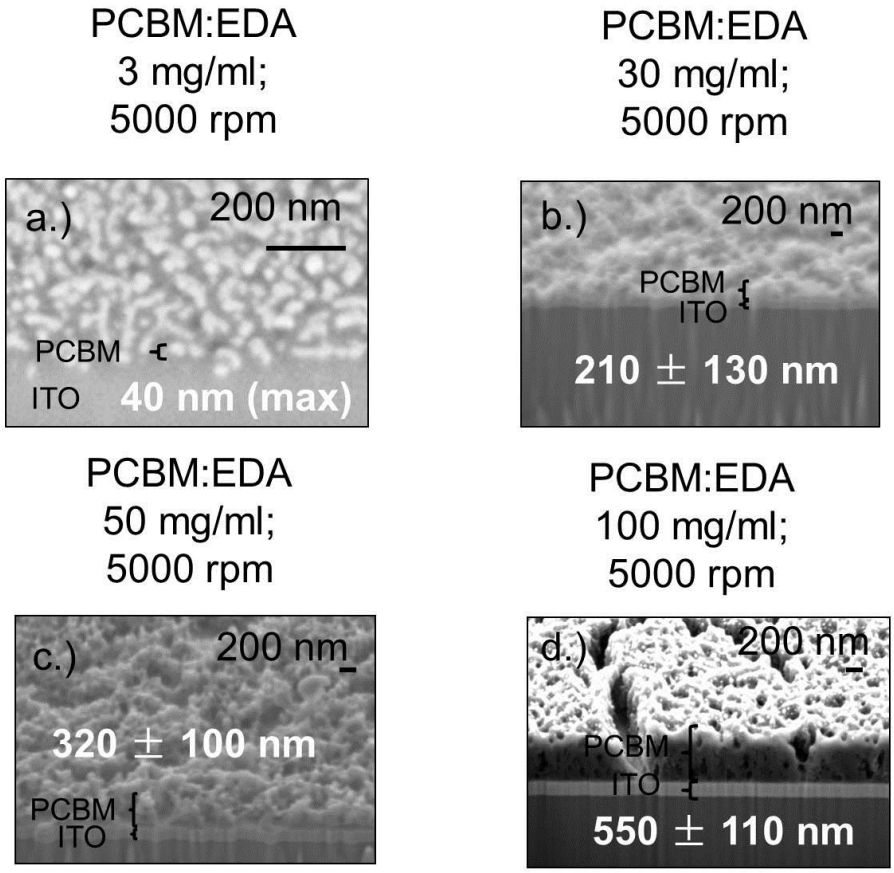


Figure 6-2: SEM images of PCBM:EDA deposited on ITO as a function of deposition conditions. PCBM thicknesses are shown in white. PCBM thickness is determined by: 1.) estimating the PCBM cluster size (a); or 2.) taking the mean and standard deviation of several cross sectional measurements (b.-d.). © 2014 IEEE [116].

The optical properties were characterized by reflection & transmission and VASE measurements of films deposited on SLG. For each measurement, a derivation of the PCBM bandgap is discussed as follows. For T&R measurements, an incident beam of light with wavelength λ and intensity I_0 transmits perpendicular to the

SLG/PCBM structure and is incident on the SLG side of the structure. Assuming that the dominant mechanisms affecting the transmission of light are: 1.) reflection from an effective 2 medium interface with resulting intensity I_1, and 2.) absorption in the PCBM bulk with resulting intensity I2, the transmitted light intensities I_0, I_1, I_2, resulting ratio of transmitted light T and resulting ratio of reflected light R are related as,

$$I_1 = (1 - R)I_0 \tag{6-3}$$

$$I_2 = I_1 e^{-\alpha x} \tag{6-4}$$

$$I_2 = I_0(1 - R)e^{-\alpha x} \tag{6-5}$$

$$T = \frac{I_2}{I_0} \tag{6-6}$$

$$\frac{T}{(1 - R)} = e^{-\alpha x} \tag{6-7}$$

with T and R both measured while α is the PCBM absorption coefficient, and x is an effective bulk PCBM optical length. Figure 6-3 shows the absorption of the PCBM:CFM and PCBM:EDA films at different anneal temperatures. There is no significant change in the ~50 nm PCBM:CFM with temperature while for the thicker PCBM:EDA film, there is measurable change after the high temperature anneal.

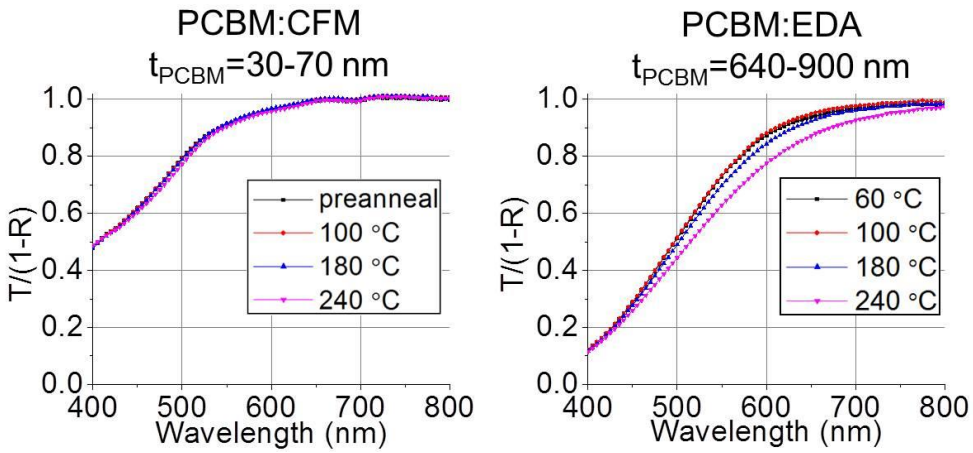


Figure 6-3: T & R measurements for PCBM films prepared by CFM and EDA blends after various anneal temperatures.

For PCBM:CFM, T & R results are consistent with previous results of transmission measurements taken of 50 nm PCBM prepared with chlorobenzene [117]. However, films grown with a PCBM:EDA blend do not show a clear absorption onset which may be due to light scattering from the PCBM layer since SEM/FIB revealed the film to be rough/porous. After annealing at 240 °C, there is a slight change in transmission and reflection in the PCBM:EDA film which may result from a change in the film morphology.

The bandgap of the films was estimated from evaluating $(\alpha E)^n$ verses E where n is 2 for a direct bandgap and 0.5 for an indirect bandgap where from Eq. (6-7)

$$\alpha x = -ln(\frac{T}{1-R}) \tag{6-8}$$

The best fit was found assuming negligible scattering and constant optical path length to be for an indirect E_g and Figure 6-4 is a plot of $(\alpha E)^{0.5}$ verses E for both EDA and CFM where the intercept is E_g,

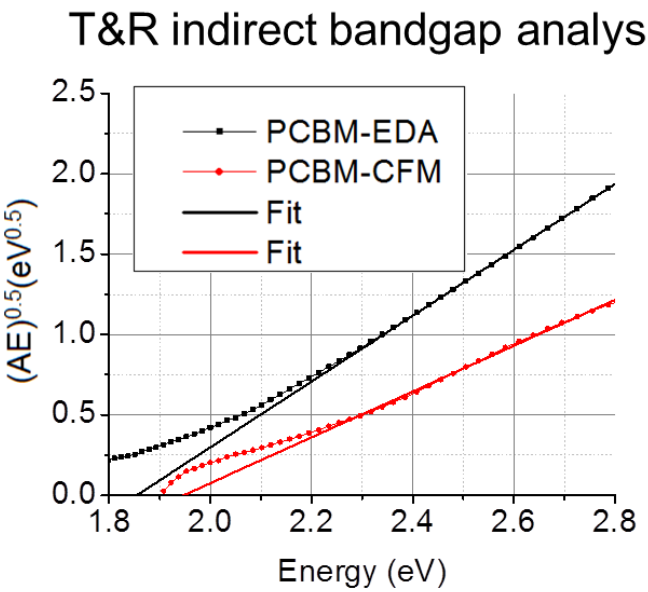


Figure 6-4: Indirect bandgap calculations for PCBM:EDA, and PCBM:CFM ,blends annealed at 100 °C with A=αx. The estimated bandgap are from linear fits of the data from 2.4-2.8 eV with the color corresponding to the respective T&R measurement.

The PCBM bandgap varies between 1.85-1.95 eV depending on the blend type. However, the modeling assumes a constant optical path length x(λ) which may not be the case for the rough/porous PCBM:EDA film and hence may explain the 0.1 eV bandgap discrepancy for the two films. While the spin coating method limits the thickness of smooth PCBM:CFM films deposited on SLG to ~50 nm, thicker PCBM:CFM films of 150 nm on Si/SiO_2/ITO have been analyzed via the use of VASE measurements.

VASE measurements of Si/ITO/PCBM:CFM samples where the PCBM film thickness was ~ 90-150 nm, were performed to evaluate the optical constants, n and k thickness, and bandgap. Only the PCBM films deposited from CFM were evaluated since films deposited from an EDA solution were too porous to obtain meaningful results. Figure 6-5 shows the n and k values as function of wavelength and results are compared to those reported by Hoppe and Zhokhavets for PCBM films grown from chlorobenzene (CBZ) solution [111], [112]. The k values are similar for the results presented here and those of Zhokhavets with ~5% difference compared to Hoppe. There is also reasonable agreement between the thickness measured by SEM cross section compared to the thickness by VASE and is summarized in Table 6-2.

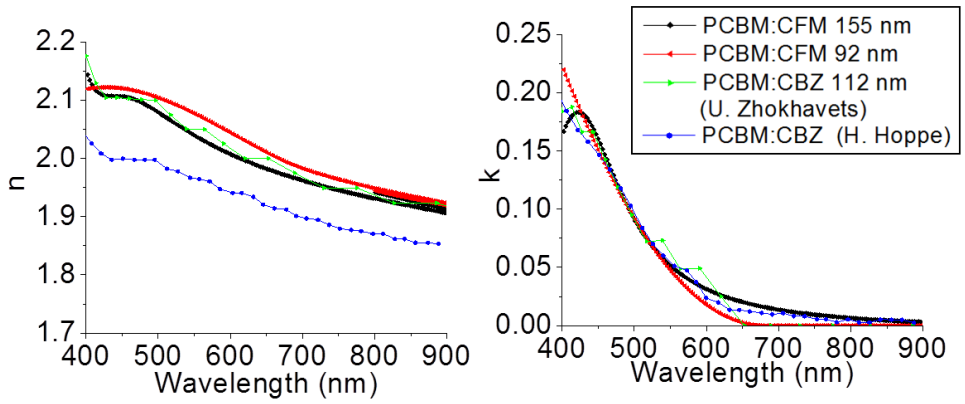


Figure 6-5: Optical n and k values calculated via ellipsometry. Measured VASE thicknesses are indicated in the figure above. Values are compared to data taken by external authors who used a PCBM:CBZ blend [112], [111]. © [2014] IEEE [116].

Table 6-2: Thickness meaurements of PCBM blends on ITO substrates.

PCBM carrier	PCBM conc. (mg/ml)	Spin speed (rpm)	VASE MSE	VASE t_{PCBM} (nm)	SEM t_{PCBM} (nm)
CFM	30	1000	8.6	155	120 ± 20
CFM	30	5000	5.6	92	80 ± 10

Using the k values from PCBM:CFM and PCBM:CBZ films (U. Zhokhavets [111]) and the relationship $\alpha=4\pi k/\lambda$ the bandgap was evaluated and Figure 6-6 shows the plots for an indirect E_g.

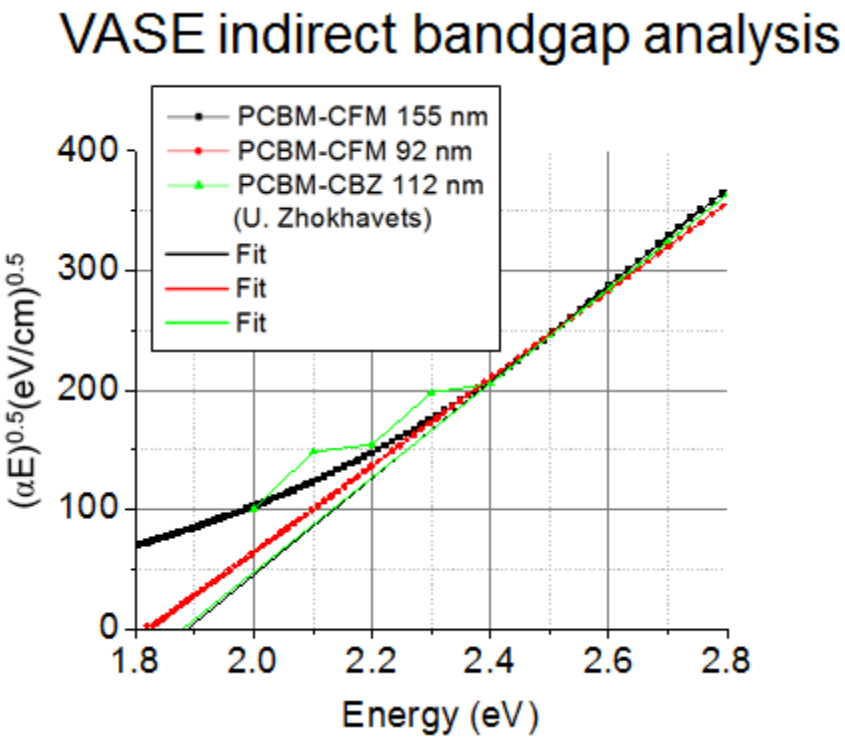


Figure 6-6: Indirect bandgap calculations for PCBM:CFM, and PCBM:CBZ blends with the respective optical measurement technique. Theoretical fits, used to estimate the bandgap are shown using straight lines from 2.4-2.8 eV with the color corresponding to the respective VASE measurement. Fitting is performed from 2.4-2.8 eV.

For the data in Figures 4 and 6, extrapolated bandgap data is summarized in Table 6-3 with sample thickness based on SEM (T&R measurements) and VASE.

Table 6-3: Estimated PCBM bandgap based on blend.

Blend	Measurement	t_{PCBM} (nm)	Bandgap (eV)
EDA	T&R	660-900	1.85
CFM	T&R	30-70	1.95
CFM	VASE	153-155	1.89
CFM	VASE	92-94	1.83
CBZ	VASE	112	1.88

Bandgap measurements on PCBM films hence reveal a value of 1.83-1.95 eV. A 1.83-1.95 eV PCBM bandgap is consistent with the measured PCBM HOMO-LUMO gap of 2.0 eV. No correlation is seen with PCBM thickness and bandgap.

The bandgap type of PCBM as indirect is also consistent with the assertions of de Haas, et al [113] which were based on the use of time-resolved microwave conductivity to determine a PCBM recombination rate of 10^{-18} m^3s^{-1}. It was asserted that this value was lower than expected for a charge recombination process based on diffusion, implying an indirect bandgap.

6.3.2 CdTe/PCBM: Morphology and Devices

PCBM was evaluated as the primary contact for CdTe cells where the current carrying contact was Pt. The surface coverage of PCBM on VT deposited CdTe was determined from backscattering electron imaging and 100% coverage could only be obtained using the EDA blend (Figure 6-7).

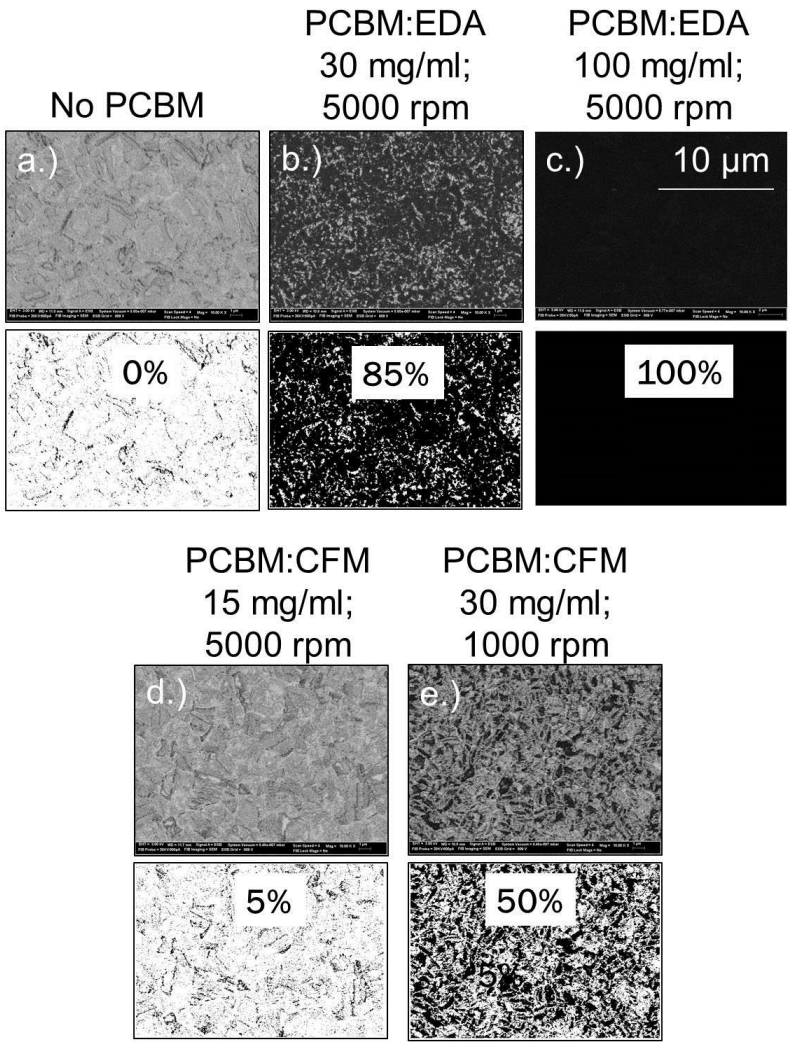


Figure 6-7: Backscattering and corresponding binary images of PCBM deposited on CdTe as a function of PCBM blend and deposition. For a.)-e.), backscattering images are placed below the PCBM deposition conditions, with corresponding binary images placed below the backscattering image. All images are scaled to 10 µm as shown above. © 2014 IEEE [116].

In contrast to PCBM deposited on smoother substrates of SLG (not shown) or SLG/ITO (Figures 6-1 and 6-2), PCBM deposited on CdTe is more nonuniform and discontinuous due to the rough surface of the citric peroxide etched, and

polycrystalline CdTe surface. Backscattering electron image (BEI) measurements of CdTe/PCBM at fixed contrast and brightness conditions reveal the uniformity/area coverage of PCBM on the etched, polycrystalline CdTe surface where images are shown as a function of solution carrier, solution concentration and spin coat speed. In order to approximate the PCBM coverage area, backscattering images were converted to binary images and the coverage area estimated from the ratio of black pixels to the total number of pixels in the image. Using grayscale values of 1-256, a pixel is defined as black if it has a grayscale value less than 115. Given the higher average atomic number of CdTe compared to PCBM, this data gives an estimate of PCBM coverage on VT deposited CdTe at various spin coating conditions. Table 6-4 summarizes the coverage obtained by backscattering/binary image analysis of the PCBM films and estimated thickness from SEM cross section.

Table 6-4: PCBM deposition conditions vs. PCBM coverage on VT deposited CdTe. Thickness was determined from SEM/FIB cross sectional measurements on CdTe/PCBM samples, by observing the minimum and maximum height of the PCBM layer. © 2014 IEEE [116].

PCBM carrier	Soln. conc. (mg/ml)	Spin speed (rpm)	Coverage (%)	Thickness (nm)
EDA	30	5000	85	0-400
EDA	100	5000	100	180-950
CFM	15	5000	5	indeterminate
CFM	30	1000	50	0-130

CdTe solar cells with a PCBM contact were fabricated and compared to a base line process which used a Cu_2Te/Ni back contact. The processing steps for the preparing the device were identical up to formation of the contact. For the PCBM device, prior to PCBM deposition, the CdTe surface was stoichiometrically etched in a CPX solution to remove the Cu_2Te back barrier which forms after Cu deposition and subsequent 180°C heat treatment. The CPX etch also reduced the thickness of CdTe by ~2 μm which could decrease/increase V_{oc} depending on whether the contact is Schottky/ohmic (section 3.2.4). The PCBM was deposited on the surface followed by a Pt contact that defined the device area and provide a current carrying contact. Figure 6-8 shows the JV curve for baseline cells with a Cu_2Te/Ni contact, and cells with a PCBM:EDA with estimated 100% PCBM coverage and Pt contacts.

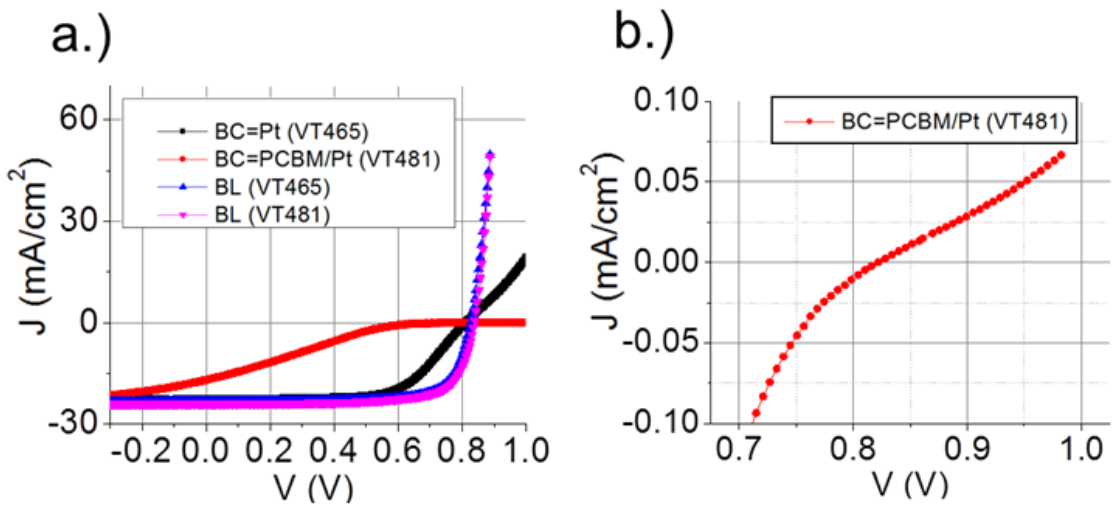


Figure 6-8: a.) AM1.5 device J-V behavior of CdTe cells with BC=PCBM/Pt in comparison to baseline (BL) cells with BC=Cu_2Te/Ni. b.) A zoomed in portion of the PCBM/Pt JV behavior showing V_{oc}. Cells with the same VT run number have identical processing steps except for the back contact. © [2014] IEEE [116].

CdTe cells with a PCBM back contact exhibit blocking behavior as noted by the losses in FF and J_{sc}. For cells with 100 % coverage and a PCBM:EDA blend, efficiency ≈ 3%, and V_{oc}= 822 mV a -18 mV difference from the baseline cell with V_{oc} =840 mV. The blocking behavior in the JV curves with increasing PCBM coverage shows that PCBM does not form an ohmic contact.

To estimate the CdTe/PCBM blocking barrier, the method of McCandless et al [4] was used as follows: 1.) JV-T measurements were made only over a narrow range from 90-120 ºC on a PCBM cell with 100% coverage since at lower temperature there was roll over in the forward bias region of the J-V curve, 2.) the series resistance R_s was determined from the slope of the J-V curve at forward bias and Figure 6-9 is a log

plot of R_s vs. 1/kT where the slope gives an estimate of the back contact barrier height of 0.6 eV.

.

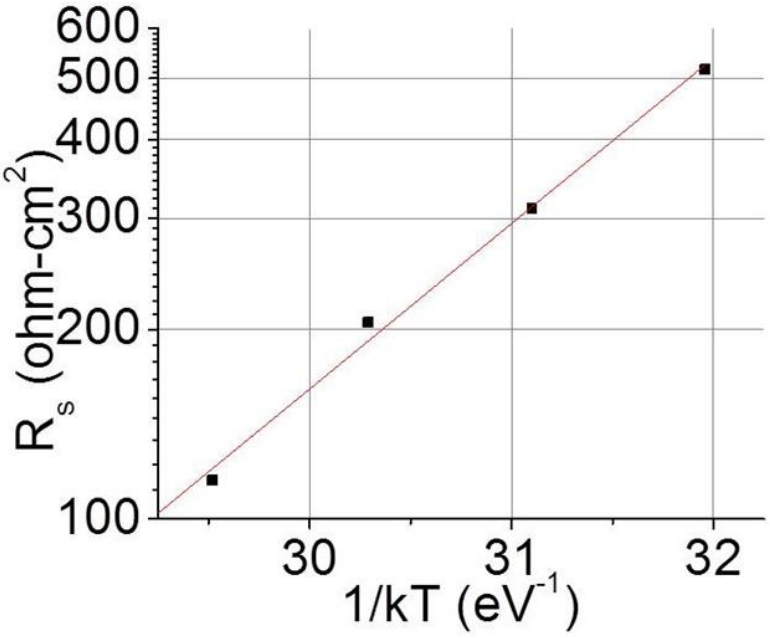


Figure 6-9: Series resistance vs. 1/kT for a PCBM cell with 100% coverage. © [2014] IEEE [116].

Assuming 1.) that the blocking behavior is not a result of interface defects between CdTe and PCBM, 2.) CdTe and PCBM valence band of 5.8 eV, and 3.) PCBM band gap of 1.8-2.0 eV, this suggests that Φ_{PCBM} = 5.2 eV, 0.6 eV Fermi level above the valence band which would make the material weakly p-type. Then, doping the PCBM could potentially push the work function to 5.8 eV, hence making the contact ohmic.

6.4 Conclusion

Material characterization of PCBM and analyses of device performance for CdTe cells with a PCBM contact have been presented. PCBM films produced with EDA are rough and porous while films produced with CFM are much smoother in comparison. Ellipsometry measurements of PCBM developed using CFM reveal n, k values consistent with those previously determined for PCBM:CBZ blends. Characterization of PCBM films on glass and ITO substrates showed the PCBM optical band gap to be ~1.83-1.95 eV. For PCBM spin coated on VT deposited polycrystalline CdTe, a blocking contact with a 0.6 eV barrier is formed.

Chapter 7

CONCLUSIONS AND FUTURE WORK

7.1 Conclusions

This work has focused on approaches to increase V_{oc} of CdS/CdTe superstrate devices. The methods used involved thinning of the CdTe layer to reduce bulk recombination, and the application/evaluation of PCBM as a contact to CdTe. Alternative devices were developed with reference to a baseline CdS/CdTe/Cu_2Te device which utilized 4-9 μm CdTe and a 0.3-0.4 eV Cu_2Te Schottky contact. Baseline and alternative contact devices were fabricated using the same window/CdTe deposition and $CdCl_2$ heat treatment processing, and hence differed only in the CdTe thickness and choice of contact. Important conclusions from this work are as follows.

1. Using a liquid junction quinhydrone-Pt probe, V_{oc} measurements of thinned CdTe devices resulted in a V_{oc} increase resulting from reducing the space charge width. This was apparent for devices fabricated with and without Cu and a maximum V_{oc} increase of 170 mV was observed with regional CdTe thickness t_{CdTe} <1 μm.

2. Optical and morphological properties of PCBM have been determined using chloroform and ethylenediamine blends. Optical PCBM n, k constants show similar behavior to those taken by previous authors, and a 1.8-2.0 eV bandgap for PCBM has been determined, consistent with a PCBM HOMO-LUMO gap of 2.0 eV.

3. PCBM was tested as a solid junction contact to CdTe. However, a blocking barrier of 0.6 eV was observed.

7.2 Future Work

Given the efficiency limitations of CdTe devices due to lower than expected V_{oc}, it is worth exploring experimental methods to minimize recombination and hence raise V_{oc}. This includes further assessment of materials which could form an ohmic contact to CdTe. Because of the favorable 5.8 eV valence band and 1.8-2.0 eV bandgap of PCBM, as well as low deposition temperature, this material could provide an ohmic contact to CdTe if it were possible to eliminate the 0.6 eV CdTe/PCBM blocking barrier which could be accomplished by doping PCBM p-type. Continued exploration and characterization of alternative materials with potential use as a back contact to CdTe should also be explored.

A second pathway to higher V_{oc} is a method to dope CdTe p-type without the formation of compensating donor defects [23]. Previous research has led to a record 1017 mV device based on bulk CdTe doping of 10^{16}-10^{17} holes/cm^3 [14], with an associated Fermi Level of 0.1-0.2 eV based on Boltzmann statistics. A V_{oc}>1V device could be possible if the Fermi level were lowered below 0.1 eV which would require raising the CdTe hole concentration above 10^{17} holes/cm^3.

REFERENCES

[1] Fraunhofer Institute for Solar Energy Systems ISE, "Photovoltaics Report," Fraunhofer ISE, 2014.

[2] M. L. Cohen and T. K. Bergstresser, "Band Structures and Pseudopotential Form Factors for Fourteen Semiconductors of the Diamond and Zinc-blende Structures," *Physical Review*, vol. 141, no. 2, pp. 789-796, 1966.

[3] M. Aven and J. Prener, "Physics and Chemistry of II-VI Compounds, Chapter 4," New York, Interscience Publishers, 1967, pp. 167-222.

[4] B. E. McCandless, J. E. Phillips and J. Titus, "Characterizing Contacts To P-type CdTe in CdS/CdTe Solar Cells," in *2nd World Conference on Photovoltaic Energy Conversion*, Vienna, 1998.

[5] "National Center for Photovoltaics," 9 March 2016. [Online]. Available: http://www.nrel.gov/ncpv/. [Accessed 19 March 2016].

[6] M. Gloeckler, I. Sankin and Z. Z., "CdTe Solar Cells at the Threshold to 20% Efficiency," *IEEE J. Photovolt.*, vol. 3, no. 4, pp. 1389-1393, 2013.

[7] M. Green, K. Emery, Y. Hishikawa, W. Warta and E. Dunlop, "Solar cell efficiency tables (version 44)," *Prog Photovolt Res Appl*, vol. 22, no. 7, pp. 701-710, 2014.

[8] M. Green, K. Emery, Y. Hishikawa, W. Warta and E. Dunlop, "Solar cell efficiency tables (Version 45)," *Prog. Photovolt: Res. Appl.*, vol. 23, no. 1, pp. 1-9, 2015.

[9] E. Wesoff, "Exclusive: First Solar's CTO Discusses Record 18.6% Efficient Thin-Film Module," Green Tech Media, 15 June 2015. [Online]. Available:

http://www.greentechmedia.com/articles/read/Exclusive-First-Solars-CTO-Discusses-Record-18.6-Efficient-Thin-Film-Mod. [Accessed 15 September 2015].

[10] First Solar, "Resource Library: Module Documentation," 7 August 2015. [Online]. Available: http://www.firstsolar.com/en/About-Us/Resource-Library/Module-Documents.aspx. [Accessed 15 September 2015].

[11] "Manufacturing Process: Advanced, Continuous Process," First Solar, [Online]. Available: http://www.firstsolar.com/Home/Technologies-and-Capabilities/PV-Modules/First-Solar-Series-3-Black-Module/Manufacturing-Process. [Accessed 15 September 2015].

[12] W. Shockley and H. Queisser, "Detailed Balance Limit of Efficiency of p-n Junction Solar Cells," *J. Appl. Phys.*, vol. 32, no. 3, p. 510, 1961.

[13] B. McCandless, "CdTe Solar Cells: Processing Limits and Defect Chemistry Effects on Open Circuit Voltage," in *MRS Proceedings*, San Francisco, 2013.

[14] J. Burst, J. Duenow, D. Albin, E. Colegrove, M. Reese, J. Aguiar, C. Jiang, M. A.-J. M. Patel, D. Kuciauskas, S. Swain, T. Ablekim, K. Lynn and W. Metzger, "CdTe solar cells with open-circuit voltage breaking the 1V barrier," *Nat. Energy*, vol. 1, p. 16015, 2016.

[15] D. Kuciauskas, A. Kanevce, P. Dippo, S. Seyedmohammadi and R. Makik, "Minority-Carrier Lifetime and Surface Recombination Velocity in Single-Crystal CdTe," *IEEE J. Photovolt*, vol. 5, no. 1, pp. 366-371, 2015.

[16] J. Burst, D. Albin, J. Duenow, M. Reese, S. Farrell, D. Kuciauskas and W. Metzger, "Advances in control of Doping and Lifetime in Single-Crystal and Polycrystalline CdTe," in *40th IEEE-PVSC*, Denver, 2014.

[17] S. S. Hegedus and W. N. Shafarman, "Thin-Film Solar Cells: Device Measurements and Analysis," *Prog. Photovolt: Res. Appl.*, vol. 12, no. 23, pp. 155-176, 2004.

[18] A. Luque and S. Hegedus, "Cadmium Telluride Solar Cells," in *Handbook of Photovoltaic Science and Engineering, Second Edition, Chapter 14*, West

Sussex, UK, John Wiley & Sons Ltd, 2011, pp. 600-641.

[19] S. S. Hegedus, D. Desai and C. P. Thompson, "Voltage Dependent Photocurrent Collection in CdTe/CdS Solar Cells," *Prog. Photovolt: Res. Appl.*, vol. 15, no. 7, pp. 587-602, 2007.

[20] N. W. Ashcroft and N. D. Mermin, "Homogeneous Semiconductors," in *Solid State Physics*, Thomson Learning, Inc., 1976, pp. 562-587.

[21] M. A. Berding, "Native defects in CdTe," *Phys. Rev. B,* vol. 60, no. 12, pp. 8943-8950, 1999.

[22] S. Fonash, Solar Cell Device Physics: pp 78-79, New York: Academic Press, 1981.

[23] S. Wei and S. Zhang, "Chemical trends of defect formation and doping limit in II-VI semiconductors: The case of CdTe," *Phys. Rev. B,* vol. 66, no. 15, p. 155211, 2002.

[24] R. K. Swank, "Surface Properties of II-VI Compounds," *Phys. Rev.,* vol. 153, no. 3, pp. 844-849, 1967.

[25] E. Janik and R. Triboulet, "Ohmic contacts to p-type cadmium telluride and cadmium mercury telluride," *J. Phys. D: Appl. Phys.*, vol. 16, no. 12, pp. 2333-2340, 1983.

[26] J. Singh, "Semiconductor Devices: Basic Principles," in *Chapter 6: Semiconductor Junctions with Metals and Insulators*, New York, John Wiley, 2001.

[27] B. E. McCandless and W. A. Buchanan, "High Throughput Processing of CdTe/CdS Solar Cells with Thin Absorber Layers," in *33rd IEEE Photovoltaic Specialists Conference,* San Diego, CA, 2008.

[28] A. Gupta, V. Parikh and A. Compaan, "High efficiency ultra-thin sputtered CdTe solar cells," *Sol. Energ. Mat. Sol. Cells*, vol. 90, pp. 2263-2271, 2006.

[29] V. Plotnikov, D. Kwon, K. Wieland and A. Compaan, "10% Efficiency Solar

Cells with 0.5 um of CdTe," in *IEEE PVSC*, Philadelphia, 2009.

[30] N. Paudel, K. Wieland and A. Compaan, "Ultrathin CdS/CdTe solar cells by sputtering," *Sol. Energ. Mat. Sol. Cells,* vol. 105, pp. 109-112, 2012.

[31] J. Sites and J. Pan, "Strategies to increase CdTe solar-cell voltage," *Thin Solid Films,* vol. 515, pp. 6099-6102, 2007.

[32] J. E. Webb and J. P. Hamilton, "Physical Properties of Glass and the Requirements for Photovoltaic Modules," in *NREL Photovoltaic Module Reliability Workshop*, Golden Co., February 16, 2011.

[33] T. Meng, B. McCandless, Q. Buchanan, R. Birkmire, C. Hamilton, B. Aitken and C. Kosik Williams, "Effect of Annealing Atmosphere and Temperature on the Properties of Cd2SnO4 Thin Films," in *38th IEEE-PVSC,* Austin, 2012.

[34] T. Meng, B. McCandless, W. Buchanan, E. Kimberly and R. Birkmire, "Cadmium tin oxide thin films deposited by RF magnetron sputtering for photovoltaic applications," *J. Alloys Compd.,* vol. 556, pp. 39-44, 2013.

[35] X. Wu, "High-efficiency polycrystalline CdTe thin-film solar cells," *Solar Energy,* vol. 77, pp. 803-814, 2004.

[36] X. Wu, R. Dhere, D. Albin, T. Gessert, C. DeHart, J. Keane, A. Duda and T. Coutts, "High-Efficiency CTO/ZTO/CdS/CdTe Polycrystalline Thin-Film Solar Cells," *Proceedings of NCPV program review meeting,* vol. 47, 2001.

[37] B. McCandless and W. Shafarman, "Chemical Surface Deposition of Ultra-Thin Semiconductors". United States/Wilmington, DE Patent US 6,537,845 B1, 25 March 2003.

[38] B. McCandless and S. Hegedus, "Influence of CdS window layers on thin film CdS/CdTe solar cell performance," in *IEEE-PVSC,* Las Vegas, 1991.

[39] N. Romeo, A. Bosio, R. Tedeschi and V. Canevari, "Growth of polycrystalline CdS and CdTe thin layers for high efficiency thin film solar cells," *Mater. Chem. Phys.,* vol. 66, no. 2, pp. 201-206, 2000.

[40] G. M. Hanket, B. E. McCandless, W. A. Buchanan, S. Fields and R. W. Birkmire, "Design of a vapor transport deposition process for thin film materials," *J. Vac. Sci. Technol. A,* vol. 24, no. 5, pp. 1695-1701, 2006.

[41] B. E. McCandless, I. Youm and R. W. Birkmire, "Optimization of Vapor Post-deposition Processing for Evaporated CdS/CdTe Solar Cells," *Prog. Photovolt. Res. Appl.,* vol. 7, pp. 21-30, 1999.

[42] E. Kimberly, "Controlling Opto-Electric Properties of Cadmium Stannate Thin Films Deposited By RF Sputtering," University of Delaware, Newark, DE, 2011.

[43] B. McCandless, M. Engelmann and R. Birkmire, "Interdiffusion of CdS/CdTe thin films: Modeling x-ray diffraction line profiles," *J. Appl. Phys.,* vol. 89, no. 2, pp. 988-994, 2001.

[44] T. Dzhafarov, S. Yesilkaya, N. Yilmaz Canli and M. Caliskan, "Diffusion and influence of Cu on properties of CdTe thin films and CdTe/CdS cells," *Sol. Energy Mater. Sol. Cells ,* vol. 85, no. 3, pp. 371-383, 2005.

[45] "Section E: General Physical Constants," in *CRC Handbook of Chemistry and Physics: 70th Edition*, Boca Raton, Florida, CRC Press, Inc., 1989-1990.

[46] B. E. McCandless, Y. Qu and R. W. Birkmire, "A Treatment to Allow Contacting CdTe with Different Conductors," in *First World Conference on Photovoltaic Energy Conversion*, Waikoloa, Hawaii, December 1994.

[47] Guide to Using WVASE32 Software for VASE and M-44 Ellipsometers: A Short Course in Ellipsometry, Lincoln, NE: J.A. Woollam Co., Inc..

[48] J.A. Woollam Co. Inc., "Complete Ease Data Analysis Manual, Chapters 3-4," 2011.

[49] A. Luque and S. Hegedus, "Measurement and Characterization of Solar Cells and Modules," in *Handbook of Photovoltaic Science, and Engineering, 2nd Edition, Chapter 18,* West Sussex, UK, John Wiley & Sons Ltd, 2011, pp. 797-840.

[50] C. Thompson, "Characterization of Photocurrent and Voltage Limitations of Cu(In,Ga)Se2 Thin-Film Polycrystalline Solar Cells," University of Delaware, Newark, DE, 2008.

[51] F. Urbach, "The Long-Wavelength Edge of Photographic Sensitivity and of the Electronic Absorption of Solids," *Phys. Rev,* vol. 92, no. 5, p. 1324, 1953.

[52] A. Iribarren, R. Castro-Rodriguez, F. Caballero-Briones and J. Pena, "Optical and structural evidence of the grain-boundary influence on the disorder of polycrystalline CdTe films," *Appl. Phys. Lett.,* vol. 74, no. 20, pp. 2957-2959, 1999.

[53] M. Roy, S. Damaskinos and J. Phillips, "The Diode Current Mechanism in CuInSe2/(CdZn)S Heterojunctions," *20th IEEE-PVSC,* vol. 2, pp. 1618-1623, 1988.

[54] B. Streetman and S. Banerjee, Solid State Electronic Devices, 6th Edition, New Delhi: PHI Learning Private Limited, 2009.

[55] Heath, Cohen and Shafarman, "Bulk and metastable defects in CuIn1-xGaxSe2 thin films using drive-level capacitance profiling," *J. Appl. Phys.,* vol. 95, no. 3, pp. 1000-1010, 2004.

[56] Heath and Zabierowski, "Advanced Characterization Techniques for Thin Film Solar Cells," in *Capacitance Spectroscopy of Thin-Film Solar Cells*, Weinheim, Wiley-VCH Verlag GmBH & Co., 2011, pp. 81-105.

[57] M. Gloeckler, A. L. Fahrenbruch and J. R. Sites, "3rd World Conference on Photovoltaic Energy Conversion," Osaka, Japan, May 11-18 2003.

[58] C. E. Michelson, A. V. Gelatos and J. D. Cohen, "Drive-level capacitance profiling: Its application to determining gap state densities in hydrogenated amorphous silicon films," *Appl. Phys. Lett.,* vol. 47, no. 4, pp. 412-414, 1985.

[59] Agilent Technologies, "Agilent 4284A Precision LCR Meter Operation Manual, Eighth Edition," Agilent Technologies, 2001.

[60] D. Desai, "Electrical Characterization of Thin Film CdTe Solar Cells,"

University of Delaware, Newark, DE, 2006.

[61] J. V. Li, A. F. Halverson, O. Sulima, S. Bansal, J. M. Burst, T. M. Barnes, T. A. Gessert and D. H. Levi, "Theoretical analysis of effects of deep level, back contact, and absorber thickness on capacitance-voltage profiling of CdTe thin-film solar cells," *Sol. Energy Mater. Sol. Cells*, vol. 100, pp. 126-131, 2012.

[62] J. Gray, "ADEPT: A General Purpose Numerical Device Simulator for Modeling Solar Cells in One, Two, and Three-Dimensions," in *IEEE 22nd PVSC*, Las Vegas, 1991.

[63] J. Gray and Y. Lee, "Numerical Modeling of Polycrystalline CdTe and CIS Solar Cells," in *23rd IEEE-PVSC*, Louisville, KY, 1993.

[64] Synopsys, "Sentaurus Device User Guide," Synopsys, 2010.

[65] A. Kanevce, D. Kuciauskas, T. Gessert, D. Levi and D. Albin, "Impact of Interface Recombination on Time Resolved Photoluminescence (TRPL) Decays in CdTe solar cells (Numerical Simulation Analysis)," in *38th IEEE-PVSC*, Austin, 2011.

[66] A. Kanevce, D. Levi and D. Kuciauskas, "The role of drift, diffusion, and recombination in time-resolved photoluminescence of CdTe solar cells determined through numerical simulation," *Prog. Photovolt: Res. Appl. ,* vol. 22, no. 11, pp. 1138-1146, 2014.

[67] R. Kapadia, Z. Fan and A. Javey, "Design constraints and guidelines for CdS/CdTe nanopillar based photovoltaics," *Appl. Phys. Lett.*, vol. 96, no. 10, p. 103116, 2010.

[68] N. Amin, K. Sopian and M. Konagai, "Numerical modeling of CdS/CdTe and CdS/CdTe/ZnTe solar cells as a function of CdTe thickness," *Sol. Energy Mater. Sol. Cells* , vol. 91, no. 13, pp. 1202-1208, 2007.

[69] N. Amin, K. Sopian, M. Yahya and A. Zaharim, "Significance of Absorber Thickness Reduction in CdTe Thin Film Solar Cells for Promising Terrestrial Usage- From the Perspective of Numerical Analysis," in *8th WSEAS International Conference on Power Systems*, Bangi, Malaysia, 2008.

[70] Y. Liu, Y. Sun and A. Rockett, "A new simulation software of solar cells-wxAMPS," *Solar Energy Materials & Solar Cells,* vol. 98, pp. 124-128, 2012.

[71] S. J. Fonash and et_al, "A Manual for AMPS 1D: A One-Dimensional Device Simulation Program for the Analysis of Microelectronic and Photonic Structures," Electric Power Research Institute.

[72] M. Burgelman, P. Nollet and S. DeGrave, "Modelling polycrystalline semiconductor solar cells," *Thin Solid Films,* Vols. 361-362, pp. 527-532, 2000.

[73] S. Degrave, M. Burgelman and P. Nollet, "Modelling of Polycrystalline Thin Film Solar Cells: New Features in SCAPS Version 2.3," in *3rd World Conference on Photovoltaic Energy Conversion*, Osaka, Japan, 2003.

[74] H. K. Gummel, "A Self-Consistent Iterative Scheme for One-Dimensional Steady State Transistor Calculations," *IEEE Trans. Electron Devices,* vol. 11, no. 10, pp. 455-465, 1964.

[75] X. Wu, "High-efficiency polycrystalline CdTe thin-film solar cells," *Solar Energy,* vol. 77, no. 6, pp. 803-814, December 2004.

[76] T. Coutts, D. Young, L. X, W. Mulligan and X. Wu, "Search for improved transparent conducting oxides: A fundamental investigation of CdO, Cd2SnO4 and Zn2SnO4," *J. Vac. Sci. Technol. A,* vol. 18, no. 6, pp. 2646-2660, 2000.

[77] K. Kim, H. Kim, D. L. J. Hwang and S. Park, "Realization of p-type ZnO thin films via phosphorus doping and thermal activation of the dopant," *Appl. Phys. Lett.,* vol. 83, no. 1, pp. 63-65, 2003.

[78] D. Young, H. Moutinho, Y. Yan and T. Coutts, "Growth and characterization of radio frequency magnetron sputter-deposited zinc stannate, Zn2SnO4, thin films," *J. Appl. Phys.,* vol. 92, no. 1, pp. 310-319, 2002.

[79] J. Fritsche, T. Schulmeyer, D. Kraft, Thißen, A. and A. Klein, "Utilization of sputter depth profiling for the determination of band alignment at polycrystalline CdTe/CdS heterointerfaces," *Appl. Phys. Lett.,* vol. 81, no. 12, pp. 2297-2299, 2002.

[80] D. Albin, *unpublished: National Renewable Energy Laboratory*, Golden, CO.

[81] W. K. Metzger, D. Albin, D. Levi, P. Sheldon, X. Li, B. M. Keyes and R. K. Ahrenkiel, "Time-resolved photoluminescence studies of CdTe solar cells," *J. Appl. Phys.*, vol. 94, no. 5, pp. 3549-3555, September 2003.

[82] J. Moseley, M. Al-Jassim, H. Moutinho, H. Guthrey, W. Metzger and R. Ahrenkiel, "Explanation of red spectral shifts at CdTe grain boundaries," *Appl. Phys. Lett.*, vol. 103, p. 233103, 2013.

[83] C. Suresh and N. Koga, "A Consistent Approach toward Atomic Radii," *J. Phys. Chem. A.*, vol. 105, no. 24, pp. 5940-5944, 2001.

[84] B. McCandless, "IEC-Corning CdTe Project: Final Report," Unpublished, 2012.

[85] C. Sah, R. Noyce and W. Shockley, "Carrier Generation and Recombination in P-N Junctions and P-N Junction Characteristics," *Proc IRE,* vol. 45, no. 9, pp. 1228-1243, 1957.

[86] B. Zengir, M. Bayhan and S. Kavasoglu, "Optical absorption in polycrystalline CdTe thin films," *Cankaya University Journal of Arts and Sciences,* vol. 1, no. 5, pp. 103-116, 2006.

[87] A. Iribarren, R. Castro-Rodriguez, V. Sosa and J. Pena, "Modeling of the disorder contribution to the band-tail parameter in semiconductor materials," *Phys. Rev. B,* vol. 60, no. 7, pp. 4758-4762, 1999.

[88] C. Seaman, "Calibration of Solar Cells By The Reference Cell Method-The Spectral Mismatch Problem," *Solar Energy,* vol. 29, no. 4, pp. 291-298, 1982.

[89] D. de Nobel, "Phase Equilibria and Semiconducting Properties of Cadmium Telluride," *Phillips Res. Repts,* vol. 14, pp. 361-399 and 430-492, 1959.

[90] J. Boucher, D. Miller, C. Warren, J. Cohen, B. McCandless, J. Heath, M. Lonergan and S. Boettcher, "Optical response of deep defects as revealed by transient photocapacitance and photocurrent spectroscopy in CdTe/CdS solar cells," *Sol. Energy Mater. Sol. Cells* , vol. 129, pp. 57-63, 2014.

[91] J. Mullins, J. Carles and A. Brinkman, "High temperature optical properties of cadmium telluride," *J. Appl. Phys.,* vol. 81, no. 9, pp. 6374-6379, 1997.

[92] D. Marple, "Optical Absorption Edge in CdTe: Experimental," *Phys. Rev.,* vol. 150, no. 2, pp. 728-734, 1966.

[93] C. Thompson, S. Hegedus, W. Shafarman and D. Desai, "Temperature Dependence of Voc in CdTe and Cu(InGa)(SeS)2 Based Solar Cells," in *33rd IEEE-PVSC,* San Diego, 2008.

[94] S. Demtsu, D. Albin, J. Sites, W. Metzger and A. Duda, "Cu-related recombination in CdS/CdTe solar cells," *Thin Solid Films,* vol. 516, no. 8, pp. 2251-2254, 2008.

[95] B. McCandless and S. Rykov, "Cross-Section Potential Analysis of CdTe/CdS Solar Cells by Kelvin Probe Force Microscopy," in *33rd IEEE PVSC,* San Diego, 2008.

[96] G. Koishiyev, J. Sites, S. Kulkarni and N. Dhere, "Determination of Back Contact Barrier Height in Cu(In,Ga)(Se,S)2 and CdTe Solar Cells," in *33rd IEEE PVSC,* San Diego, 2008.

[97] S. Demutsu, "Impact of Back Contact Materials on Performance and Stability of CdS/CdTe Solar Cells," Colorado State University, Fort Collins, 2006.

[98] B. McCandless, "CdTe Etching," Unpublished, Newark, DE, 206.

[99] S. Li and B. McCandless, "CdTe thickness and HT," Unpublished-Institute of Energy Conversion/University of Delaware , Newark, DE, 2013.

[100] "Dektak 3 Profilometer," [Online]. Available: https://www.inrf.uci.edu/facility/equipment/characterization/dektak-3-profilometer/. [Accessed 19 March 2016].

[101] S. Feldman-Peabody, R. Gossman and T. Lucas, "Method and system for application of an insulating dielectric material to photovoltaic module substrates". USA Patent US20120021536 A1, 26 Jan 2012.

[102] J. Kiel, B. Kirby, C. Majkrzak, B. Maranville and M. Mackay, "Nanoparticle concentration profile in polymer-based solar cells," *Soft Matter,* vol. 6, no. 3, pp. 641-646, 2010.

[103] W. Geens, T. Martens, J. Poortmans, T. Aernouts, J. Manca, L. Lutsen, P. Heremans, S. Borghs, R. Mertens and D. Vanderzande, "Modelling the short-circuit current of polymer bulk heterojunction solar cells," *Thin Solid Films,* Vols. 451-452, pp. 498-502, 2004.

[104] M. Rispens, A. Meetsma, R. Rittberger, C. Brabec, N. Sariciftci and J. Hummelen, "Influence of the solvent on the crystal structure of PCBM and the efficiency of MDMO-PPV:PCBM 'plastic' solar cells," *Chem. Commun.,* vol. 17, no. 9-10, pp. 2116-2118, 2003.

[105] X. Yang, J. van Duren, M. Rispens, J. Hummelen, R. Janssen, M. Michels and J. Loos, "Crystalline Organization of a Methanofullerene as Used for Plastic Solar-Cell Applications," *Adv. Mater.,* vol. 16, no. 9-10, pp. 802-806, 2004.

[106] M. Reyes-Reyes, K. Kim, J. Dewald, R. Lopez-Sandoval, A. Avadhanula, S. Curran and D. Carroll, "Meso-Structure Formation for Enhanced Organic Photovoltaic Cells," *Org. Lett.,* vol. 7, no. 26, pp. 5749-5752, 2005.

[107] L. Chang, H. Lademann, J. Bonekamp, K. Meerholz and A. Moul, "Effect of Trace Solvent on the Morphology of P3HT:PCBM Bulk Heterojunction Solar Cells," *Adv Funct Mater,* vol. 21, no. 10, pp. 1779-1787, 2011.

[108] J. Maibach, T. Adermann, T. Glaser, R. Eckstein, E. Mankel, A. Pucci, K. Mullen, U. Lemmer, M. Hamburger, T. Mayer and W. Jaegermann, "Impact of processing on the chemical and electronic properties of phenyl-C61-butyric acid methyl ester," *J. Mater. Chem. C,* vol. 2, no. 37, pp. 7934-7942, 2014.

[109] Z. Guan and e. al, "Direct Determination of the Electronic Structure of the Poly(3-hexylthiophene):phenyl-[6,6]-C61 Butyric Acid Methyl Ester Blend," *Organic Electronics,* vol. 11, no. 11, pp. 1779-1785, 2010.

[110] L. Goris, K. Haenen, M. Nesladek, P. Wagner, D. Vanderzande and L. De Schepper, "Absorption phenomena in organic thin films for solar cell applications investigated by photothermal deflection spectroscopy," *J. Mater.*

Sci., vol. 40, no. 6, pp. 1413-1418, 2005.

[111] U. Zhokhavets, R. Goldhahn, G. Gobsch, M. Al-Ibrahim, H. Roth, S. Sensfuss, E. Klemm and D. Egbe, "Anisotropic Optical Properties of Conjugated Polymer and Polymer/Fullerene Films," *Thin Solid Films,* vol. 444, no. 1-2, pp. 215-220, 2003.

[112] H. Hoppe, N. Sariciftci and D. Meissner, "Optical Constants of Conjugated Polymer/Fullerene Based Bulk-Heterojunction Organic Solar Cells," *Mol. Cryst. Liq. Cryst.,* vol. 385, no. 1, pp. 113-119, 2002.

[113] M. de Haas, J. Warman, T. Anthopoulos and D. de Leeuw, "The Mobility and Decay Kinetics of Charge Carriers in Pulse-Ionized Microcrystalline PCBM Powder," *Adv. Funct. Mater.,* vol. 16, no. 17, pp. 2274-2280, 2006.

[114] E. Hauff, V. Dyankonov and J. Parisi, "Study of Field Effect Mobility in PCBM Films and P3HT:PCBM Blends," *Sol Energy Mater Sol Cells,* vol. 87, no. 1-4, pp. 149-156, 2005.

[115] V. Mihailetchi, J. van Duren, P. Blom, J. Hummelen, R. Janssen, J. Kroon, M. Rispens, W. Verhees and M. Wienk, "Electron Transport in a Methanofullerene," *Adv. Funct. Mater.,* vol. 13, no. 1, pp. 43-46, 2002.

[116] C. Walkons, B. Guralnick, B. McCandless and R. Birkmire, "CdTe Solar Cells with a PCBM Back Contact," in *40th IEEE-PVSC,* Denver, 2014.

[117] S. Cook, H. Ohkita, Y. Kim, J. Benson-Smith, D. Bradley and J. Durrant, "A Photophysical Study of PCBM Thin Films," *Chem Phys Lett,* vol. 445, no. 4-6, pp. 276-280, 2007.

[118] H. J. Hovel, "Chapter 2: Carrier Collection, Spectral Response, and Photocurrent," in *Semiconductors and Semimetals: Volume II,* London, Academic Press, Inc, 1975, pp. 8-25.

[119] C. Greeff and H. Glyde, "Anomalous Urbach tail in GaAs," *Phys. Rev. B,* vol. 51, no. 3, pp. 1778-1783, 1995.

[120] S. Demtsu and J. Sites, "Effect of back-contact barrier on thin-film CdTe solar

cells," *Thin Solid Films,* vol. 510, no. 1-2, pp. 320-324, 2006.

[121] S. Sze, Physics of Semiconductor Devices, 3rd Edition, Chapter 3, Hoboken: John Wiley & Sons, Inc., 2007.

Appendix A

EFFECT OF CDTE DEPOSITION TEMPERATURE ON CDTE DEVICE PERFORMANCE AND CHARACTERISTICS

This appendix section examines the effect of CdTe deposition temperature VT T_{ss}=550-630ºC on device performance for C065/CTO/ZTO/CdS/CdTe/Cu_2Te/Ni devices. The deposition temperature T_{ss} over this range influences device performance as previously mentioned in section 4.3.3. and this is shown again in Figure A-1, and Table A-1.

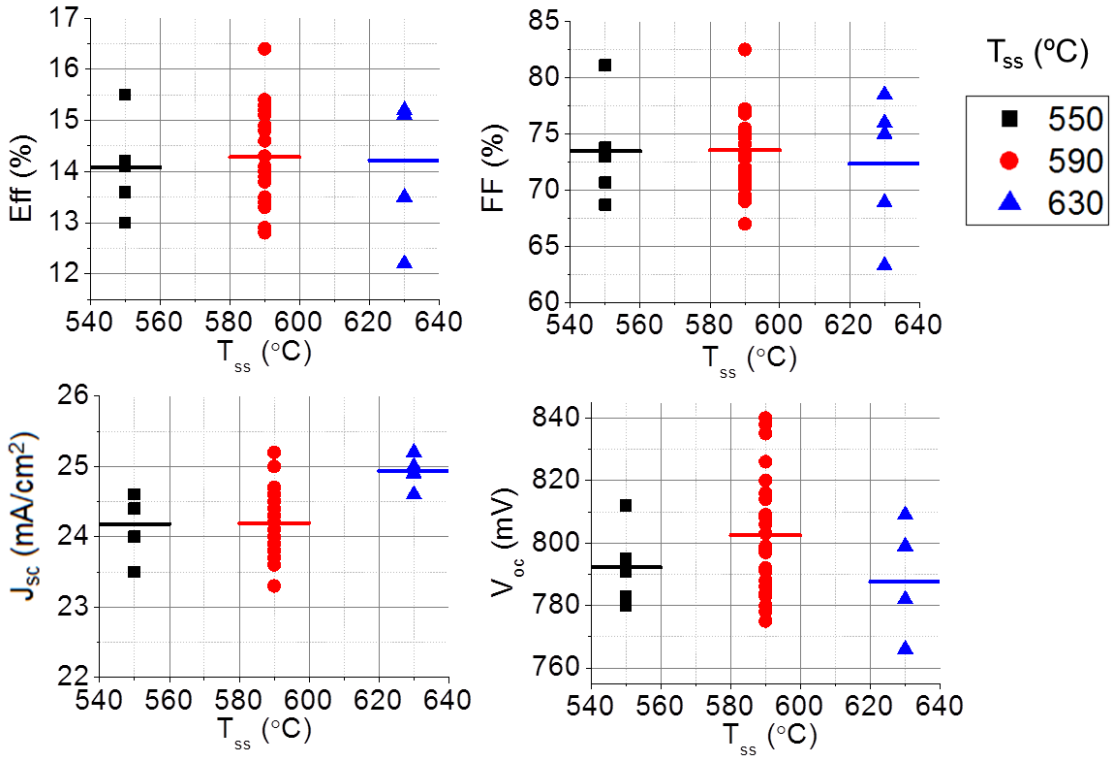


Figure A-1: Device performance of C065/CTO/ZTO window stack best efficiency CdTe cells/sample with T_{ss}=550-630 ºC, t_{CdTe}=4-10 µm and t_{CdCl2}=25 minutes. Samples are of size 1"x"1 or 2"x1". Solid lines represent statistical averages. Cells with parasitic behavior exhibiting efficiency η<10%, R_{oc}>4 Ω-cm^2 (excessive series resistance), or G_{sc} > 2 mS/cm^2 (excessive voltage dependent collection current or shunting) are excluded from this analysis.

Table A-1: Average device performance of best efficiency CdTe C065/CTO/ZTO cells/sample based on VT T_{ss}.

T_{ss}	V_{oc}	J_{sc}	FF	η
(ºC)	mV	mA/cm^2	%	%
550	792	24.2	73.5	14.1
590	803	24.2	73.6	14.3
630	788	24.9	72.3	14.2

While a limited number of measurements have been taken on CdTe devices at 550 ºC and 630 ºC, there may exist a trend for T_{ss} on V_{oc} (550-630 ºC) and J_{sc} (590-630 ºC). Hence, measurements are performed to characterize photocurrent collection (J_{sc}) as well as second order metrics which can influence recombination (V_{oc}) as a function of deposition temperature. Second order recombination metrics include bandgap, CdTe crystal disorder properties (Urbach energy), space charge width, doping, diode ideality factor, recombination current, and activation energy of recombination. Devices are analyzed using CV/DLCP, quantum efficiency (QE), and current-voltage-temperature-light intensity (JVTI) measurements.

A.1 Characterization Devices and Performance

This section lists the device performance metrics with specific emphasis on V_{oc} for CdTe devices chosen for characterization and developed with T_{ss}= 590-630 ºC. Devices were developed as previously described in section 2.1 with 500 nm CTO, 50-75 nm ZTO, and 4-9 µm CdTe.

The initial device performance of the characterization cells is summarized in Table A-2.

Table A-2: Initial STC device performance of characterization cells fabricated with different CdTe deposition temperature T_{ss}.

T_{ss}	V_{oc}	J_{sc}	FF	η
ºC	mV	mA/cm^2	%	%
550	794-816	23.9-24.2	73.5-77.1	14.1-15.1
590	822-840	23.3-24.0	72.8-76.8	14.3-15.4
630	772-799	24.4-25.0	67.5-78.8	14.7-15.1

Hence, devices are examined with initial efficiency=14-15.5%, FF=67-79%, and J_{sc}~24-25 mA/cm^2. A higher J_{sc} is observed for T_{ss}=630 ºC compared to T_{ss}=550-590 ºC and this is discussed in greater detail in section 0. The V_{oc} performance of the characterization cells with T_{ss}=550 ºC (794-816 mV) and 590 ºC (816-838mmV) is above the statistical average of best efficiency devices ($V_{oc,avg}$(550 ºC)=792 mV, $V_{oc,avg}$(590 ºC)=803 mV). While this is not necessarily the case for all characterization cells fabricated with T_{ss}=630 ºC, the V_{oc} performance of these devices (772-799 mV) is within 16 mV of the statistical average (788 mV). A list of characterization devices with respective V_{oc} prior to measurements is shown in Table A-3.

Table A-3: V_{oc} performance of specific characterization cells fabricated with different CdTe deposition temperature T_{ss}. Values of Voc are listed in bold while the cell number is listed underneath. SELH conditions→T= 300 ºK, 1000 W/m^2, and ELH bulb illumination.

Sample	T_{ss} ºC	V_{oc}(STC) (mV) DLCP	V_{oc}(STC) (mV) QE	V_{oc}(SELH) (mV) JVTI
VT408.6	550	**794-795** 008		NA
VT448.6		**812-816** 006		**808-811** 006
VT464.2	590	**837-838** 002		**828-830** 005
VT465.2		**822-826** 008		**816-821** 007
VT481.6		**835-837** 008		**822-824** 006
VT438	630	**797-799** VT438.6-002	**772-774** VT438.2-004	**781-785** VT438.6-001
VT439.3		**780-782** 001		**791** 001

The variation in V_{oc} is due to measurement hysteresis. Lower values of V_{oc} for JVTI measurements may be due to cell degradation between measurements as seen by an increase in voltage dependent collection current and lower FF, or possibly a mismatch between the AM1.5 and ELH spectrum. The shunt conductance of these devices is low (G_{sc}<0.5 mS/cm^2) and should not significantly affect performance.

A.2 QE Measurements

This section discusses QE measurements, which were used to characterize photocurrent losses and CdTe bandtail absorption properties of bandgap and Urbach energy as a function of T_{ss}.

QE measurements from 350-900 nm are shown for CdTe devices with similar thickness and hence CdTe grain size [27] (Figure A-2).

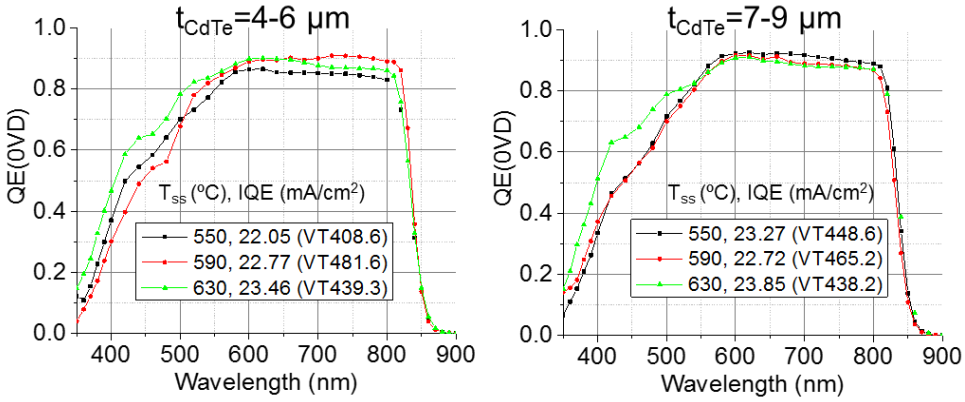


Figure A-2: QE measurements of CdTe devices fabricated with T_{ss}=550-630 ºC. Measurements are taken at equilibrium conditions of 0V with no white bias illumination.

For CdTe devices developed with T_{ss}=550 ºC vs T_{ss}=590 ºC, there is no consistent trend in the QE response and associated integrated quantum efficiency (IQE). However, for the samples VT408.6 and VT481.6, there is a noticeable difference in the λ=600-800 nm QE response where photocarrier losses are dominated by bulk recombination in CdTe or reflection.

No difference was observed in the QE response at reverse bias (-0.5V) or when applying a 90 mW/cm^2 white bias light, and hence, photocarrier collection is not sensitive to light dependent defects and is maximized at 0V.

For CdTe devices developed with T_{ss}=630 ºC, a consistent increase is observed in the QE response at short wavelength (350-520 nm), associated with a higher integrated quantum efficiency IQE and hence J_{sc} (Table A-2). This increase in short wavelength QE is suggestive of a thinner CdS layer resulting in lower parasitic CdS absorption. As previously mentioned, (section 4.3.3), increasing the CdTe deposition

(anneal) temperature with a fixed $CdCl_2$ treatment results in depletion of sulfur from CdS into CdTe [18] and subsequent thinning of CdS.

The CdTe bandgap E_g and Urbach energy E_U are measured from long wavelength QE measurements where band-tail light absorption is observed in the QE data ($E>E_g$=1.5 eV or λ>820 nm). Fitting was performed over λ=850-880 nm using

$$\ln\big(QE(E)\big) = \frac{(E - E_g)}{E_U} \qquad \text{(A-1)}$$

and the fits are shown in Figure A-3.

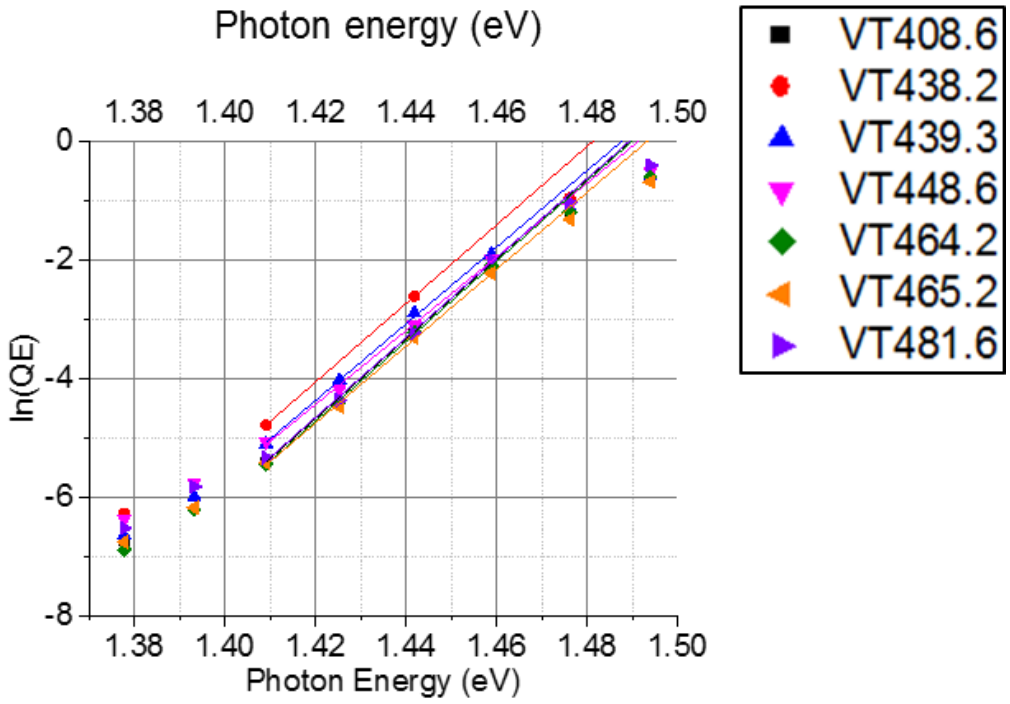


Figure A-3: Experimental ln(QE) vs E data with fitting of ln(QE) vs E to determine the bandgap E_g and Urbach energy E_U. The best fit is found over 4 points from 1.41-1.46 eV (850-880 nm). Below 1.41 eV (880 nm), noise dominates the QE.

The resulting Urbach energy and bandgap are summarized in Table A-4.

Table A-4: Measured bandgap, Urbach energy, and V_{oc}

Sample	T_{ss}	t_{CdTe}	E_g	E_U	V_{oc}
	ºC	µm	eV	meV	mV
VT408.6	550	4.4	1.49	15	794-795
VT448.6		8.0		16	812-816
VT464.2	590	5.9			837-838
VT465.2		7.3	1.49	15	822-826
VT481.6		4.2			835-837
VT438.2	630	8.8	1.48	15	772-774
VT439.3		5.3	1.49	16	780-782

Urbach energy of the CdTe devices ranges from 15-16 meV and no trend is observed regarding Urbach energy for CdTe devices developed with VT deposition temperature T_{ss}=550-630 ºC, or with Urbach energy and V_{oc}. Since the CdTe grain size is related to the Urbach energy [52], the QE measurements also suggest similar CdTe grain size for 4-9 µm. However, this would need to be confirmed by XRD or AFM measurements which is beyond the scope of this work.

The CdTe device VT438.2, which was developed with T_{ss}=630 ºC does exhibit a smaller bandgap of 1.48 eV compared to the other devices with E_g=1.49 eV, and a decrease in bandgap by 10 meV may also contribute to the relatively smaller V_{oc}=772-774 mV. The smaller bandgap is suggestive of a higher concentration/uptake of sulfur from CdS than the other devices, and as previously stated, a thinner CdS on VT438.2 was also apparent from short wavelength QE measurements (Figure A-2). For a sulfurized $CdTe_{1-x}S_x$ alloy, a 1.49 eV bandgap corresponds to a sulfur concentration of x=0.02 while a 1.48 eV bandgap corresponds to a sulfur concentration of x=0.03 [49]. From the phase diagram of $CdTe_{1-x}S_x$, a higher concentration of sulfur CdTe is also

expected for increased CdTe deposition (anneal) temperature. However, the detection of sulfur within the CdTe bulk would be needed for more definitive conclusions. A sulfur detection technique such as x-ray diffraction or electron dispersive spectroscopy could be applied to the device CdTe films, but is beyond the scope of this work.

A.3 DLCP Measurements

This section discusses DLCP measurements, which were used to analyze the Voc vs T_{ss} relation for bulk CdTe doping, associated Fermi energy, and space charge width. The technique of DLCP was utilized over CV since the latter technique cannot provide reliable doping measurements of CdTe (see section 4.4.2).

DLCP measurements were taken at 300 ºK, 1 MHz, from -1V to 0.5 V forward bias. An estimate of CdTe doping is taken using DLCP and Eq. (2-43) to solve for $N_{DL}(V)$. A lower limit of space charge width (W) was estimated by using the moment of charge response, $\langle x \rangle$ measured by Eq. (2-45) for DLCP measurements. Measurements of $N_{DL}(V)$ and $\langle x(V) \rangle$ as a function of applied bias are shown in Figure A-4.

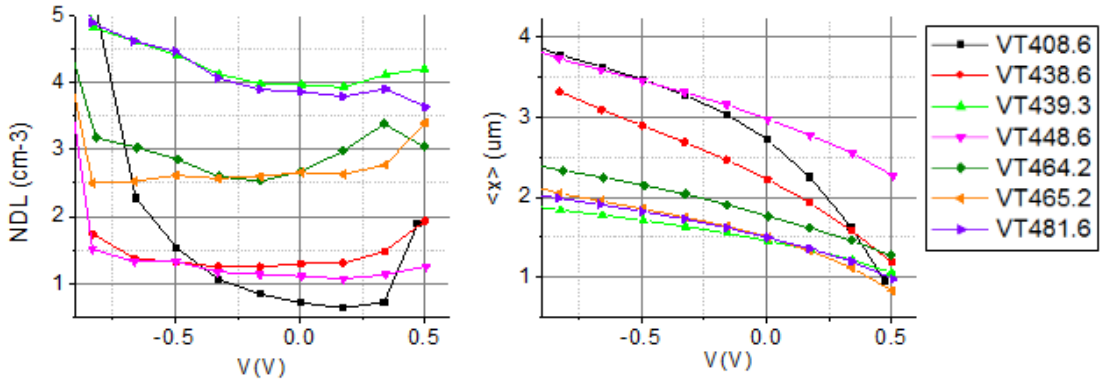


Figure A-4: a.) DLCP measurements of $N_{DL}(V)$ and b.) corresponding space charge width measurements <x(V)>.

The bulk CdTe doping is estimated by the minimum value of N_{DL}, while space charge width at equilibrium is estimated by <x(V=0)>. The Fermi energy is also estimated using a Boltzmann approximation

$$E_F = -kTln(\frac{N_{DL,min}}{N_V}) \quad \text{(A-2)}$$

with the hole density $p \rightarrow N_{DL,min}$, $N_v = 1.8*10^{19}$ cm^{-3} [57] and kT=25.8 meV (T=300 ^oK). This is summarized in Table A-5.

Table A-5: Values of $N_{DL,min}$ E_F, <x(V=0)> and corresponding V_{oc} for CdTe samples fabricated with a CdTe deposition temperature T_{ss}=550-630 ºC.

Sample	T_{ss}	$N_{DL,min}$	E_F	<x(V=0)>	V_{oc}
	ºC	10^{14} cm^{-3}	meV	µm	mV
VT408.6	550	0.6	326	2.7	794-795
VT448.6		1.1	310	3.0	812-816
VT464.2	590	2.5	289	1.8	837-838
VT465.2		2.5	289	1.5	822-826
VT481.6		3.6	280	1.5	835-837
VT438.6	630	1.3	306	2.2	797-799
VT439.3		3.9	278	1.5	780-782

For T_{ss}=550-590 ºC, plots of V_{oc} vs $N_{DL,min}$ and E_F are plotted in Figure A-5.

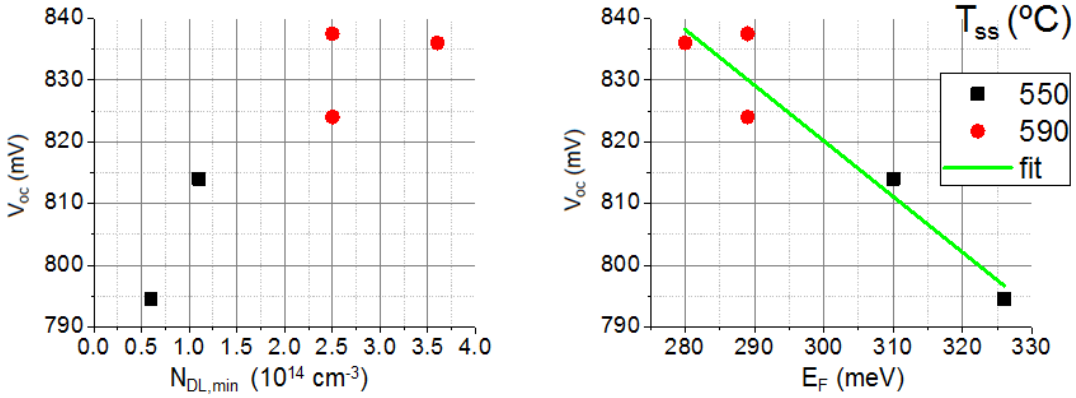


Figure A-5: Plots of V_{oc} vs $N_{DL,min}$ and V_{oc} vs E_F, where the Fermi energy E_F is modeled using $N_{DL,min}$ and Eq. A-2. A fit to V_{oc} vs E_F suggests a linear relation.

For devices fabricated using a CdTe deposition temperature T_{ss}=550-590 ºC, the higher deposition temperature T_{ss}=590 ºC results in devices with a higher V_{oc} (822-838 mV) and associated higher $N_{DL,min}$ ranging from 2.5-4*10^{-14} cm^{-3}. The value of V_{oc} is controlled by the separation of quasi Fermi levels of electrons and holes

$$V_{oc} = E_{Fn} - E_{Fp} \qquad \text{(A-3)}$$

If $E_{Fp}(V=V_{oc})=E_F(V=0)$ (section 3.2.4, Figure 3-8, 3-9) then theoretically, the slope dV_{oc}/dE_f=-1.

A calculation of the Fermi energy from $N_{DL,min}$ over the T_{ss}=550-590 ºC range (Eq. A-2) suggests a linear relation where

$$V_{oc}(mV) = 1090\ (mV) - \frac{0.9E_F(meV)}{q} \qquad \text{(A-4)}$$

A slope of dV_{oc}/dE_F=-0.9 is lower than expected and may the result of an overestimate of the hole concentration p where the actual value of $p<N_{DL,min}$.

Devices which are processed at a higher temperature of T_{ss}=630 ºC exhibit $N_{DL,min}$=1-4*10^{-14} cm^{-3}, but a lower V_{oc}=780-799 mV and do not fit the linear V_{oc} vs E_F model, while the calculated values of E_F based on $N_{DL,min}$ are also suspect. It is expected that an increased CdTe deposition temperature should form a higher p-type material due to CdTe thermochemistry [3]. While a higher hole concentration should result in a lowered Fermi level and hence higher V_{oc}, this is not observed with CdTe devices given a deposition temperature T_{ss}=630 ºC. However, a competing recombination mechanism which may form unwanted donor defects is increased impurity diffusion from the C065 glass into the CdTe at higher anneal temperatures which may result in the lower V_{oc} for T_{ss}=630 ºC deposited films. A relatively lower

value of $N_{DL,min}$=1.3*10^{-14} cm^{-3} for VT438.6 is not expected for a higher temperature deposited CdTe film. However, due to possible impurities which could form donor defects, the value of $N_{DL,min}$ for these devices may not accurately describe the CdTe hole density and the actual Fermi energy may be higher than that listed in Table A-5. One possibility for a lower than expected value of $N_{DL,min}$ would be the presence of a shallow donor defect which could form along with shallow acceptor p-type defects and which would affect the net hole concentration, subsequent CdTe Fermi level, and hence V_{oc}.

The space charge width of the CdTe devices at 0V varies between 1.5-3.0 μm. It can also be observed that smaller values of $N_{DL,min}$ =0.6-1.1*10^{14} cm^{-3} are associated with the larger values of space charge width (2.7-3.0 μm). One possibility for this is based upon a relation between the shallow acceptor density N_a, space charge width W, and junction charge Q from CV theory (section 2.3.4.1)

$$Q = qAN_aW \tag{A-5}$$

where A is the area. This relation assumes that the CdS layer is totally depleted of free carriers which should hold true for $W<t_{CdTe}$. The relationship also assumes that the total junction charge Q should be constant with variations in N_a and W. However, an inversely proportional relationship $N_{DL,min} \propto 1/<x>$ is not observed and better estimates of the space charge width W and doping N_a would be needed to challenge or validate the model given by Eq. A-5.

An estimate of the built in voltage V_0 can be taken using the moment of charge response <x> with $W \rightarrow <x>$,

$$<x>^2 = \frac{2\varepsilon(V_0 - V)}{qN_a} \tag{A-6}$$

and where V_0 is calculated by determining the values of the intercept $2\varepsilon V_0/qN_a$ and slope $-2\varepsilon V_0/qN_a$ with $N_a \rightarrow N_{DL}$. An analysis of V_0 for devices VT465.2 and VT481.6 was previously performed over the range -0.5 to 0V as described previously in section 4.4.2 which resulted in V_0=0.97-1.06 V. This is consistent with previously measured values of V_0~1V on polycrystalline CdTe performed using low temperature V_{oc}-T measurements [60]. A similar fitting analysis (not shown) on sample VT464.2 over the range -0.5 to 0V results in V_0=1.03 V.

However, when using Eq. A-6 with the values of $<x(V)>$ in Figure A-4 for devices developed using T_{ss}=550 ºC and T_{ss}=630 ºC, meaningful data of V_0 cannot be obtained due to the following: 1.) the $<x>^2$ vs N_{DL} plot is too nonlinear to obtain constant values of V_0; or 2.) fitting results in nonphysical values of $V_0<V_{oc}$, or values of V_0~1.5 V. Eq. A-3 was derived from C-V theory based on an assumptions of: 1.) a capacitance response is dominated by free carrier density; and 2.) 1-D carrier transport, appropriate for a device where the semiconductor layers are composed of single crystal materials. These assumptions do not hold for polycrystalline CdTe devices where the CdTe layer may exhibit deep defect states and 2-3D grain boundary defects.

A.4 JVTI Measurements and Diode Analysis

This section discusses the use of current-voltage-temperature-light intensity (JVTI) measurements to analyze the effect of CdTe deposition temperature T_{ss} on recombination activation energy E_A. The quality of the CdTe devices utilized for JVTI measurements is also evaluated.

The use of current-voltage-temperature-light intensity (JVTI) measurements were utilized to obtain diode activation energy E_A as a function of VT-CdTe deposition temperature T_{ss}, using

$$V_{oc} = \frac{E_A}{q} - \frac{AkT}{q} ln \frac{J_{00}}{J_{sc}} \qquad \text{(A-7)}$$

by extrapolating E_A from linear V_{oc} and T data ranging from 220-300 ºK and using temperature increments of 6-15 ºK. Results are shown in Figure A-6 and Table A-6.

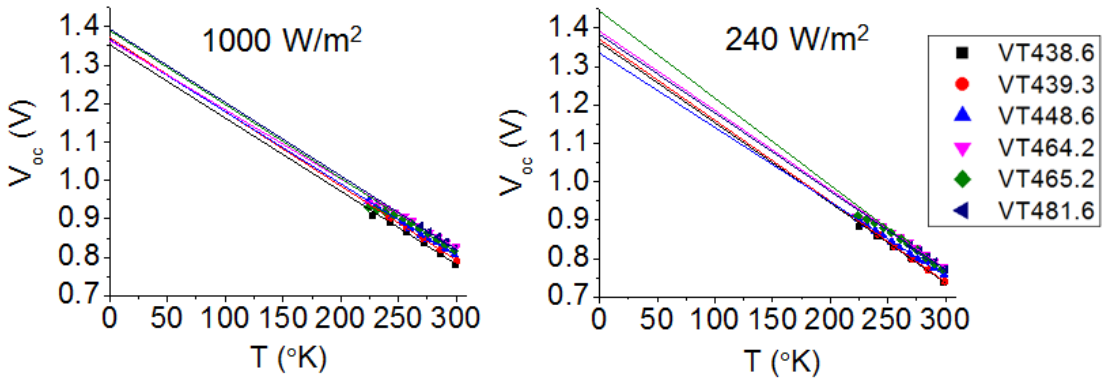


Figure A-6: V_{oc} vs T data taken at 240 W/m^2 and 1000 W/m^2 illumination intensity used to extrapolate the activation energy of recombination E_A.

Table A-6: Activation energy of recombination E_A vs VT-T_{ss}. SELH conditions→T= 300 ºK, 1000 W/m^2, and ELH bulb illumination.

Sample	T_{ss}	E_A (100%)	E_A (24%)	E_g (QE meas.)	V_{oc}(SELH)
	ºC	eV	eV	eV	mV
VT448.6	550	1.37	1.33	1.49	808-811
VT464.2	590	1.36	1.39	1.49	828-830
VT465.2		1.39	1.44	1.49	816-821
VT481.6		1.39	1.38	1.49	822-824
VT438.6	630	1.35	1.36	1.48	781-785
VT439.3		1.37	1.37	1.49	791

For V_{oc}-T data taken at 1000 W/m^2, or 250 W/m^2 there is no conclusive trend of activation energy vs T_{ss} or V_{oc} and values range from 1.35-1.44 eV. If E_A=E_g, this would suggest that V_{oc} was dominated by SRH recombination [85] [93]. However for E_A<E_g, this suggests the presence of another recombination mechanism influencing V_{oc}, possibly an interface mechanism [93]. A comparison of the activation energy E_A with the CdTe absorber bandgap, derived from QE measurements reveals a 50-160 mV difference. It is also possible that the magnitude of light intensity may vary the electric field profile across the device or at the interface.

However, the activation energy of recombination may also be influenced by device degradation. JV measurements taken initially on the devices utilized for JVTI characterization and retested prior to JVTI characterization reveal differences in FF, diode factor A and recombination current J_0 (Table A-7).

Table A-7: Values of FF, A and J_0 for characterization cells utilized for JVTI measurements. A and J_0 were derived using dark JV data at 300 ºK and linear data from dV/dJ vs 1/(J-GV) and ln(J-GV) vs V-RJ plots for J>10 mA/cm^2. Key: Initial=initial cell performance, retested=prior to JVTI analysis, I=inconclusive .

Sample	FF(STC) (initial)	FF(SELH) (retested)	A (initial)	A (retested)	J_0 (initial)	J_0 (retested)
	%	%			mA/cm^2	mA/cm^2
VT448.6	77.1	76.4	I	I	I	I
VT464.2	73.4	69.9	1.09	1.33	4E-12	7E-10
VT465.2	74.9	73	1.36	1.50	1E-9	9E-9
VT481.6	75.0	69.6	1.31	1.39	4E-10	2E-9
VT438.6	75.6	60.5	I	1.80	I	5E-7
VT439.3	78.8	63.6	I	1.70	I	3E-7

Initial STC and SELH rests reveal a decrease in FF between devices. Aside from cell degradation, a decrease in FF may also be attributed to a mismatch between the AM1.5 and ELH bulb spectrum . A decrease in FF is also associated with an increase in series resistance ΔR_s=0.6-2.9 ohm-cm^2 which may be attributed to uncontrolled lateral resistance across the sample from excessively spaced positive and negative contacts during JV testing. However, an increase in series resistance should not affect V_{oc}/recombination since $V=V_{oc}$ implies J=0 and hence the series resistance voltage drop JR_s=0.

For devices with FF<75%, dV/dJ vs 1/(J-GV) and ln(J-GV) vs V-RJ plots (Eqs. (4-2) and (4-3)) reveal an increase in recombination current and diode factor, consistent with cell degradation resulting in a SRH mechanism due forming after initial testing. Due to the nonlinear dV/dJ vs 1/(J-GV) and ln(J-GV) vs V-RJ behavior associated with FF≥75% devices (see section 4.3.2 for examples and a discussion), meaningful results of A and J_0 cannot be obtained for an initial/retest comparison.

A.5 Conclusions

For CdTe devices fabricated using a vapor transport deposition temperature T_{ss}=550-630ºC, the best V_{oc} performance is observed for CdTe deposited at 590 ºC, while the optimal J_{sc} performance is observed for CdTe deposited at 630 ºC. The use of QE measurements suggest that a greater photocurrent collection (Jsc) occurs at 630 ºC due to a greater blue QE response which is consistent with a thinner CdS layer and subsequent higher sulfur diffusion into CdTe, suggested by a relatively smaller 1.48 eV bandgap. The use of QE and JVTI measurements also suggest a consistent Urbach energy E_U and activation energy of recombination E_A over the T_{ss}=550-630 ºC range and hence, the variation in V_{oc} over the T_{ss} range does not appear to depend on E_A or E_U. DLCP measurements suggest CdTe hole concentration ranging from 0.6-4*10^{14} cm^{-3} and a space charge width of 1.5-3 µm. The variation in T_{ss}=550-590 ºC results in a higher value of $N_{DL,min}$ for T_{ss}=590 ºC consistent with an increase in p-doping and associated decrease in Fermi energy. This however cannot be concluded for the lower V_{oc}, CdTe devices fabricated with VT T_{ss}=630 ºC where the observed decrease in V_{oc} may occur due to the formation of an unwanted defect, possibly due to contamination from the C065 glass.

Appendix B

QUANTUM EFFICIENCY: THEORY OF LONG WAVELENGTH MEASUREMENTS

This appendix provides a detailed description of quantum efficiency theory used to determine CdTe optoelectronic properties performed at photon energies below the CdTe bandgap of 1.5 eV.

The use of long wavelength quantum efficiency (QE) measurements with λ=800-900 nm are utilized to measure the CdTe bandgap and qualitatively measure CdTe grain disorder via Urbach bandtail energy measurements, as discussed below.

In the infrared region from λ=800-900 nm, the QE begins to drop as the photon energy becomes smaller than that of the CdTe bandgap. In this region, light entering the cell is nearly uniformly absorbed in the CdTe layer. Thus, this method gives insight into the properties of the CdTe bulk layer. By subjecting the cell to reverse bias vs. 0V and light vs. dark conditions, the response of bulk/interface defects to illumination and changes in the depletion width can be observed. For a purely intrinsic direct bandgap CdTe material, one might expect a sharp cutoff in absorption below the material bandgap. However, due to the presence of band tail states in CdTe, the absorption edge behaves exponentially with photon energy hυ so that

$$\frac{d(ln(\alpha))}{d(h\upsilon)} = \frac{1}{E_U} = \frac{1}{\gamma kT} \qquad \text{(B-1)}$$

where E_U is the Urbach energy. This is known as Urbach's rule [51]. The Urbach energy is a measure of crystal disorder with decreased values of E_U associated with increased grain size and decreased crystal disorder [52].

A relation between $\alpha(\lambda)$ and QE for long wavelength light with $\lambda \geq 850$ nm and at no applied bias (V=0) can be derived based on the following assumptions: 1.) light is incident on the window side of a window/CdTe device, where light absorption only occurs in the CdTe layer; 2.) the wavelength is sufficiently large that no parasitic absorption occurs in the glass/CTO/ZTO/CdS window layers; 3.) 1-D carrier transport physics [118] which are governed by the CdS/CdTe n-p junction; 4.) uniform charge density within the CdS and CdTe layers resulting in a depleted CdS layer, and CdTe layer with a space charge width $W >> t_{CdS}$ and neutral bulk region with no electric field [95], [118]; 5.) the CdTe device is thick enough where t_{CdTe}=4-9 μm, with a corresponding space charge width =1-3 μm and diffusion length $L<1$ μm [60] such that the back barrier does not influence photocurrent; 6.) for long wavelength light, the value of the CdTe absorption coefficient $\alpha(\lambda)<10^3$ cm^{-1} and hence $\alpha(\lambda)L$, $\alpha(\lambda)W$, $\alpha(\lambda)t_{CdTe} << 1$. Based on the above assumptions a relation between $\alpha(\lambda)$ and $QE(\lambda)$ is obtained [118],

$$\alpha(\lambda) = \frac{QE(\lambda)}{(1 - R(\lambda))(L + W)} \tag{B-2}$$

Using this information, the material bandgap can be determined from the QE as follows. By taking Eqs. (B-1) and (B-2) and by assuming that $R(\lambda)$ is constant in the IR region of interest, a linear relation is found between ln(QE) and the photon energy E.

$$\ln\big(QE(E)\big) = (E/E_U) + C_1 \tag{B-3}$$

By letting ln(QE)=x, E=hυ and extrapolating ln(QE) to the E-axis, where where QE=1, the band tail energy E_0 can be determined. Then, Eq. (B-3) can be rewritten as

$$\ln\big(QE(E)\big) = \frac{(E - E_0)}{E_U} \tag{B-4}$$

If an approximation of E_0=E_g is made [119], the CdTe bandgap can be estimated. The data should be fit over a region where

$$\frac{d}{dE}\ln\big(QE(E)\big) = const \tag{B-5}$$

Appendix C

BACK BARRIER FITTING

This appendix section discusses fitting approaches and modeling used to determine the back barrier Φ_b.

Consider the circuit model for CdTe J-V measurements taken in the dark (Figure C-1).

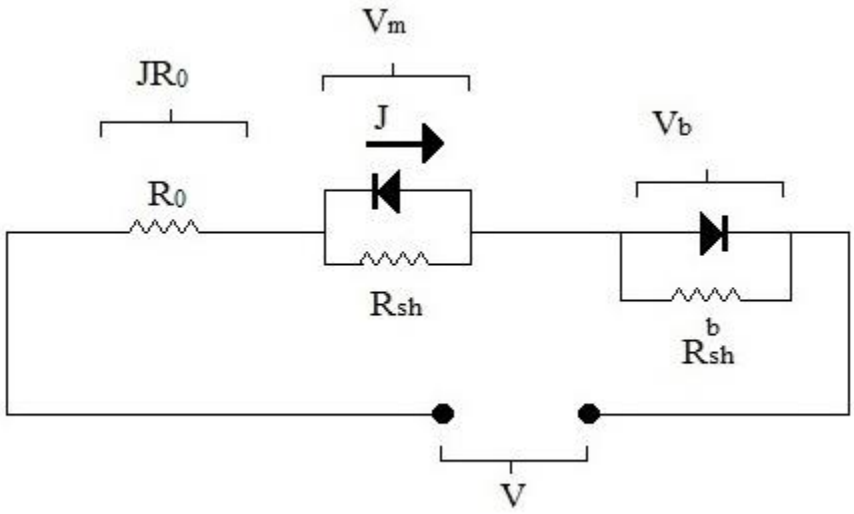


Figure C-1: CdTe device with a back contact.

Using the circuit model in Figure C-1, the current through the back contact in forward bias is modeled as [120],

$$J = -J_t(\exp\left(\frac{-qV_b}{kT} - 1\right) + {V_b}/{R_{sh,b}} \quad \text{(C-1)}$$

with V_b as the voltage across the back contact and J_t as the turning current [96],

$$J_t = A(T)^* T^2 \exp(\frac{-q\Phi_b}{kT}) \quad \text{(C-2)}$$

where A(T)* is the effective Richardson constant [121] and $A(T)^* \propto T^{-3/2}$ [120] while Φ_b is the back barrier.

For a CdTe device at T<300 º K and forward biased above 1 V, the back barrier affects the J-V characteristics and the turning current J_t can be derived from these characteristics. This is shown in Figure C-2.

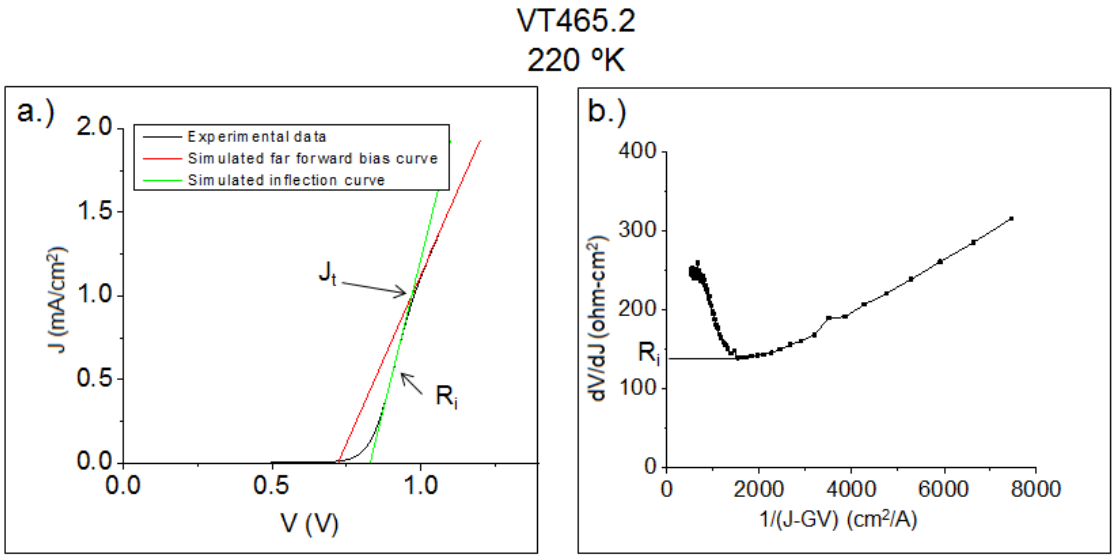


Figure C-2: a.) Turning current J_t, found by linear fits taken in far forward bias where back contact shunting dominates the J-V curve and around the inflection point where dV/dJ=0. b.) Determination of the inflection point resistance Ri where dV/dJ=0. The upward curvature for 1/(J-GV)<2000 cm^2/A is the result of the back contact.

The turning current J_t is found by the intersection of two linear fits: 1.) where back barrier shunting dominates (Eq. (C-1) with $J \sim V_b/R_{sh,b}$) and from the inflection point in the J-V data which is the point where dV/dJ=0, giving an dV/dJ intercept R_i. If the temperature dependence of $J_t(T)$ is dominated by the exponential term $\exp(\frac{-q\Phi_b}{kT})$ in Eq. (C-2), then

$$-\ln(J_t) = const + \frac{q\Phi_b}{kT} \tag{C-3}$$

Then, an Arrhenius plot of ln(Jt) vs 1/T can be utilized to determine the back barrier Φ_b.

Another J-V fitting method to determine Φ_b is as follows [4]. For back barrier voltage $V_b << kT$,

$$J \sim -J_t\left(1 - \frac{qV_b}{kT} - 1\right) \tag{C-4}$$

$$= A(T)^* T^2 \exp\left(\frac{-q\Phi_b}{kT}\right)\left(\frac{qV_b}{kT}\right)$$

The contact resistance of the back contact R_c is then defined as

$$R_c = \frac{V_b}{J} = \frac{k}{qA(T)^* T}\exp\left(\frac{q\Phi_b}{kT}\right) \tag{C-5}$$

where

$$R_s = R_0 + R_c \tag{C-6}$$

is the total series resistance which is the sum of the temperature dependent contact resistance R_c and temperature independent series resistance R_0. If the contact resistance R_c is dominated by the exponential term $\exp(\frac{-q\Phi_b}{kT})$, then

$$\ln(R_c) \sim const + \frac{q\Phi_b}{kT} \tag{C-7}$$

or

$$\ln(R_s - R_0) \sim const + \frac{q\Phi_b}{kT} \tag{C-8}$$

with R_s estimated from Eq. (4-2) and $R_0 \sim R_s$ at high temperatures. Hence, the back barrier Φ_b can be derived from the slope of an Arrhenius temperature plot of $\ln(R_s-R_0)$ vs 1/T.

Appendix D

PREVIOUSLY PUBLISHED MATERIAL

Portions of the text and graphics included in this dissertation have been previously published in the IEEE-Photovoltaic Specialist Conference publication "CdTe solar cells with a PCBM back contact" by Walkons, Guralnick, McCandless, and Birkmire [116].

Reuse of the previously published material in the present work is expressly permitted by IEEE as stated on the publisher's website at https://www.ieee.org/publications_standards/publications/rights/permissions_faq.pdf (accessed 30 March 2016) and excerpted here:

> "The IEEE does not require individuals working on a thesis to obtain formal reuse license, however, you must follow the requirements listed below:
>
> …In the case of illustrations or tabular material, we require that the copyright line © [Year of original publication] IEEE appear prominently with each reprinted figure and/or table."