INTERDIGITATED BACK CONTACT SILICON HETEROJUNCTION SOLAR CELLS: ANALYSIS WITH TWO-DIMENSIONAL SIMULATIONS

by

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ABSTRACT

Interdigitated back contact silicon hetero-junction (IBC-SHJ) solar cells using a-Si emitter and contact layers show significant potential advantages over standard hetero-junction devices: higher short-circuit current (J_{sc}) since there is no grid shading and higher open-circuit voltage (V_{oc}) due to better surface passivation. However, they often suffer from low fill factor (FF). IBC-SHJ processing steps include two separate photoresist masks for doped amorphous silicon depositions, and all amorphous layers are deposited using Plasma Enhanced Chemical Vapor Deposition (PECVD). The thicknesses of the front surface layers are optimized so that reflection and absorption are minimized. Measurement techniques, such as current-voltage, reflection, and quantum efficiency, were used to characterize the experimental devices. These techniques were also investigated in simulations to match modeled data to experimental results. Using two-dimensional simulations to model IBC-SHJ devices on Float Zone (FZ) n-Si, we found that the FF was nearly independent of the defect concentrations in contact and passivating i-layers but strongly dependent on the defects in emitter and the band gap in the rear i-layer. V_{oc} and J_{sc} were nearly independent of defects in either doped layer. In a-Si doped layers it is well known that the number of defects increase with doping. We find that the FF is sensitive to either mid-gap or band tail states and that S-shaped JV curves responsible for low FF can be eliminated by a decrease in p-layer mid-gap or band tail defect levels, or by decreasing the rear i-layer's band gap. The insensitivity of FF to defects in the n-layer or in the i-layer suggests the FF is dominated by minority carrier

injection/collection from the p-type emitter layer. The dependence of FF on the rear i-layer band gap suggests that increasing the offset in the valence band impedes minority carrier collection. Rear-surface geometry, wafer resistivity, and wafer lifetime and thickness were also investigated in simulations, and their results are shown. With the advancement of IBC-SHJ technology, new device structures, such as larger cells with more interdigitated fingers, will be fabricated and simulated.

Chapter 1

INTRODUCTION

As the demand for fossil fuels continues to increase, the interest and development in solar electricity as a sustainable renewable energy source also rises. The ultimate goal is to increase solar cell device and module performance and simultaneously to lower costs. These conflicting goals must be achieved, both in manufacturing and installation. The first silicon solar cell was created by Russell Ohl in 1941 [1]. Today, crystalline silicon is the leading material in solar panels throughout the world. However, even with the high efficiencies achieved with this type of solar cell, the cost of making thick, crystalline wafers is still too high because of the use of excess silicon and high temperature processing. As wafers get thinner, though, traditional solar cell designs begin to fail since they require high temperatures and thick pastes, which lead to thermal expansion problems (warping) on thin wafers. Also, as the thickness decreases, the requirement for very well passivated surfaces increases. Thus, there has been a move to incorporate amorphous silicon into the device design concept, which would allow for processing thinner wafers at lower temperatures with excellent passivation due to the heterojunction.

1.1 Solar Energy and Photovoltaics

On a clear day, approximately 4.4×10^{17} photons strike an area roughly 1 cm^2 of the Earth's surface every second [2]. Figure 1.1 shows the spectral distribution of the irradiance of these photons as a function of their respective wavelengths [3]. The

AM0 spectrum represents sunlight outside of the Earth's atmosphere. AM1.5 (Air Mass) is the accepted spectrum used to measure solar cells at the terrestrial level. The 1.5 correlates to the fact that radiation has passed through an equivalent thickness of 1.5 times the Earth's atmosphere. This is the level of the solar zenith angle; around 48.19 °s [3]. The photons that have energy greater than the band gap of the solar cell can be converted into electricity. These photons, when absorbed by the semiconductor, can promote an electron from the valence band to the conduction band. This leaves a hole behind in the valence band, and thus creates an electron-hole pair. All electron-hole pairs have energy greater than the band gap. As soon as they are created, the electron and hole decay to states near the edges of their respective bands. The excess energy is lost as heat, and this represents one of the fundamental loss mechanisms in solar cells, as shown in Figure 1.2.

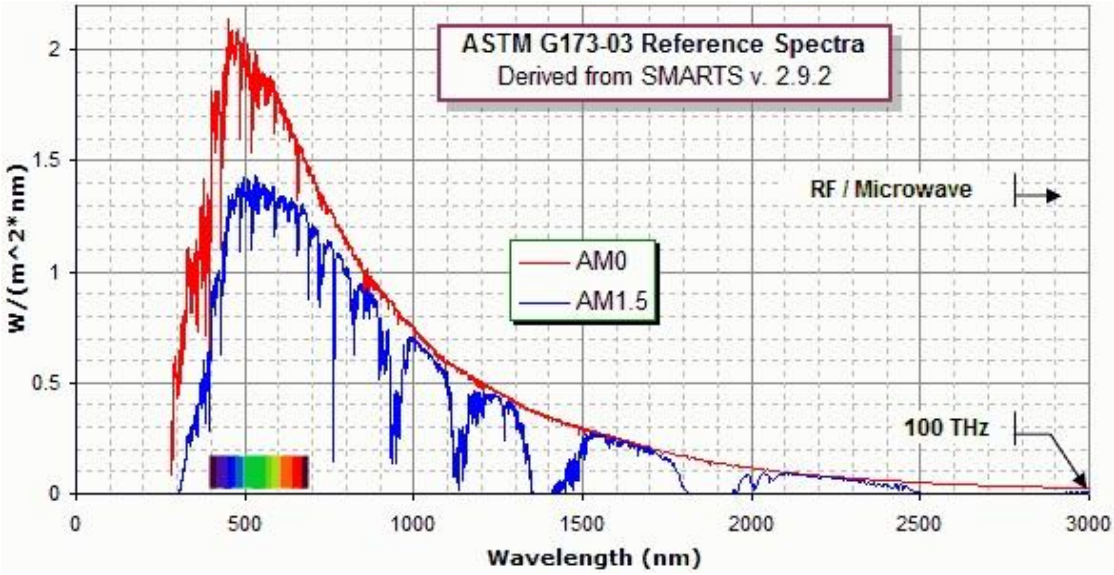

Figure 1.1 The AM0 and AM1.5 solar spectrum [3].

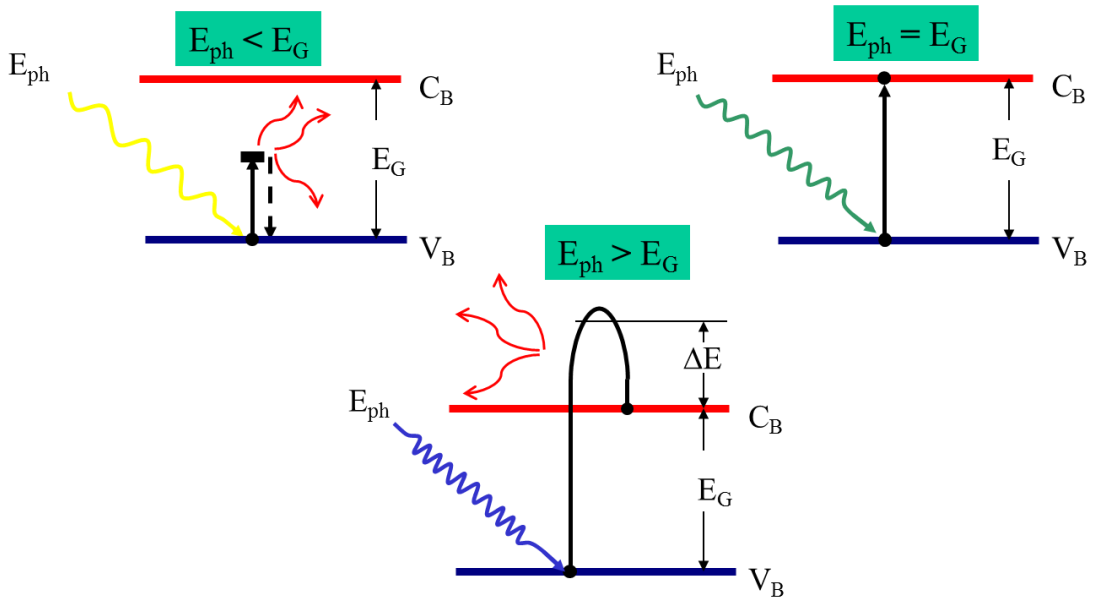

Figure 1.2 **Photons of energy greater than (center) or equal to (right) the band gap can promote an electron from the valence band to the conduction band, leaving a hole behind. Photons of energy less than the band gap (left) only result in heat dissipated to the lattice, but no electron or hole generation.**

1.2 SHJ Solar Cells and Advantages

Amorphous/crystalline silicon heterojunction (SHJ) solar cells carry several advantages over standard thick crystalline wafer solar cells. The main advantage of the SHJ device is their simple fabrication processing and very high cost-reduction potential. The low temperature processing prevents carrier lifetime degradation, typically with temperatures equal to or less than 250 °C [4]. This type of solar cell has superior passivation of the bulk material and wafer surface, which yields an excellent back-surface field. This gives the SHJ cell an advantage with higher open-circuit voltages (V_{oc}). In fact the only solar cells with V_{oc} > 700 mV have been SHJ devices or some variation thereof. Figure 1.3 shows the standard structure of a SHJ solar cell tested at IEC. This type of device was first used to establish an understanding of the

fundamental issues in SHJ device processing and to validate the code in modeling photovoltaic structures using Sentaurus.

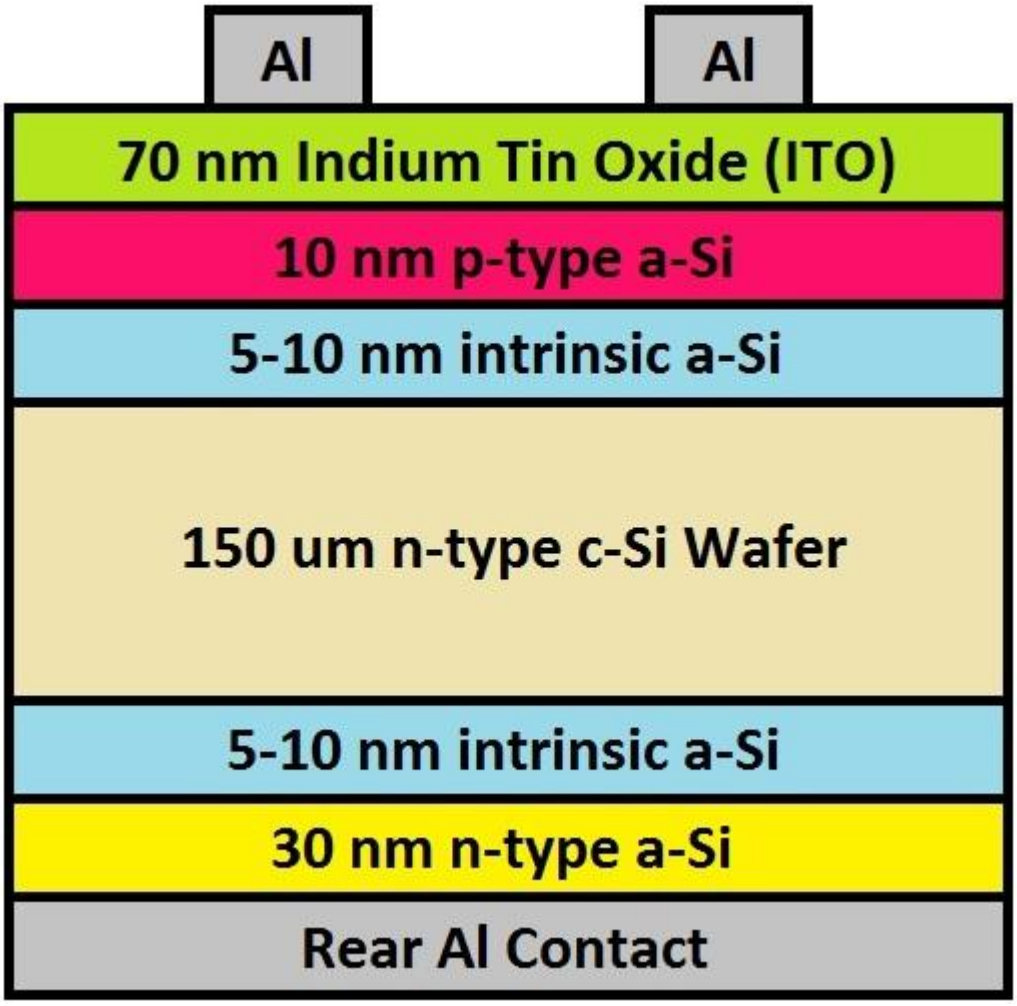

Figure 1.3 Device diagram of a SHJ solar cell. SHJ cells have several advantages over thick crystalline wafer cells.

1.3 IBC Solar Cells and Advantages

Interdigitated back contact (IBC) solar cells are a technological advancement over the standard SHJ devices. The front surface of the IBC cells tends to be more homogeneous than SHJ cells because both contact grids are on the rear side of the device [5]. Front-contacted solar cells can have up to 10% shading loss when using screen-printed metal grids, and so, IBC cells add the potential for higher short-circuit currents (J_{sc}) because they have no reflection loss caused by grid shading [6]. IBC cells allow for easier module interconnection, which lowers costs even further than SHJ cells. Because there is no need to conduct current laterally along a diffused emitter, like a standard n+/p device or along a transparent conductor like the SHJ cell does, there is no trade-off between grid shading and series resistance [7].

The focus of this paper is on the combination of the two cell structures, which form the interdigitated back contact silicon heterojunction (IBC-SHJ) solar cell. These devices were first suggested by IEC, who has pioneered and patented the concept, in 2006 [8]. IBC-SHJ devices have all of the advantages of SHJ and IBC cells, including higher V_{oc} and J_{sc}, and no trade-off between optical losses and series resistances due to contact grids. The combination of the two separate device types also reduces the optical and electrical limits that each experience separately. The introduction of the IBC into the SHJ removes the absorption loss that the emitter and intrinsic amorphous silicon layers would normally experience. Likewise, the introduction of the SHJ into the IBC allows the rear side of the device to have an increased V_{oc} due to low surface recombination velocity. They do, however, suffer from low fill factor (FF), and a major focus of this research has attempted to determine methods of improving this parameter through modeling. Though the content of the

presented research describes the modeling of a two-cell IBC-SHJ structure, the model is currently being changed to accurately simulate an improved device structure.

1.4 Thesis Topics

The goal of this research is to establish areas of improvement in the IBC-SHJ solar cells that are currently being developed through the use of two dimensional modeling. Chapter 2 discusses the processes that are incorporated into the creation of this device. Rear surface geometry and front surface optics are also described. Chapter 3 lists the measurement techniques used to characterize experimental cell results that are used to match the model to experiments. These involve reflection, current-voltage, and quantum efficiency measurements. The theory behind each technique is also disclosed. Chapter 4 introduces the reader to the TCAD program Sentaurus that is used to model the IBC-SHJ device results. Each section of code used to program the physics behind all layers in the structure is discussed. Chapter 5 shows results from simulations of IBC-SHJ devices. The effects of the band gap of the rear intrinsic amorphous silicon layer and the defect levels in the emitter layer are the main interest. Chapter 6 includes a summary of the work, and how the techniques described can be applied to new device structures, such as to larger IBC-SHJ cells with different rear-surface geometries.

Chapter 2

INTERDIGITATED BACK CONTACT SILICON HETEROJUNCTION SOLAR CELL DEVICE

The IBC-SHJ solar cell consists of several thin film layers including amorphous silicon layers deposited on both sides of a crystalline silicon wafer. The layers on the front surface of the wafer are responsible for the optical performance of the device, and their thicknesses are fine-tuned accordingly to minimize absorption and reflection. The IEC has developed a unique multilayer stack consisting of three layers: amorphous silicon carbide (a-SiC:H), amorphous silicon nitride (a-SiN_x:H), and intrinsic amorphous silicon layer (intrinsic a-Si:H). The rear surface of the wafer has an additional intrinsic a-Si:H layer, along with the interdigitated doped amorphous silicon fingers (p- and n-type a-Si:H) and aluminum metal contacts. The gaps in between the fingers are passivated using SiN_x. This chapter discusses the fabrication and processing of the IBC-SHJ solar cell. Figure 2.1 shows the basic structure of the IBC-SHJ solar cell, Figure 2.2 shows the processing steps in device creation, and Figure 2.3 depicts the in-line PECVD system used at IEC.

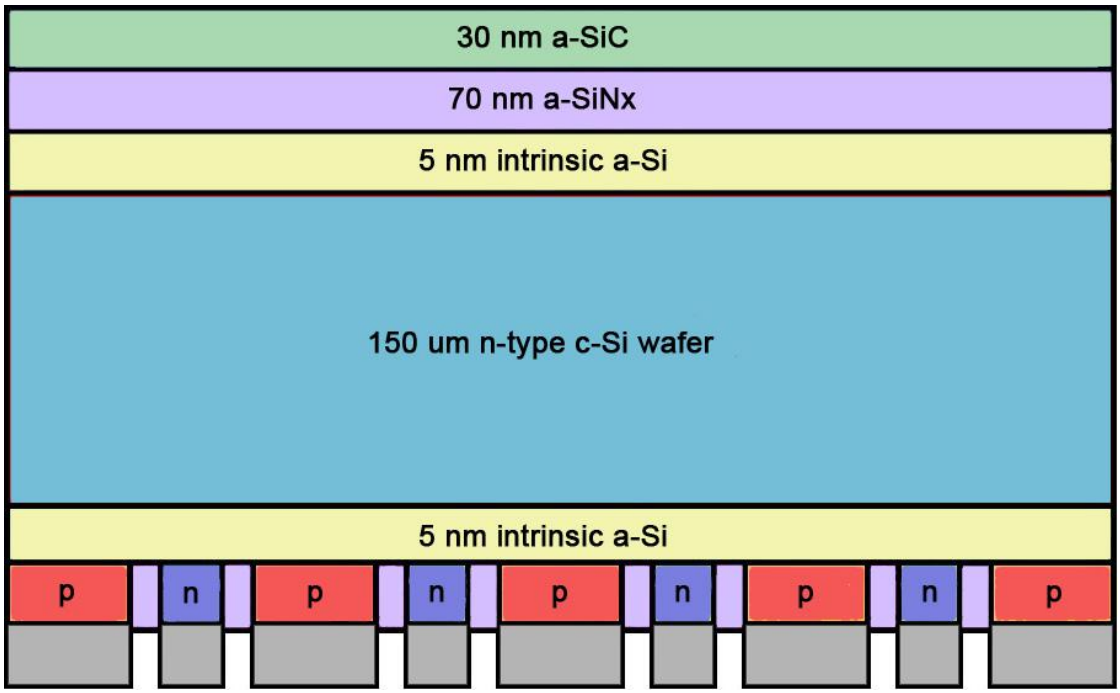

Figure 2.1 **Diagram of an IBC-SHJ solar cell. The device has three front surface optical layers, is passivated by intrinsic a-Si:H on both sides of the wafer, and has interdigitated doped amorphous fingers on the rear side. The fingers are capped with a 0.5 um aluminum contact, and SiN_x passivates the gaps between the fingers. The width of the fingers are either 1200-500 um or 1400-250 um (p-n).**

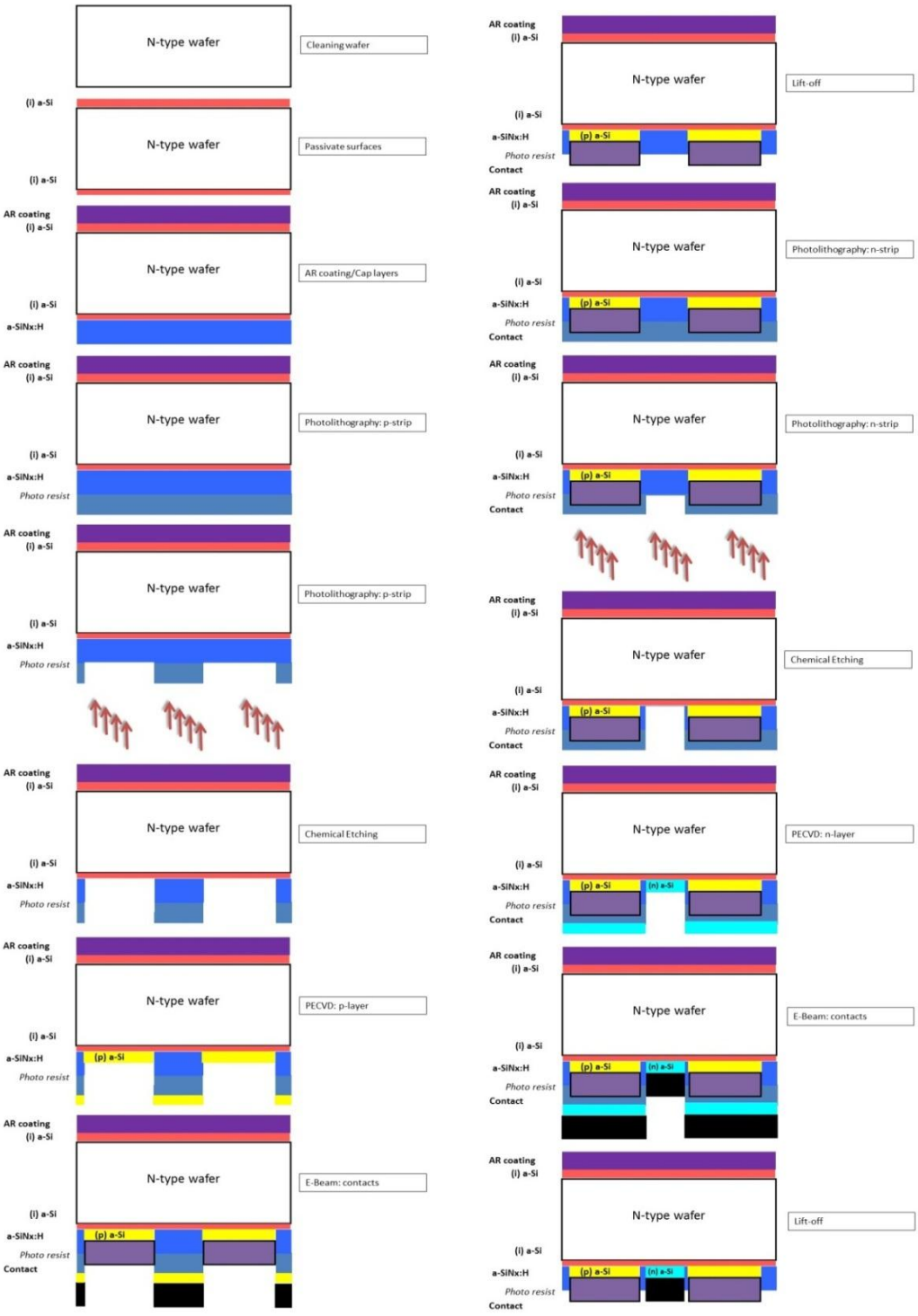

Figure 2.2 Processing steps performed in fabricating an IBC-SHJ solar cell. 'AR Coating' incorporates both a-SiN_x:H and a-SiC:H.

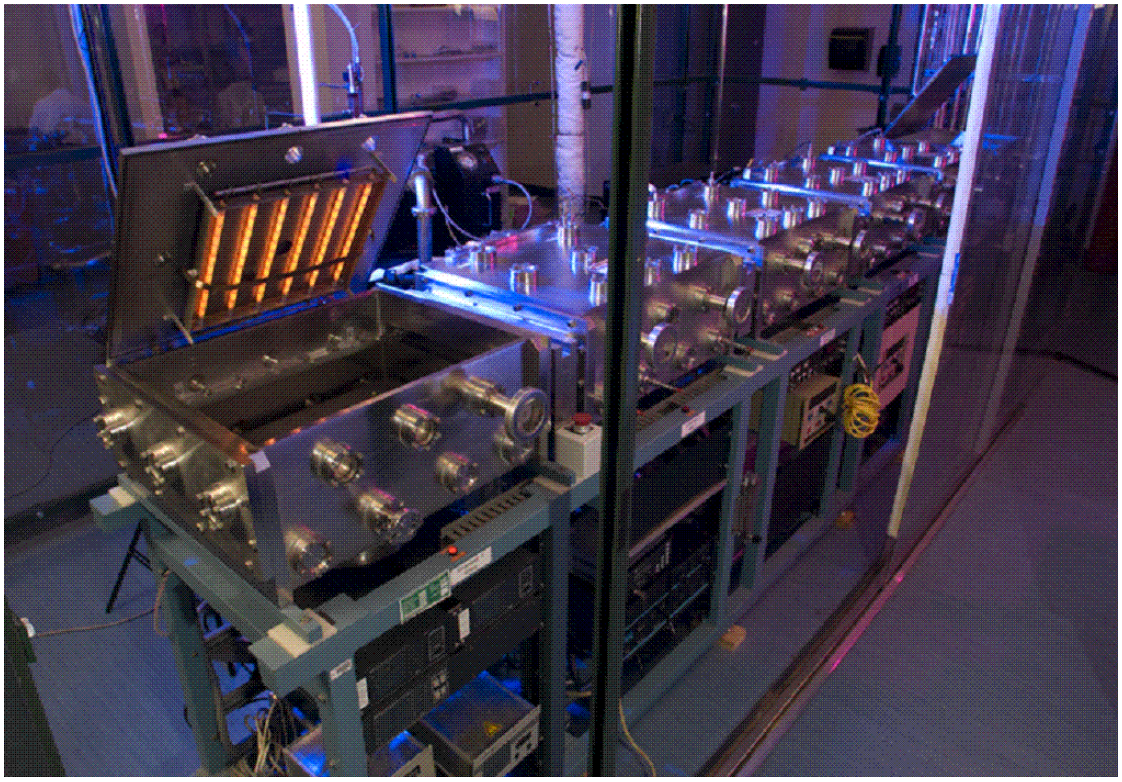

Figure 2.3 Six-chamber in-line PECVD system at IEC.

2.1 c-Si Wafer

Both polished and textured crystalline wafers were used for the IBC-SHJ experiments. The wafers were n-type, created from the Float Zone (FZ) technique, and were 150 um thick. N-type Si material has been proved to be more suitable for IBC solar cells due to its larger tolerance to most common impurities compared to p-type Si. Previous simulations of IBC-SHJ solar cells based on p-type c-Si had pointed out several limiting factors, including the front surface passivation, the quality of the intrinsic amorphous silicon/crystalline silicon interfaces, and the quality of the contacts. By using FZ wafers [9], silicon crystal of higher purity and longer minority

carrier lifetimes are achieved, compared to wafers formed by the Czochralski process. The resistivity of the wafers is 2.5 Ωcm, and they are oriented in the (100) direction. All wafers undergo a thorough cleaning using a wet chemical process.

The cleaning of the polished silicon begins with a five minute dip in acetone, and is followed by a five minute dip in methanol. The wafers are then rinsed off with isopropyl alcohol and are given an additional five minute rinsing in de-ionized (DI) water. Next, the wafers are dipped into a sulfuric acid and hydrogen peroxide mixture, or piranha etch, at a 2:1 ratio for five minutes. The purpose of this etch is to grow a native oxide and gather residual solvent on the wafer. This is followed by another five minute DI rinsing. The last cleaning step for a polished wafer is a bath in a 10% concentrated hydrofluoric acid (HF) solution for one minute. Pre-textured wafers experience further cleaning steps after the HF bath. A solution of 5% tetramethylammonium hydroxide (TMAH) with Triton X-100 surfactants covers the wafers for 10 minutes. The temperature of the wafers is held between 60 and 70 °C for this cleaning. This is followed by a five minute rinse in DI water. The piranha etching, an additional DI rinse, and the HF etch follow again after this last step.

2.2 Anti-Reflective Layers

The front surface optical layers are all deposited using plasma-enhanced chemical vapor deposition (PECVD). The intrinsic a-Si:H layer is deposited between 200 and 250 °C and undergoes a 25 minute in-situ vacuum annealing at 300 °C. The passivation quality of this layer degrades if the deposition is made at lower temperatures. The a-SiN_x:H is deposited at 300 °C, and the a-SiC:H is deposited at 200 °C. The RF power used is 40 W for the a-SiN_x:H and between 20 to 60 W for the

intrinsic a-Si:H. The deposition pressure in the chamber is 1.25 Torr for all amorphous layers with the exception of the carbide and intrinsic layers, which are deposited under a pressure of 500 mTorr. The flow of SiH_4 in the chamber has been both 20 and 16 sccm for the devices over the course of the research. The RF plasma frequency is set at 13.56 MHz. The a-SiC:H layer is used to protect the a-SiN_x:H layer during the back surface processing steps, and the a-SiN_x:H layer improves the passivation quality of the intrinsic a-Si:H layer. Passivation quality is also not lost with the deposition conditions of the carbide and nitride layers.

2.3 Rear Passivating Layer and Gap Passivation

The rear i-layer has an important role as it is used for high quality current transport at the interfaces on the back surface of the device. Like the front surface i-layer, this layer is deposited at 200-250 °C and then has a 25 minute vacuum anneal at 300 °C. The properties of the rear intrinsic a-Si:H layer was a key point in this research, as it affects both open-circuit voltage and fill factor. The results on the study of the rear i-layer are discussed in chapter 6. A layer of SiN_x is deposited using PECVD at 300 °C onto the rear intrinsic a-Si:H layer. After several photolithography and a-Si doped layer deposition steps result in formation of the interdigitated doped a-Si:H layers, the remaining SiN_x is used to passivate the gaps between the fingers.

2.4 Doped Amorphous Layers and Device Contacts

Two sets of interdigitated p- and n-doped a-Si:H layers are deposited on the rear surface of the device. Both layers are deposited using PECVD, incorporating photolithography processes, at a lower temperature of 175 °C. The p-type fingers are

deposited first, and then aluminum contact deposition follows. Next, the same steps are used to deposit the n-type fingers and their respective aluminum contacts. The masks defining the p- and n-layer metal contact fingers are aligned using a mask aligner using multiple registration marks. The aluminum is deposited using electron-beam evaporation at a thickness of 0.5 um.

2.5 Front Surface Optics

The three layers on the front surface of the c-Si wafer are responsible for how much light reaches the wafer. The thicknesses are optimized at 30 nm for the a-SiC:H and 70 nm for the a-SiN_x:H. The thickness of the intrinsic a-Si:H layer is 5 nm. Their combined thickness is adjusted for minimum reflection [10]. These thicknesses yield a minimum current density loss of 2.04 mA/cm^2. Other front surface optical structures were investigated, such as replacing the a-SiC:H and a-SiN_x:H with ZnS films, but the triple stack structure yields the highest device results.

2.6 Rear Surface Geometry

Masks were designed such that there are two cells fabricated on each 1"x1" c-Si wafer, as shown in Figure 2.4. The difference between the two cells is the width of the interdigitated doped a-Si:H layers. One cell has p-n-gap width dimensions of 1200-500-25 um, and the other has width dimensions of 1400-250-25 um. With five p-type fingers and four n-type fingers, there are eight gaps and the total width of one cell is 8.2 mm. Various other geometries were studied in this research, and the results of some of the simulations are discussed in chapter 5. Two processing steps limit cell performance in regards to the fingers: the positive photoresist masking material and

the alignment of the masks. The photoresist material cannot withstand high temperatures, and thus, the PECVD deposition is limited to a temperature of 175 °C. Alignment of the p- and n-type fingers is also difficult, especially while incorporating a gap width of only 25 um. If the fingers overlap or come in contact with one another, shunting occurs in the device.

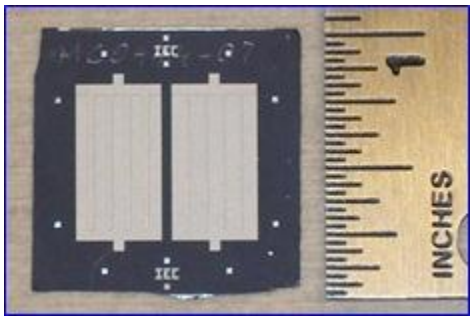

Figure 2.4 **Rear view of IBC-SHJ substrate. Two devices are processed onto one c-Si wafer. The total width of the cells is equal, but the rear surface geometries differ. The small aluminum tabs are where the contact probes are placed for testing. The first cell (left) has 1200 µm-wide p-strips and 500 µm-wide n-strips. The second cell (right) has 1400 µm-wide p-strips and 250 µm-wide n-strips. Both cells have 25 µm-wide gaps. The length of the strips and gaps is 1.3 cm, the width of the aluminum connecting the strips is 0.1 cm, and the dimensions of the contacts pads are 0.1x0.1 cm^2.**

Chapter 3

OPTICAL AND ELECTRICAL CHARACTERIZATION

The basis of this work was to establish a verifiable model of device performance of the IBC-SHJ solar cell. This was done by matching experimental data with simulated results of reflection, external quantum efficiency, and current-voltage data measurements. Though the experiment and model comparison is made in chapter 5, chapter 3 discusses these three types of measurements in detail.

3.1 Ultraviolet-Visible Spectrometer

Reflection measurements were made on IBC-SHJ devices using a PerkinElmer Lambda 750 Spectrophotometer. Figure 3.1 shows the schematic of the internals of this equipment. Two lamps are used for the full length of the spectrum of the IBC cells, which ranges from 300 nm to 1200 nm. A tungsten lamp operates for all wavelengths above 320 nm, and a switch is made to a deuterium lamp at 319.20 nm. A monochromator spreads the light across gratings, and shines it through a 2 nm-wide slit. This beam is then split into two signals; one for a sample beam, and one for a reference beam. After traveling through attenuators and sample compartments, the two signals meet in the integrating sphere, where the resulting data can be analyzed. The integrating sphere has three holes which are blocked by different combinations of reflecting plates and samples. For transmission measurements, the sample is placed on the front of the integrating sphere so that the light passes through the sample before proceeding into the sphere. Two diffuse reflecting plates cover the two exit holes on

the sphere for this type of measurement. For reflection measurements, the rear diffuse reflecting plate is replaced by the sample, and the front of the sphere is left clear for the light to pass through. In the case of reflection, the system is first calibrated by an auto-zero correction using either a diffuse or specular reflecting plate on the rear-side of the integrating sphere, depending on whether the sample is textured or planar, respectively. In the case of transmission, the system is always auto-zeroed using the diffuse reflecting plate. The wavelengths are scanned in 1 nm intervals.

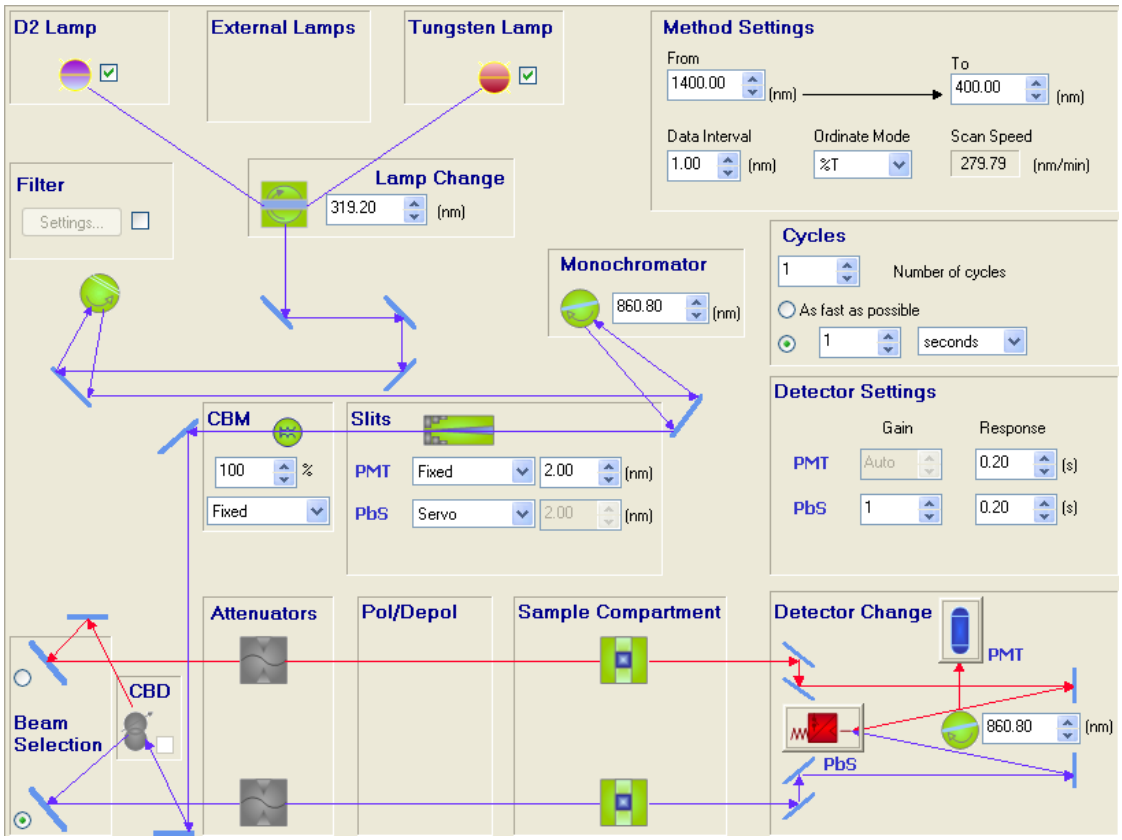

Figure 3.1 Equipment schematic of UV-Vis Spectrophotometer.

The sample beam incident on the device has a vertical crescent shape roughly 1.5 cm tall and 0.75 cm wide. It is tall enough to get a good coverage area of the device, and at the same time, narrow enough so that no light is reflected off of the metal clips that hold the samples in place during transmission measurements. The importance of reflection measurements is that it serves as an early check to make sure the model is matched to experimental data. Because the reflection measurement is purely optical, if the model cannot calculate the same reflection curve, then there is something wrong with how the layers are represented optically in the model; this problem is easy to isolate. Figure 3.2 shows the measured front surface reflection from one of the devices used for modeling. It has a textured Si surface with the multilayer AR (intrinsic a-Si:H, a-SiN_x:H, and a-SiC:H) stack discussed in Chapter 2.

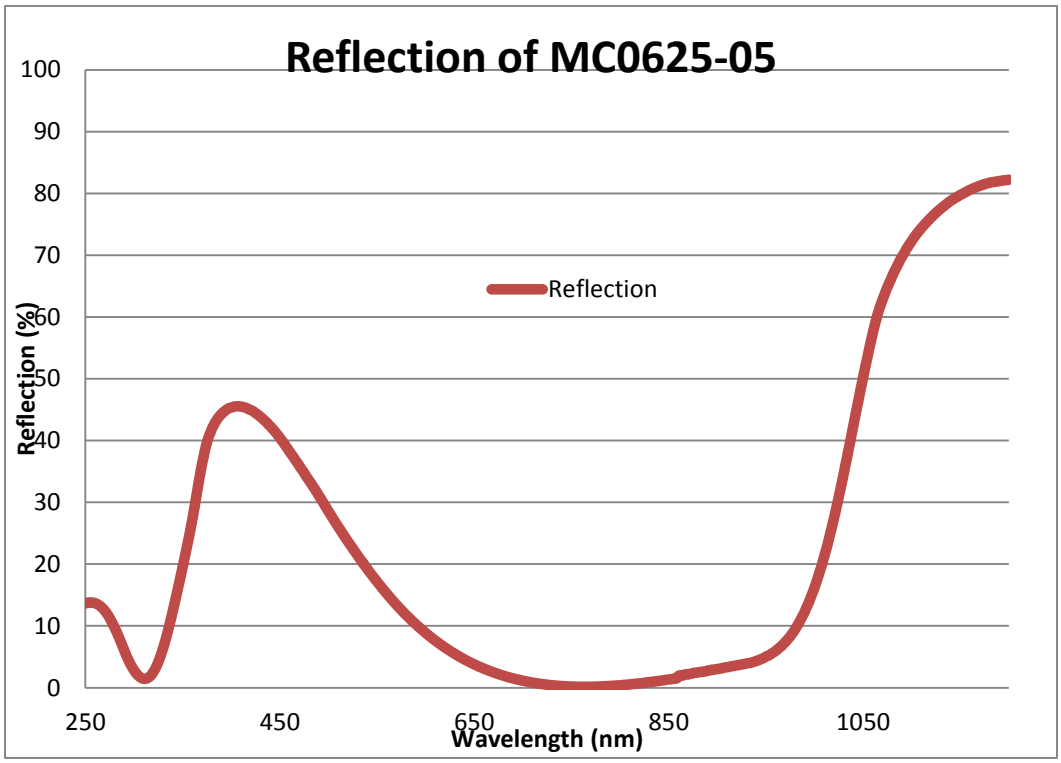

Figure 3.2 Reflection curve of MC0625, which is a device used in simulations.

3.2 Current-Voltage Analysis

Current-Voltage curves, or JV curves, are the first measurement performed on finished IBC-SHJ solar cells. They consist of illuminating a solar cell with light close to the AM1.5 spectrum, and then measuring current while voltage is applied across the device. The intensity of the light is at 1000 W/m^2, and the sample temperature is kept at 25±1 °C using forced air cooling. These conditions are known as the 'standard test conditions.' The four main parameters extracted from JV curves are V_{oc}, J_{sc}, FF, and efficiency. The devices are contacted using the four-point probe technique, which is designed to eliminate the series resistance in the measurement leads from the source measurement unit (SMU) and contact resistance between the leads and the device. Figure 3.3 is a diagram of the four-point probe technique. From this setup, no current flows in the loop containing the voltage source, and thus, there are no voltage drops due to series or contact resistance [11]. Eliminating parasitic resistance allows more accurate measurement of the intrinsic junction properties and device performance, specifically the FF.

The illumination comes from a 1000W Xenon Arc Lamp, which is seated in an elliptical reflector which also collimates the light. The light reflects upwards and then horizontally off of a mirror, coming to an AM1.5 filter. Once filtered, the light reflects from another mirror, passes through TEC15 glass that acts as a filter, and reaches the device. A shutter is used to control when the light is or isn't illuminating the solar cell for light and dark JV curves. Two kelvin probes with two contacts each are used to make electrical contact to the aluminum electrodes on the IBC-SHJ device.

In addition, a temperature sensor is placed on the device to monitor cell temperature, and a thermo-electric cooler is used to ensure that this value is 25°C.

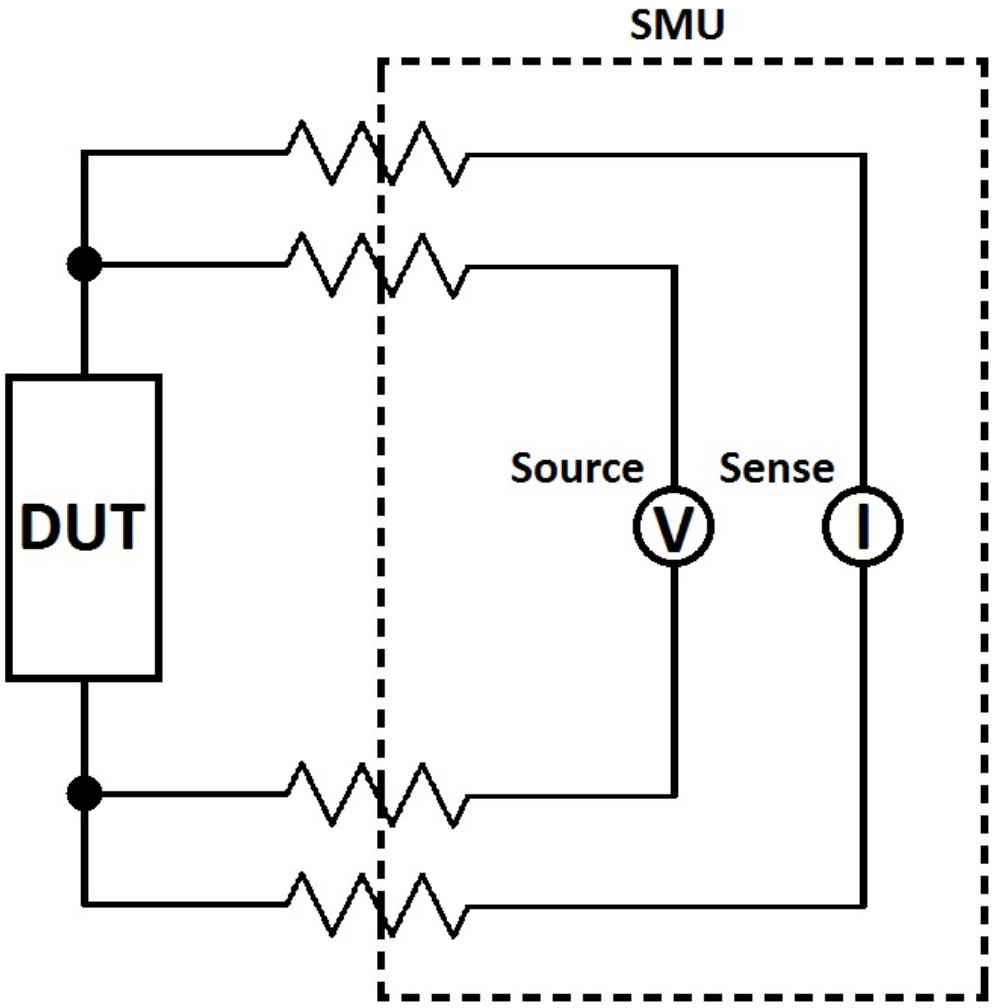

Figure 3.3 **Diagram of the four-point probe measurement on the device under test (DUT). Series resistance exists in the source measurement unit (SMU), the leads, and in the contact between the leads and the DUT. The SMU is responsible for applying voltage across the DUT, and then measuring the resulting current.**

After the lamp is ignited, a 15-minute warm period is observed to allow the intensity of the light to stabilize. The system is then calibrated using two silicon standards that have been characterized at NREL. The first standard is used to adjust the intensity of the lamp to match the J_{sc} of the silicon cell with that of its NREL-measured value. The second standard is used to verify the calibration. The device is then placed on the testing block and probed so that it is ready for a measurement. Once parameters, such as cell name and area, along with the structure description and testing comments, are entered by the cell tester, the cell measurement begins. A total of four JV measurements are taken from the DUT; two curves while the cell is illuminated, and two while the light is blocked by the shutter. The first curve in both sets has voltage swept across the cell from -0.6 V to 1.2 V. Likewise, the second curve in both sets has voltage swept across the cell from 1.2 V to -0.6 V. The incremental step of the voltage is 4.5 mV. The point of sweeping voltage in both directions on the solar cells is to see if there is any hysteresis in the measurements. Well-behaved IBC-SHJ solar cells show no hysteresis.

3.2.1 Diode Analysis

After measuring the IBC-SHJ solar cells in this manner, their JV curves can be analyzed to characterize the quality of the diode. A simple lumped circuit model can be used to approximate the JV result of any solar cell. This model consists of a shunt resistance, a series resistance, the diode, and a light-activated constant current supply that is in opposition to the diode, as shown in Figure 3.4.

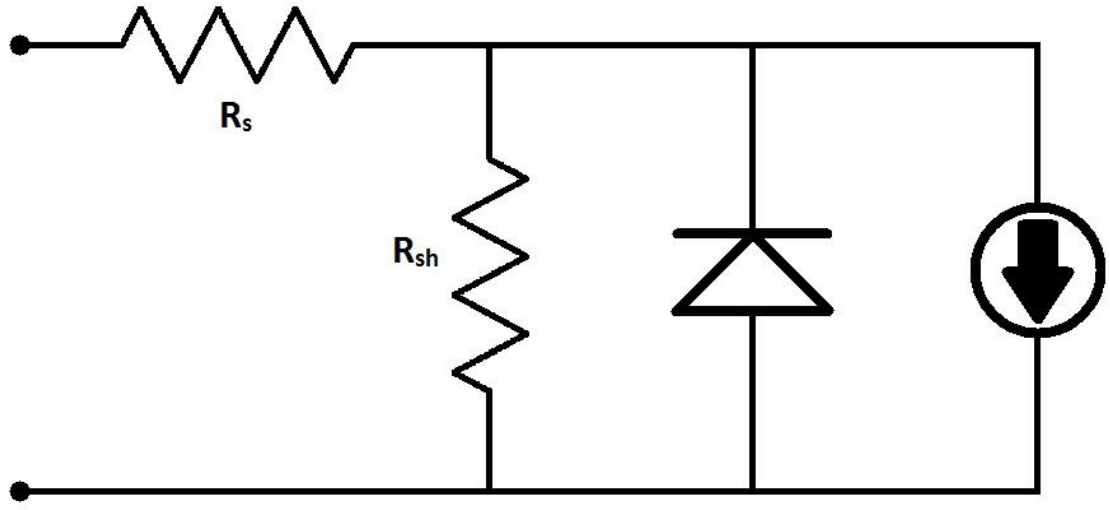

Figure 3.4 Lumped circuit model of a solar cell. Analysis can lead to characterization of the series resistance and diode parameters.

The equation that incorporates these circuit elements is:

$$J = J_0 * e^{\left(\frac{q*(V-R_S*J)}{A*k*T}\right)} + G * V - J_L \quad (3.1)$$

J_0 is the diode current, G is the shunt conductance obtained from the shunt resistance, A is the diode ideality factor, and J_L is the light-activated current [12]. The anticipated G term is to the right of the series resistance in Figure 3.4 because with this cell structure, the current will have flown through the junction and to the grids before a shunting issue can arise. Before analyzing the diode, the series and shunt resistance effects must be removed from the equation. For well-behaved solar cells that have flat JV curves for voltages less than 0 V, the G-term becomes much less than the other two terms, and can be ignored. However, for JV data that shows slight shunting, this G-term must be accounted for. The shunt conductance is calculated from plotting dJ/dV vs. voltage around 0 V, and taking the value at this voltage. Once this conductance is

obtained, the G*V term can be subtracted from equation 3.1 to allow for further analysis of the device.

Next, to remove the series resistance effect of the diode, some algebra must be invoked. To calculate the series resistance, the derivative of equation 3.1 (dV/dJ) must be taken, and from this comes equation 3.2:

$$\frac{dV}{dJ} = \frac{A*k*T}{q*(J+J_L)} + R_S \tag{3.2}$$

From this equation, a plot of dV/dJ vs. $1/(J+J_L)$ is created. An important note is that for light JV curve analysis, J_L (or for constant J_L, J_{sc}) is subtracted out of the equation for ease of analysis. By fitting a linear curve to the data points between 0 and 1 cm^2/mA, the diode ideality factor and series resistance can be obtained. The series resistance comes directly from the y-intercept of the curve fit, and the ideality factor is derived from dividing out the k*T/q term from the slope. This "A" factor, though unitless, has physical meaning while it is between 1 and 2.

With the G and R_S values calculated, the diode parameters can be solved for. By plotting the corrected values of J and V as $(J+J_{SC}-GV)$ vs. $(V-R_SJ)$ on a semi-logarithmic plot (y-axis) and using an exponential curve fit, the first quadrant of the JV curve is analyzed. Once the curve is fit over the same region used for the dV/dJ curve fitting, J_0 and the A-factor can be solved for. The constant term outside of the exponential is J_0, and the value of A comes from dividing out the q/(k*T) term inside the exponential. This A value should be very similar to that obtained from the dV/dJ curve fit.

Though all devices are analyzed this way, the goal of analyzing an IBC-SHJ solar cell through these calculations is to further match simulations to the results of experimental devices. However, as shown in Figure 3.5, this analysis is problematic.

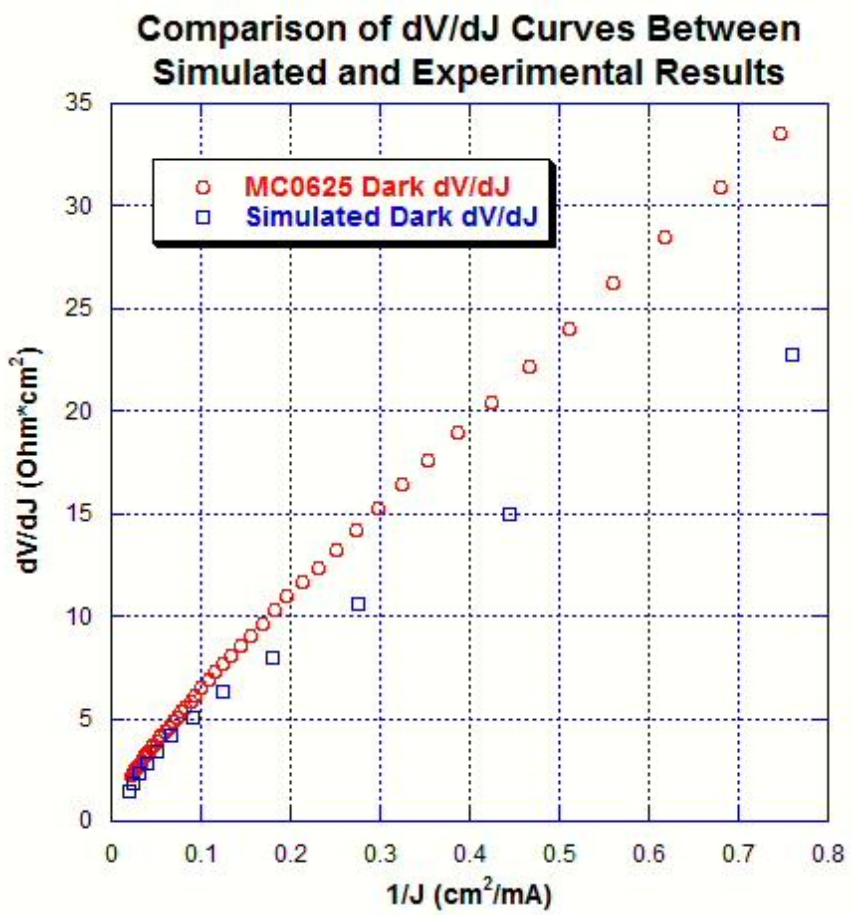

Figure 3.5 Comparison of simulated and experimental dark dV/dJ curves for IBC-SHJ solar cells. Simulated curves have a bend in the data, resulting in two fitting sections.

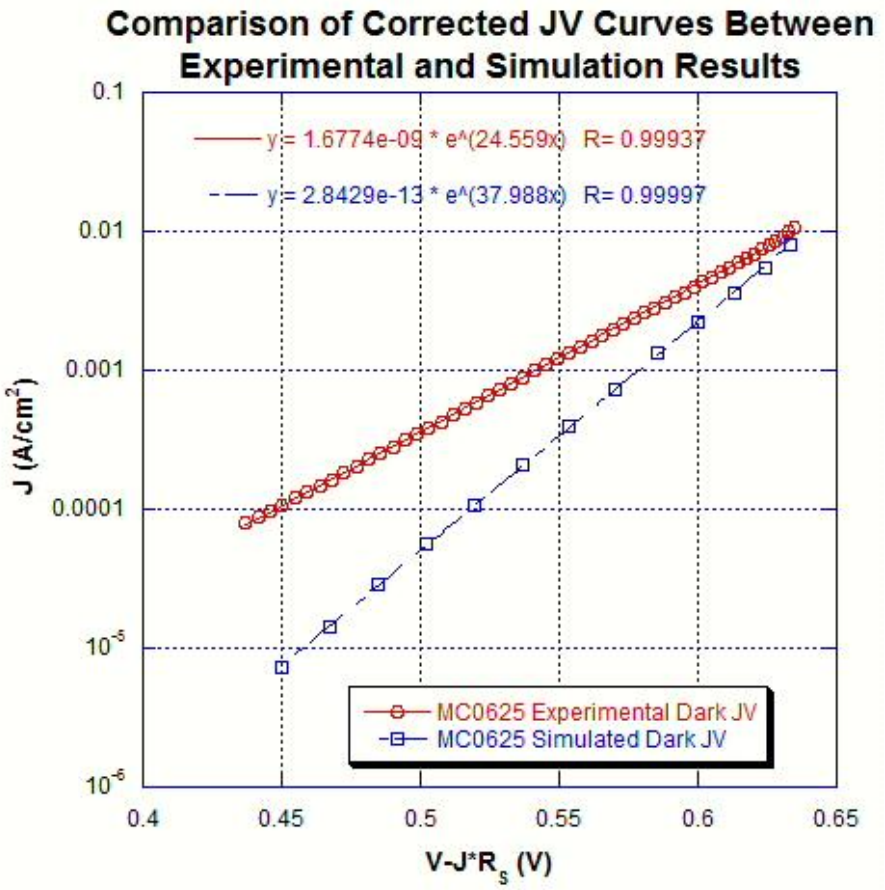

Figure 3.6 Comparison of simulated and experimental dark series-corrected JV curves for IBC-SHJ solar cells. J_0 is nearly four orders of magnitude lower in the simulated curve, and the A-factor is near 1, showing that a source of recombination is not present in the model.

The experimental results trend show that a linear fit is quite possible throughout the entire domain of Figure 3.5. However, this is not the case for the simulated data, as it presents a bend in the data near 0.1 cm^2/mA. This leads to two fitting regions on either side of this specified area. Fitting a straight line to the data on the higher end results in an A factor that is too low and a series resistance that is too high. Conversely, fitting the data towards the origin yields an A factor near that of the experimental data, but a series resistance that is half of what device results show. This

means that there is a source of recombination, affecting the series resistance, in the device that the model has yet to incorporate. Chapter 5 describes in depth how the model is still valid even without this source of recombination. Figure 3.6 better shows the difference between the experimental results and the model by comparing the series resistance-corrected JV curves. Thus, dV/dJ analysis is not a good tool to use as validation for the model. Nonetheless, the method is used to characterize device results to see if the trend of the series resistance decreases or increases in the same way the simulation predicts for different experiments.

Table 3.1 Results from dV/dJ and JV correction analysis. R_s has units of Ohm*cm^2 and J_0 has units of A/cm^2. There are two cells per piece, each with a different interdigitated geometry, and thus the -001 and -002.

	Measured dV/dJ and JV Correction Results						
		Light			Dark		
Piece	FF	Rs	A	Jo	Rs	A	Jo
MC0737-01-001	64.9	1.49	~ 2	1.7E-06	1.89	1.70	7.6E-09
MC0737-01-002	60.7	2.22	~ 2	4.3E-06	3.41	1.59	2.5E-09
MC0799-01-001	68.8	1.11	1.98	2.9E-07	1.01	1.90	4.8E-08
MC0799-01-002	63.4	1.31	~ 2	4.7E-06	1.42	~ 2	4.0E-07
MC0799-05-001	69.9	1.53	1.67	4.4E-08	1.55	1.56	3.7E-09
MC0799-05-002	68.2	1.56	1.77	1.1E-07	1.5	1.62	7.7E-09
MC0836-08-001	65.8	1.34	~ 2	1.0E-06	1.46	1.60	4.0E-09
MC0836-08-002	63.8	1.53	~ 2	1.8E-06	1.57	1.66	7.3E-09

There are several trends one can derive from Table 3.1. The FF of the first cell tends to be higher than that of the second, whereas the series resistances tend to be less in the first than in the second. This would lead researchers to believe that the 1200-500-25 um p-width/n-width/gap-width cell structure is superior, but the second cell

geometry of 1400-250-25 um yields higher currents, which makes both cells match in efficiency.

3.3 Quantum Efficiency and Spectral Response

Quantum efficiency (QE) is the measure of how well a solar cell can convert incoming photons into electrical current at a given wavelength, i.e. the ratio of electrons out to photons in. The QE ranges between 0 and 1; if the QE is 1 at some wavelength, then that means every photon incident on the solar cell was converted into current. Where JV measurements use the broad AM1.5 spectrum, QE measurements show the wavelength dependence of the photocurrent J_L [12]. Effects that lower QE in an IBC-SHJ are front surface reflection, absorption in the SiC layer, absorption in the SiN_x layer, absorption in the intrinsic a-Si layer, and poor generation and collection in the emitter/base regions. In contrast to standard Si solar cells, there is no grid shadowing or absorption loss in the diffused emitter.

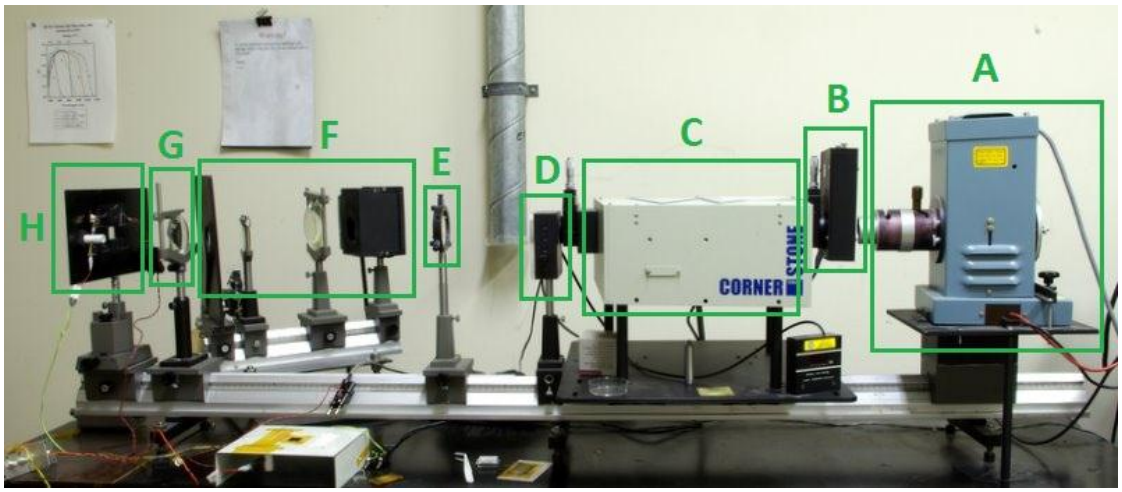

Figure 3.7 QE measurement setup diagram. The hardware consists of a 250W 24V halogen light source (A), a filter wheel (B), a monochromator (C), a variable frequency light chopper (D), a collimating lens (E), a bias light setup (F), a focusing lens (G), and the testing block (H).

Figure 3.7 shows the setup for QE measurements. A 250 W EHJ Halogen bulb is the light source for the system. The light shines through a filter wheel using long pass filters that remove higher-order wavelength modes of the lightwaves. Otherwise, the signal from the monochromator would include interfering modes at 2 or 3 times the specified wavelength. After passing through the filter wheel, the light passes into a monochromator that splits the light into separate wavelengths. The light is divided by a grating that reflects the light into a slit, which produces Gaussian light beams with a full width half maximum of roughly 10 nm [13]. The Gaussian beam goes through the variable frequency chopper which rotates at a speed of 72 to 78 Hz, which is manually set by the user. This turns the light beam into an AC signal. The beam continues into a collimating lens, and then passes through a focusing lens which contracts the beam to an area 2.5mm x 2.5mm. This area is smaller than the size of most solar cells tested

on the QE system, and so area-related effects are not usually a problem. However, because the beam width is just slightly larger than the pitch of the interdigitated fingers, the integrated quantum efficiency value, which should correlate with the J_{sc} value from JV testing, is usually lower. To fix this problem, the focusing lens' position is changed to defocus the beam, allowing more of the fingers to be position within the beam's area, and allowing the beam width to span several pairs of p and n fingers, thus better averaging the response.

The QE system also has the ability to bias the DUT, both with voltage and with light. A DC light source is sometimes used to flood the solar cell with either white or filtered light. Since only the photo-current that is in-sync with the variable frequency chopper is sensed, the device can be tested in either the dark or the light since the lock-in rejects any DC signal. A shutter is used to control the bias light's access to the solar cell. Voltages are also used to bias the devices to determine cell characteristics for each different applied voltage. Applying 0V bias across the cell results in an integrated quantum efficiency which is comparable to the J_{sc} condition measured from JV. A voltage bias of -1V yields what one would expect to be a maximum integrated quantum efficiency. The high reverse bias effectively eliminates recombination, giving the 'optically limited' photoresponse, and thus describes the maximum current output for a well-behaved device under one-sun illumination. A voltage bias around the maximum power voltage gives insight into how the device operates while it is producing its maximum power.

The system is initially calibrated when a new bulb is used for a light source. A pyroelectric radiometer is used to measure the incoming flux of photons at each wavelength in steps of 5 nm. This reference scan is completed twice; once for the

monochromator using only one grating, and again for when the monochromator uses both of its gratings. Once these two data curves are obtained, the silicon standards used to calibrate the simulator for JV measurements are used to measure what their respective integrated quantum efficiency is. A scaling factor is implemented and varied until the measurement yields an integrated quantum efficiency that correlates with the correct J_{sc} of the silicon standard. From then on, all measurements made using the new bulb are checked with the calibration sample each time the system is turned on.

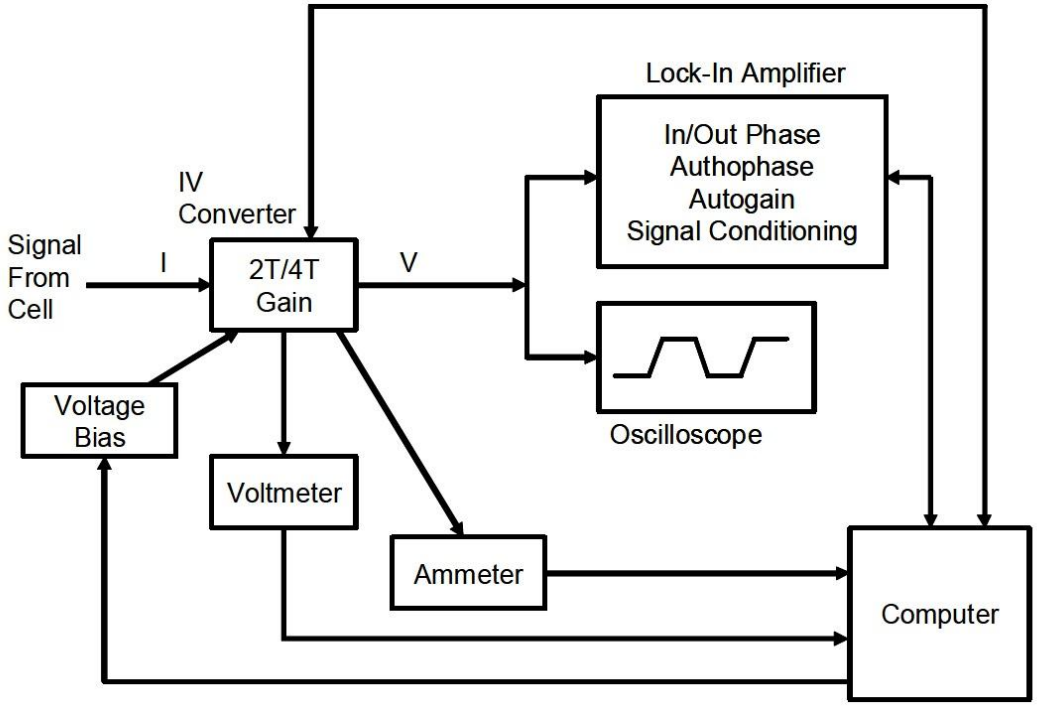

Figure 3.8 The electrical stage of the QE system [13]. The signal passes through a custom-built IV converter, and then into the oscilloscope and Lock-In Amplifier. The data is then read into the computer.

Figure 3.8 shows a high level diagram for the electrical stages involved in the QE measurement using the electrical current produced from the solar cell. Cell contact is made using the four-point probe technique, as was done for JV testing. The signal from the cell passes through a custom-built IV converter, and then into an oscilloscope and a Standford Research Labs SR830 DSP Lock-In Amplifier. The IV converter takes the electrical current as an input and produces a corresponding voltage as an output signal. It can handle a two terminal or four terminal measurement. The Lock-In Amplifier controls the in- and out-of-phase signals, and is synchronized using the variable frequency chopper, which is also connected to the Lock-In. Also, a wide range of data over several orders of magnitude can be measured due to the IV converter and Lock-In each having variable gain. The data is read into the computer, and the program calculates the QE values for each wavelength. QE measurement wavelength ranges typically start from 350 nm, and go slightly past the band edge of the absorber material. The band edge can be calculated as follows:

$$\lambda_{be} = \frac{h*c}{E_g} \sim \frac{1240\ (nm*eV)}{E_g\ (eV)} \tag{3.3}$$

For the IBC-SHJ solar cells, this band edge is around 1127 nm, and the QE measurement ends at 1200 nm. Figure 3.9 is an example of a QE measurement made on an IBC-SHJ device with a polished wafer.

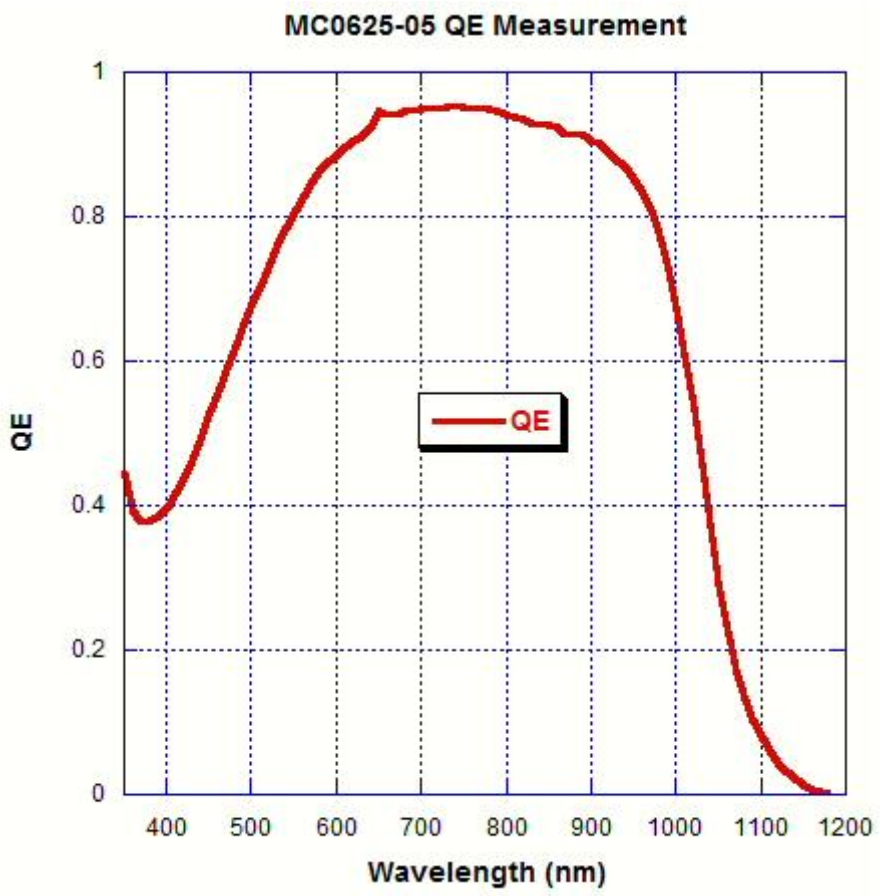

Figure 3.9 Measured QE curve on IBC-SHJ solar cell.

Chapter 4

SYNOPSYS SENTAURUS TCAD

Sentaurus is the TCAD software used for all of the simulations done in this research. This software contains several programs that allow users to simulate everything from material processing to device results. Some of these programs can be accessed directly via a Linux terminal, but the incorporation of Sentaurus Workbench allows users to combine the programs they wish to use into one screen, making programming and data simulation much simpler. The three programs used in this research were Structure Editor, Device, and Inspect [14].

4.1 Workbench

Sentaurus Workbench is the front panel of all software used in the simulations. The program acts as a spreadsheet that calls any other Sentaurus program that the user can access. The top of this spreadsheet has these programs defined, and all spreadsheet cells beneath each program are used for variables. The second row of the spreadsheet contains the names of these variables, which can be accessed in the code of programs. Each row below this is considered an "experiment," and the cells in these rows contain the values for their respective variables. Examples of variables for the Structure Editor are layer thickness, number of interdigitated fingers, and interdigitated finger width, and examples of variables for Device are intrinsic layer band gap, surface recombination velocity, and interface and bulk defect densities.

4.2 Structure Editor

Sentaurus Structure Editor allows the user to create 2D and 3D geometrical structures representative of the device they wish to model [15]. The user can create this structure either by using the graphical user interface (GUI) incorporated with the program, or by using TCL programming to simulate the structure. The GUI incorporates all functions that the user has access to in the programming code in simple drop-down menus. However, in performing experiments where geometry is the main experimental parameter, using the code is simpler means of operating the software.

4.2.1 Command File

There is a single command file to write the code to operate the structure editor. The geometrical structure, the materials used in the structure, the doping, and mesh are all created and chosen in this file.

4.2.1.1 Variable Definition

As with most other programming code, all of the variable definitions are made at the beginning of the file. All layer thicknesses and widths are established, as well as the doping in the silicon layers. The values from the Workbench are called using "@Variable_Name@" and are stored in their respective variable.

4.2.1.2 Geometrical Structure

The c-Si wafer, intrinsic layers, the nitride, and the carbide layers are created separately from the interdigitated doped amorphous layers and contacts. They are

created by the create-rectangle function, where the dimensions of the layers specified. In the same line of code, the material that the layer will consist of is chosen, and the layer is named. Though the IBC-SHJ structure studied is created in 2D, the program assumes a third dimension thickness of 1 um. An example line of code would read as:

(sdegeo:create-rectangle (position 0 0 0) (position BulkWidth BulkThickness 0) "Silicon" "cSiBulk")

In this example, BulkWidth and BulkThickness are the variables for the total width and thickness of the c-Si wafer, "Silicon" is the material name loaded from the material database in the software for the wafer, and "cSiBulk" is the variable name of this layer to be called in all future code. This specific code creates the wafer layer.

4.2.1.3 Layer Doping

The doping level of the wafers is specified using the define-constant-profile function, including the doping in the wafer, the intrinsic layers, and the doped amorphous layers. First, a profile is created containing the concentration of the dopant and the dopant type. Then, this profile is placed into the layer that it matches with. The same profile can be placed into multiple layers, as was done for the front- and rear-side intrinsic layers.

4.2.1.4 Contact Definition and Gap Passivation

Much like the processing steps for experimental IBC-SHJ solar cells, the p-type and n-type strips are created separately from one another. First, the p-type strips are placed, the aluminum contacts are created on top of the strips, and then the aluminum is defined as a contact. The refinement mesh, which will be discussed later

in the chapter, for the p-strips is also created here, along with the doping. Next, the same is done for the n-strips. Once both p- and n-strips are placed, the gaps are passivated by inserting Si_3N_4 between the fingers.

4.2.1.5 Refinement and Meshing

Sentaurus solves the equations it is instructed to calculate by looking at finite-sized sections, or "Yee Cells." Dividing the entire device into these tiny cells is called meshing, and is important to calculating solutions that one wishes to observe. The mesh can be broad for thick layers, such as the c-Si wafer. However, for the thin amorphous layers, and especially the interfaces between the layers, the mesh must be refined to much smaller Yee Cells. This is because most of the physics is happening at these interfaces. The user does not have too much control over the exact size of the mesh. Rather, they can establish maximum and minimum bounds for the dimensions of the mesh, and the program automatically chooses what it sees as the optimum refinement. The Yee Cells created are in the shape of triangles for almost all simulations in Sentaurus. The anti-reflection layers, along with the rear passivating intrinsic layer, are easy enough to refine. However, the interdigitated p- and n-strips and the Si_3N_4 gap passivating layers are more difficult, and require more code. They are refined using the same loop structure as was used to create them. Once the meshing is complete, the Structure Editor creates and saves three files: a boundary file, a command file, and a mesh file. Both the boundary and mesh files are accessed by Sentaurus Device, and are used for setting up the calculations to acquire device results for the simulations.

4.3 Device

Sentaurus Device uses both a command file and a parameter file to perform its responsibilities. This section is what calculates all device physics. Physical models, bulk layer defects, interface defects, illumination, and other layer parameters are specified in these two files [16].

4.3.1 Command File

The command file in Sentaurus Device is where some physics are set up, and the simulation parameters are defined. This file is the most accessed out of the program, as most experiments revolve around the variables that can be observed in these sections.

4.3.1.1 Physics Model

The section begins by creating the five files it will output data to, then immediately specifies the physical characteristics of the device to solve for. Examples of such are the electron and hole densities and lifetime throughout the solar cell, the electric field vectors, and the current. A complete list of parameters to solve for can be found in the manuals. The aluminum contacts are also specified as electrodes, and a bias can be applied directly to them if need be. The default is to have zero voltage across both of the contacts.

4.3.1.2 Doped and Amorphous Bulk Traps

Once a layer has been chosen, the recombination is specified as SRH doping dependence. Both of the intrinsic and both of the doped amorphous layers have traps

and defects in their bulk that are carefully modeled using exponential band tail and midgap Gaussian defect states. For both of these types of defects, the concentration and capture cross section are specified. The peak concentration of the band tail states and the width of the Gaussian midgap states are held constant for all simulations. Conversely, the characteristic energy of the band tail states and the peak concentration of the Gaussian midgap states are varied for model validation and simulation results. The formulas for both of these types of defect densities (band tail and then Gaussian midgap) are

$$N_0 * e^{-\left|\frac{E-E_0}{E_S}\right|} \quad (4.1.a)$$

$$N_0 * e^{-\frac{(E-E_0)^2}{2*E_S{}^2}} \quad (4.1.b)$$

Where N_0 is the initial peak concentration of defects, E_0 is the energy position of the peak concentration, and E_s is the characteristic energy for band tail or the width of the Gaussian midgap defect densities. The main effect of these parameters on JV performance is from Fill Factor.

Table 4.1 **Values used in the modeling of traps and defects in the intrinsic and doped amorphous silicon layers.**

Defect Type		(i)a-Si	(p)a-Si	(n)a-Si
Valence Tail States	$N^{v\text{-}tail}{}_D$ ($cm^{-3}ev^{-1}$)	10^{18}	10^{21}	10^{21}
	$E^{v\text{-}tail}{}_D$ eV	0.06	0.12	0.12
Conduction Tail States	$N^{c\text{-}tail}{}_A$ ($cm^{-3}ev^{-1}$)	10^{18}	10^{21}	10^{21}
	$E^{c\text{-}tail}{}_A$ (eV)	0.04	0.07	0.07
Acceptor-like dangling bond states	$N^{db}{}_A$ ($cm^{-3}ev^{-1}$)	10^{15}	$1.5*10^{19}$	$1.5*10^{19}$
	$E^{db}{}_A$ (eV)	1.10	1.30	0.70
	$\sigma^{db}{}_A$ (eV)	0.15	0.20	0.20
Donor-like dangling bond states	$N^{db}{}_D$ ($cm^{-3}ev^{-1}$)	10^{15}	$1.5*10^{19}$	$1.5*10^{19}$
	$E^{db}{}_D$ (eV)	0.90	1.10	0.45
	$\sigma^{db}{}_D$ (eV)	0.15	0.20	0.20

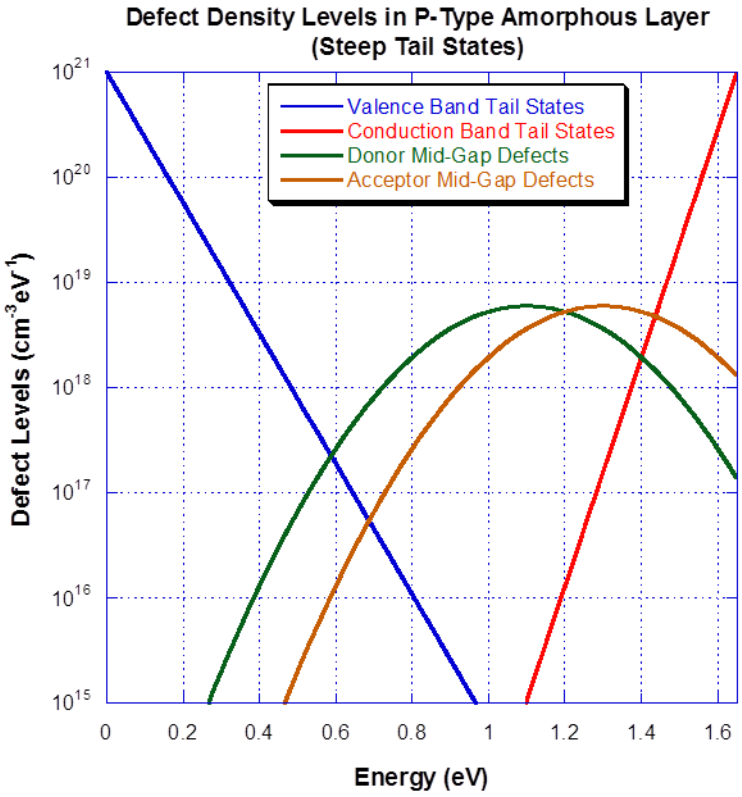

Figure 4.1 **Distribution of defects for the p-type amorphous silicon strips.**

The values shown in Table 4.1 were taken from two sources. The data for the intrinsic layers was taken from Meijun Lu's graduate thesis [17], and the doped amorphous layer values were taken from transmission line simulations. A series of variable-spaced metal contacts were evaporated through a mask on a layer of doped amorphous silicon. A voltage was applied to the contacts, and the current was measured as the contact separation was changed. By varying the traps and defect densities, we attempted to match the conductivity and activation energy that we have found experimentally on our layers. The capture cross sections of electrons and holes in the intrinsic layers range in order of magnitude from 2E-15 cm^2 to 7E-17 cm^2. For the doped amorphous layers, the range of cross sections is 1E-14 cm^2 to 1E-16 cm^2. The values of the capture cross sections are mostly taken from literature.

4.3.1.3 Optical Generation

If the user wishes to simulate light JV curves or reflection and quantum efficiency curves, then an illumination spectrum must be programmed into Sentaurus Device. For JV curves, the layers that will be affected by the optics need to be specified. Using the OpticalGeneration function, the direction and polarization of the light must first be specified. Next, the solar spectrum must be incorporated, either by loading in a text file with the wavelengths and flux intensities, or by directly typing in the wavelength array and intensity array. For the IBC-SHJ, this includes the SiC, the Si_3N_4, the top intrinsic layer, and the c-Si wafer. Both lateral and vertical dimensions must be specified in the code, followed by material type. If the user wishes to simulate reflection and quantum efficiency, the OpticalGeneration function becomes much more condensed. The model assumes a quantum yield of 1, meaning there is

one carrier per photon. The optics are described in the code using the transfer matrix method (TMM), where the excitation is defined by the angle of illumination, the starting wavelength of the light, and the intensity of the light, which is 1000 W/m^2. The width of this monochromatic beam is coded to shine on the entire device, which is different from the size of the beam in experimental QE scans. At the end of the command file, the wavelength is incremented from the starting wavelength.

4.3.1.4 Interface Defects and Recombination

Since the IBC-SHJ device incorporates intrinsic layers on both sides of the c-Si wafer, the most important interface to evaluate is between these layers. The interface defect levels are modeled similar to that of the bulk layer defects. However, though there are two band tail states, there is only one midgap level density of states. This gives the total defect distribution a U-shape, which matches well with literature. Though the order of magnitude of these defects are about eight orders of magnitude lower than that of the bulk defect densities, their effect on V_{oc} is much greater. In attempting to model experimental IBC-SHJ devices, D_{it} was altered to achieve a well-matched V_{oc}. Both front and back a-Si:H/c-Si interfaces were modeled using the same exact paramters. The Si_3N_4 layer was given a fixed positive charge density, which is specified in the Workbench. The standard value for the simulations was 5E16 cm^{-3}. The SiC layer is characterized in the code as the beginning of the OpticalGeneration function, and has no fixed charge.

4.3.1.5 Solving

The solutions to the simulations come from solving the Poisson equation, coupled with the electron and hole continuity equations. Several general solution boundaries are called, some of which are the maximum allowable error, the maximum number of allowed iterations per step, and the digits of precision, after which the type of solution is selected. As stated before, this was illuminated JV curves, dark JV curves, or reflection and quantum efficiency curves. For reflection and quantum efficiency, the wavelengths are scanned from start to end based on what the user specifies on the Workbench. Also, the maximum and minimum step size between wavelengths is taken from user input in the code in the event the solution does not cleanly converge at the initial wavelength step size. For illuminated JV curves, the voltage across the contacts is scanned from 0V to 0.8V. The solution is broken into two sections. The first section allows for broad voltage ranges up to 0.45V due to the current density showing almost no change in value in this voltage range. The second section refines the range so gather a more accurate FF and V_{oc}. The dark JV curves are calculated in the same manner; the only difference is that there is no optical generation.

4.3.2 Parameter File

Sentaurus Device is the only tool on the Workbench that uses a parameter file in addition to a command file. All other physical parameters of the IBC-SHJ device layers are described in the parameter file that weren't included in the command file. Sentaurus has included all important physical data for each of its layers in the material

list, and the user can access these files and change the default values as they see fit, or simply only change a few values using code in the parameter file.

4.3.2.1 Physical Layer Parameters

As stated above, the physical data of the layers can be accessed via the files stored by Sentaurus, or by using code to change specific values. The general files for the doped amorphous silicon were accessed through the use of **Region = "pStrip.#" { Insert = "PStrip.par" }** or **Region = "nStrip.#" { Insert = "NStrip.par" }** where # is the chosen number of the strip you are uploading the data for. Some examples of parameters that can be changed in these files are band gap, electron affinity, electron and hole effective mass, mobility, trap level for SRH recombination, and the n and k values. The only values altered in the amorphous doped layer files were the n and k values for optics, the mobility of electrons and holes, and the band gaps; all other default values were unchanged. The same insertion for the silicon nitride and carbide layers was made for their respective optimized n and k values (R=2 for Si_3N_4 and R=5 for SiC). R is the ratio of Ammonia/Silane for the Nitride and Methane/Silane for the Carbide.

4.3.2.2 Interface Recombination

The interfaces between the top and rear intrinsic layer with the c-Si wafer have surface recombination velocities that are programmed as variables, as several simulations were run to see the effect of changing this value. However, the interface between the doped amorphous layers and the intrinsic rear layer had a fixed surface recombination velocity. Both types of interfaces have transport mechanisms that were

modeled as thermionic. The parameter files for the intrinsic layers are incorporated into the code because the band gap of these two layers is considered a variable in the simulations.

4.4 Inspect

Sentaurus Inspect is a graphics and data extraction tool. All data calculated from Device can be loaded and manipulated to view using this program [18]. The program also interacts with the Workbench by creating extra columns that display the four main JV parameters once a set of simulations finish.

4.4.1 Command file

As with the Structure Editor, there is only a single command file used in Inspect. Most of the code revolves around creating equations to analyze the data, and then turning this data into graphs. The file begins with defining Planck's Constant, the speed of light, and the charge of an electron. Then, with the exception of setting the color scheme for the curves, the command file goes directly into analyzing the data.

4.4.1.1 JV Parameter Calculation

The first set of data extracted from the solution files of Device is the current vs. voltage. I_{sc}, V_{oc}, FF, and efficiency are then calculated by vector manipulation in the code, and then displayed on the Workbench once the simulation finishes. The line structure of the curves for the plots is defined, and the JV and power curves are displayed. Once this code is finished, a file is created containing the JV data.

4.4.1.2 Optics and Quantum Efficiency Calculation

If reflection and quantum efficiency was the chosen simulation type, more in-depth equations are needed to extract the data from Device. First, array functions are used to extract the reflection, transmission, absorption, wavelength, and total current values from the generated data. Next, J_{photon}, external quantum efficiency, and internal quantum efficiency are calculated. At the end of this code, a file is created that saves the EQE, IQE, transmission, and reflection all together.

Chapter 5

RESULTS

The first goal of two-dimensional simulations is to determine how closely the simulated data matches experimental results. This was most easily done by comparing generated current-voltage and quantum efficiency data with physically measured data. Once the computer model is validated by closely simulating measured characteristics and data, experimental simulations can be carried out with confidence by changing variables in the program.

5.1 Comparison of Experimental and Simulated Results

Once the general model was created, parameters such as D_{it} at the c-Si/a-Si interface and doped layer defect levels were varied to match the I_{sc}, V_{oc}, FF, and efficiency of actual devices. To first order, the dependence of device results on model parameters can be summarized as follows. Decreasing or increasing D_{it} inversely increases or decreases the resulting V_{oc} of simulated devices. The FF of the solar cells is matched by changing the level of the midgap defects in the doped amorphous layers. The I_{sc} largely depends on the front surface/front multilayer optics and hence was an easier parameter to model since the relevant materials' properties can be directly measured. Correct efficiencies follow once the other three parameters are fit. Several devices were matched to their respective simulations to add confidence in the model. Figure 5.1 shows such a comparison for one of our devices.

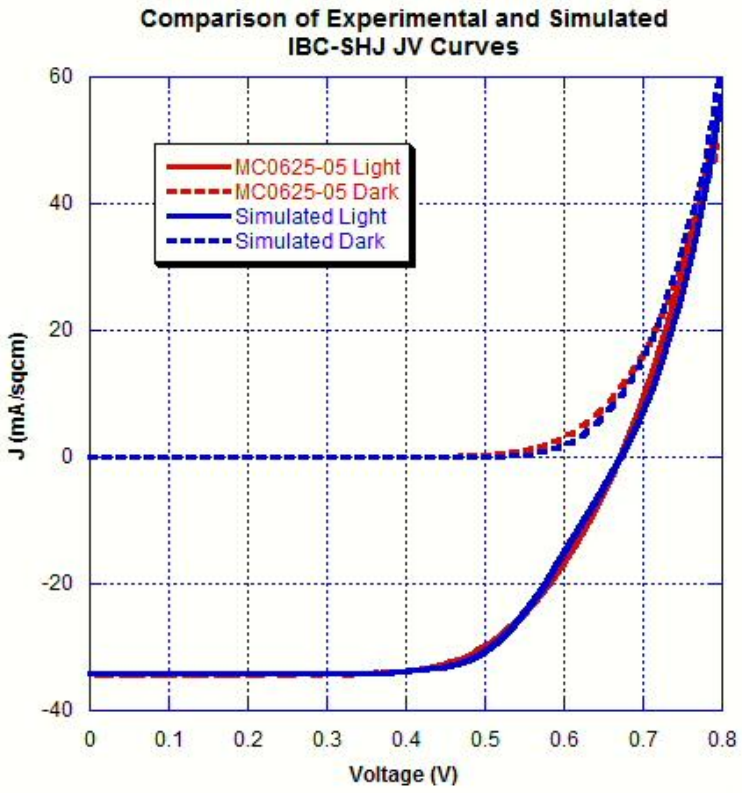

Figure 5.1 Simulated and measured light and dark JV curves for an IBC-SHJ solar cell showing good agreement.

As was discussed in Chapter 3, the simulation model is missing a source of recombination affecting the series resistance that is present in experimental devices, but this does not invalidate the model, as the third quadrant of the JV curve is the main focus in this research. The physical parameters used to describe the doped and intrinsic amorphous silicon layers agree well with several published results [19]-[25]. A coefficient of determination, or 'R^2', fit was used to see how well the modeled JV curves numerically match with experimental results. Equation 5.1 shows how the R^2 value is calculated.

$$R^2 = 1 - \frac{SS_{err}}{SS_{tot}} = 1 - \frac{\sum_i (y_i - f_i)^2}{\sum_i (y_i - \bar{y})^2} = 1 - \frac{Sum\ of\ squares\ of\ residuals}{Total\ sum\ of\ squares} \qquad (5.1)$$

This type of fit measures the variance of the simulation data from the measured data. An R^2 value can be between 0 and 1, and values greater than 0.99 means that the simulations are an excellent fit to experiments. Table 5.1 shows the results of performing this analysis on three different IBC-SHJ cells. The JV curves were analyzed in two sections: the entire curve and again in only the power quadrant. The near-perfect power-quadrant fits show that the missing recombination source affects only the first quadrant.

Table 5.1 R^2 values for three different IBC-SHJ solar cells. The three cells were chosen based on their different cell structures.

R-squared Values for IBC-SHJ Solar Cells		
	R-squared	R-squared (Power Quadrant)
MC0625	0.9968	0.9982
MC0737	0.9793	0.9995
MC0799	0.9587	0.9996

5.2 Doped Layer Defect Levels

Figure 5.2 shows the effect of increasing the midgap defects in the doped layers for an IBC-SHJ solar cell [26]. The FF can increase from 63% to 75% with a decrease of two orders of magnitude in mid-gap defect levels in the doped p- and n-type layers. Note that a factor of three decrease in doped layer defects from $2*10^{19}$ to $6*10^{18}$ $cm^{-3}eV^{-1}$ eliminates the S-shaped curve. This raises the point that S-shaped curves in our devices may be caused by having a large density of defects in our doped layers. Since our doped layers are currently deposited at a temperature around 175°C,

we can achieve lower densities of defects if we were to deposit these layers at higher temperatures (200°C-250°C). These higher temperature depositions in SHJ solar cells have shown improved contacts between the Indium Tin Oxide (ITO) and a-Si:H layers. N-layers deposited at 200 °C or below have non-ohmic blocking contacts with ITO while those deposited at 250 °C have low resistance ohmic contacts [27]. The restriction on doing so at this time is the temperature limitation the present photolithography mask exhibits.

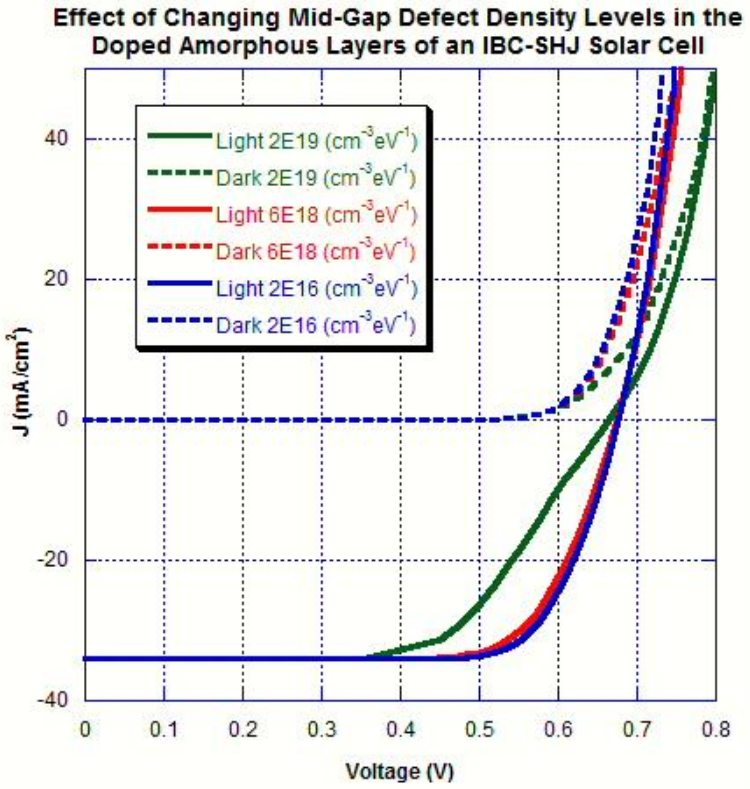

Figure 5.2 Effect of a-Si doped layer defect densities on light and dark JV curves. FF increased from 63 ("S-shaped curve") to 73 to 75% as defects decreased as shown. (All band tail energies 0.12/0.07 eV).

Modeling a generic IBC-SHJ solar cell, we have analyzed the dependence of FF on the defects in the p-type and n-type a-Si layers separately as shown in Figure

5.3 for two pairs of doped layer valence/conduction band tail energies: either 0.12/0.07 eV or 0.07/0.04 eV, respectively. By holding the p-layer mid-gap defect density constant at a low value of $L=2*10^{16}$ $cm^{-3}eV^{-1}$ and varying the n-layer mid-gap defect density between this value and $2*10^{19}$ $cm^{-3}eV^{-1}$, we see almost no effect on the FF of an IBC-SHJ device. In contrast, holding the n-layer mid-gap defect density constant at a high value of $H=2*10^{19}$ $cm^{-3}eV^{-1}$ and varying the p-layer mid-gap defect density, the FF decreases rapidly beyond 10^{18} $cm^{-3}eV^{-1}$ partially due to forming an S-shaped curve. The FF is limited to about 75% for defect densities lower than 10^{17} $cm^{-3}eV^{-1}$ by the band tail energies of 0.12/0.07 eV. Thus, the FF of our devices depends mainly on the defect levels in the p-layers, and as such, the S-shaped curve arises from having high defect densities in this layer. A FF of 70% is still achievable with defect densities of 10^{19} $cm^{-3}eV^{-1}$, but the device performance degrades rapidly past this point. When the doped layer band tail energies are reduced from 0.12/0.07 eV to 0.07/0.04 eV, the FF increases from 75% to ~ 80% and the dependence on midgap defects decreases. There is no S-curvature for band tail energy of 0.07/0.04 eV even at high p-layer midgap defects. Since band tail states are responsible for shallow trapping while midgap states are responsible for recombination, we infer that that S-shaped curves are due to trapped charge rather than recombination in the doped layer. The dark JV curves are also sensitive to the defects in the p-layer indicating a limit to minority carrier injection not collection.

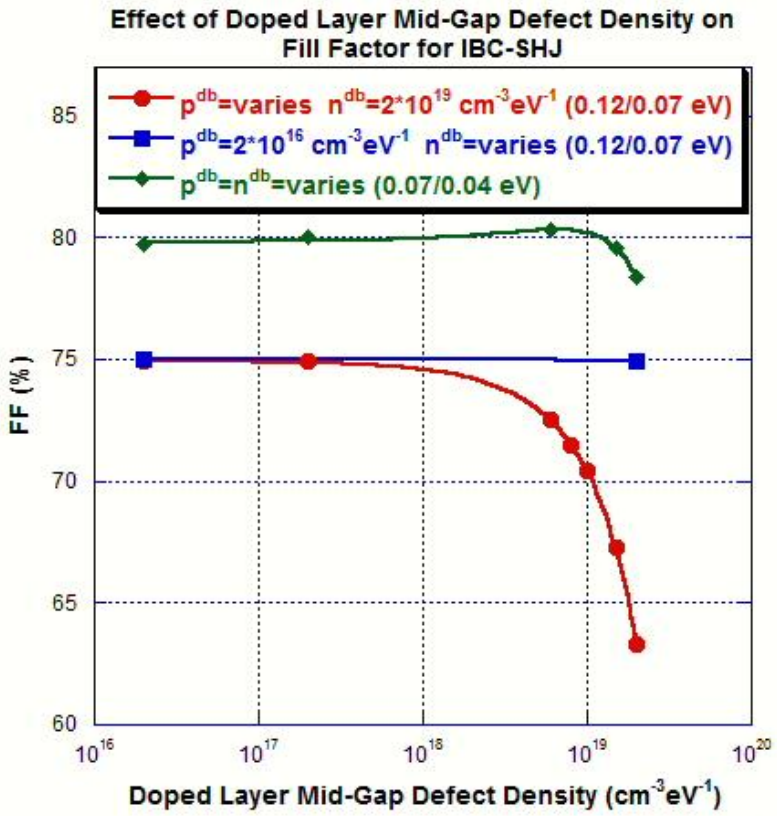

Figure 5.3 Relationship of Fill Factor to defect density in the doped a-Si layers. The band tail energies for the valence/conduction tail states were 0.120/0.07 eV for the red and blue curves, and 0.07/0.04 eV for the green curve. The 'db' stands for dangling bond.

Table 5.2 shows the V_{oc}, J_{sc}, FF and efficiency for high and low values of defect densities in the p and n doped layers and i-layers. Neither V_{oc} nor J_{sc} are very sensitive to the doped layer or i-layer defects. It is surprising that the mid-gap defects in the i-layer (H*) have a negligible effect on the performance of the device. Increasing their value by two orders of magnitude reduced the efficiency from 14.3 to 14.2%. There are several possible explanations for this: the i-layer defect densities were much lower than in the doped layers; the high electric field ensures negligible

recombination; and/or the fact that surface recombination is fixed at 10 cm/s, hence independent of the i-layer defects.

Table 5.2 Effect of mid-gap dangling bond defect levels for a-Si doped layers on JV parameters for low (L=2x10^{16} cm^{-3}eV^{-1}) and high (H=2x10^{19} cm^{-3}eV^{-1}) levels of mid gap defects in the p or n a-Si layers. H* refers to increase in two orders of magnitude in the i-layer mid-gap defect densities with H doped layer defects.

Tail State Energies	p^{db} Density	n^{db} Density	V_{oc} (mV)	J_{sc} (mA/cm^2)	FF (%)	Eff. (%)
0.12/0.07 (eV)	L	L	675	34.1	75.0	17.3
	L	H	674	34.0	74.9	17.2
	H	L	666	34.1	63.4	14.4
	H	H	665	34.0	63.3	14.3
	H*	H*	665	34.0	63.0	14.2
0.07/0.04 (eV)	L	L	675	33.9	79.7	18.2
	H	H	676	34.1	78.4	18.1

5.3 Rear i-Layer Band Gap

As stated previously, the rear i-layer must allow current to flow freely. The effectiveness of this ability can be changed based on the value of the band gap. Experimentally, there are three ways that the band gap can be changed: by changing the deposition temperature of the i-layer, by changing the H_2/SiH_4 ratio in the layer, and by changing the power of the RF plasma. The first two methods have a greater effect on band gap than the third. To lower the band gap of the i-layer, one can

increase the deposition temperature, increase the H_2/SiH_4 ratio, or reduce the power of the plasma. The motivation behind decreasing the band gap of the rear i-layer is to increase the FF [28]. Also, because thicker i-layers yield solar cells with higher V_{oc}'s but lower FF, we attempted to find a relation between the two that wouldn't hinder our results dramatically [26].

Three sets of experiments were run to determine the effect of changing the rear i-layer band gap on FF. While no change was made on the front i-layer, the rear i-layer was modeled with a thickness of 5nm, 8nm and 10nm, along with allowing the band gap to vary for each thickness. Figure 5.4 shows the JV results for an 8nm-thick rear i-layer with band gaps ranging from 1.76 eV to 1.66 eV. The response of V_{oc} and I_{sc} is minimal, but the FF changes from 35% for Eg = 1.76 eV to 78% for Eg = 1.66 eV. One can also see that the S-shaped curve starts to appear for band gaps higher than 1.72 eV. This is worth noting since the band gap of the devices made in our lab is typically around 1.72 eV, hence the experimentally observed S-shaped curves could result from slightly higher band gaps than anticipated.

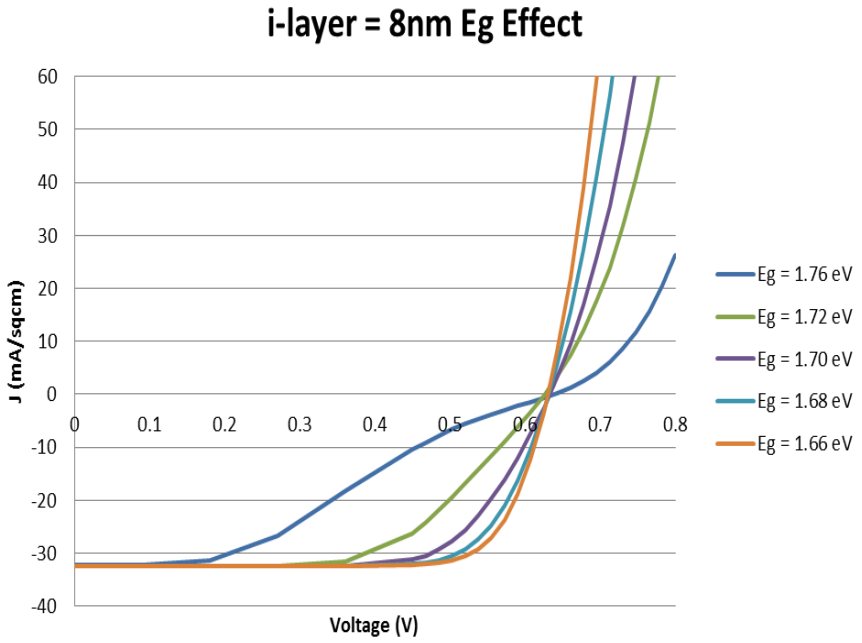

Figure 5.4 Effect of changing the rear i-layer band gap on JV curves.

From simulations, one can display the effects of changing the i-layer band gap in band diagrams. When the band gap is decreased, the offset in the valence band decreases. Thus, the S-shaped curve arising from larger band gaps is thought to be due to collection of the minority carriers (holes) at this offset. Figure 5.5 is a set of simulated band diagrams showing this change in the valence band [29].

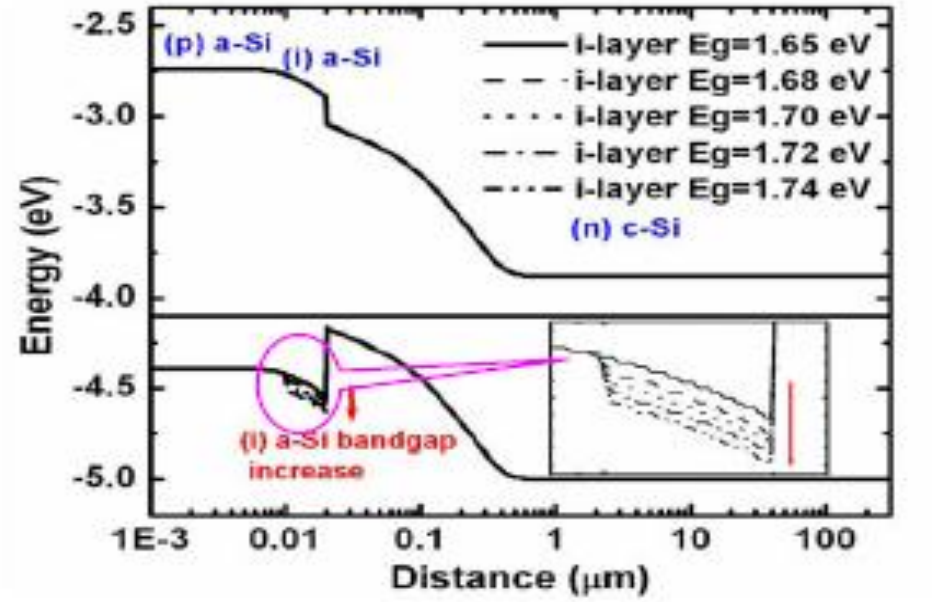

Figure 5.5 Band diagram of p-i-n structure with increasing band gap [29].

The data from the three sets of simulations is shown in Figure 5.6. The highest FF achievable with the modeled cell is around 72%. As the band gap decreases, the differences between the three thicknesses decreases, until the spread of FF at E_g = 1.66 eV is less than 2%. This relationship is beneficial, as it allows the rear i-layer to be deposited thicker, allowing for higher V_{oc}'s while keeping the FF high.

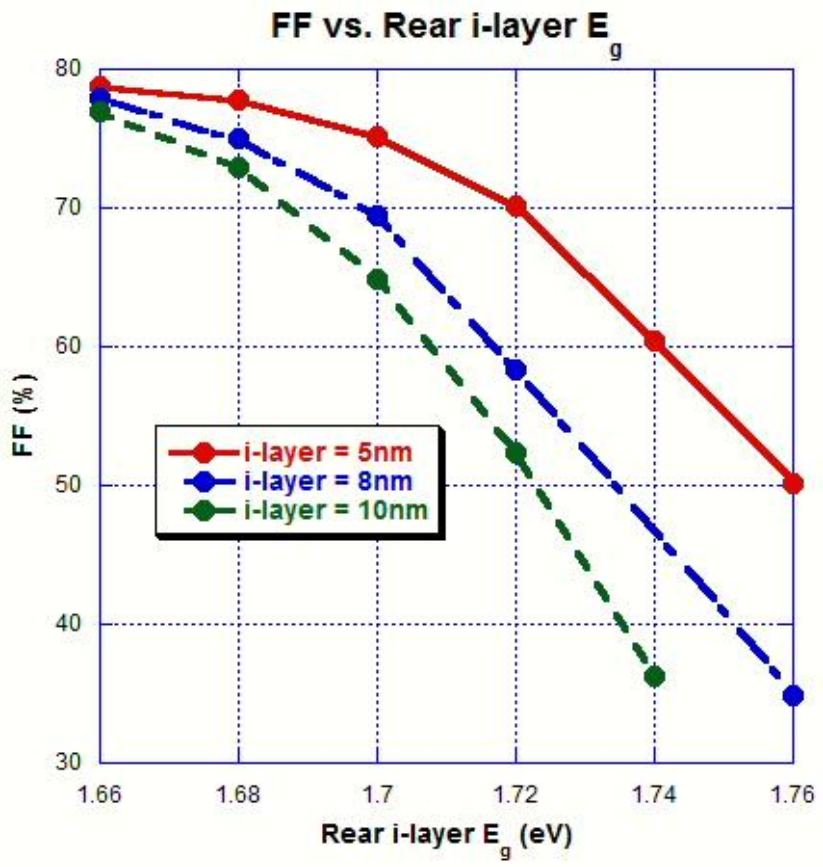

Figure 5.6 Effect on FF from changing rear i-layer band gap. The data is for three thicknesses of i-layer: 5nm, 8nm, and 10nm.

5.4 Geometry Simulations

The standard p-, n-, and gap-widths were varied to determine whether the dimensions used in the IBC-SHJ solar cell were optimal. Also, the number of interdigitated fingers was changed to see how the performance of the devices would alter.

5.4.1 Number of Fingers

Several simulations that modeled an increasing number of fingers were performed. The baseline widths (1400, 250, 25 um for the p-strip, n-strip, and gap) were used for the fingers, and only the number of fingers and total device width was changed. The range of strips was from two p-strips/one n-strip to six p-strips/five n-strips. Figure 5.7 shows the effect of using a different number of fingers. The general trend is that device performance suffers with the fewer strips there are. No S-shaped curve appears, but the FF of the solar cells decreases (71.2% to 67.3%) with the subtraction of fingers. Short-circuit current does not seem to change substantially (33.5 mA/cm2 to 33.0 mA/cm2), and the open-circuit voltage decreases slightly (640 mV to 629 mV) with the decrease in number of fingers. From the figure, one can see that there is very little change between having a 4p/3n and 6p/5n contact cell. From this, we can see that the standard number of fingers used is sufficient for our devices.

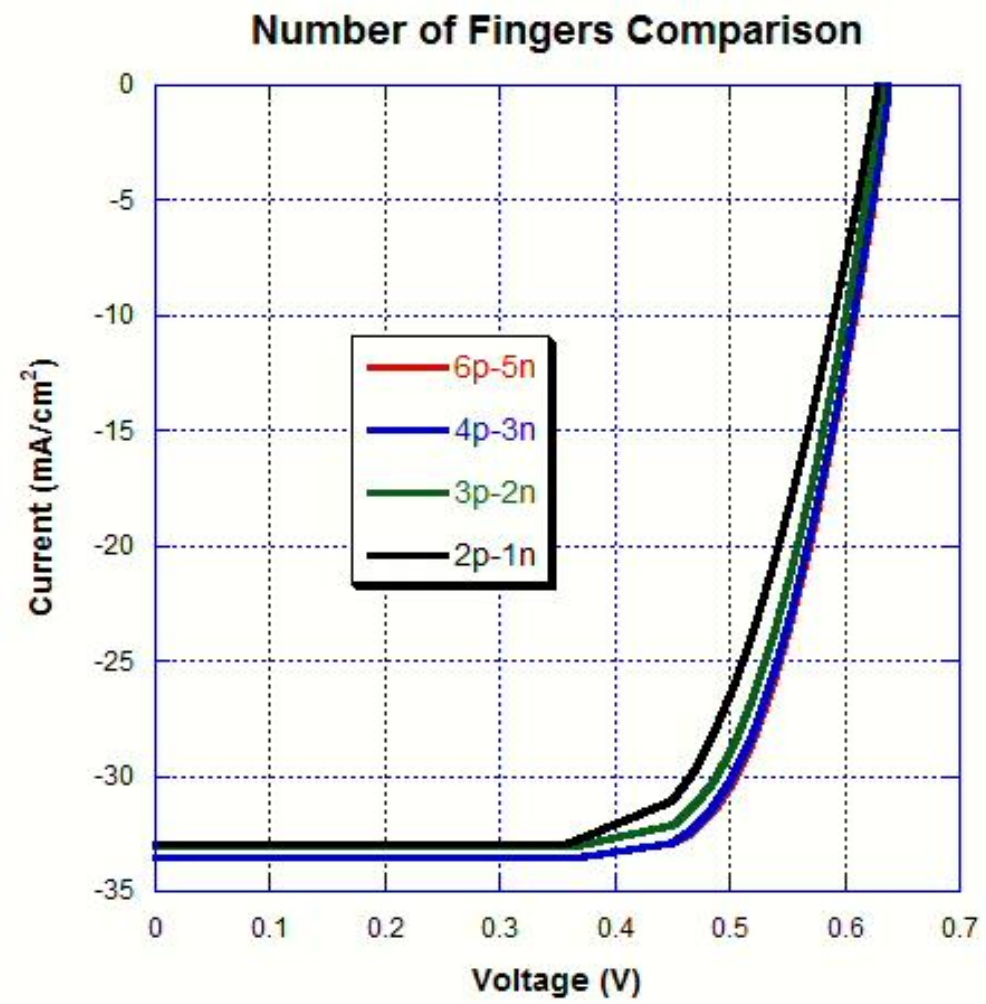

Figure 5.7 JV curves of increasing number of interdigitated strips on the rear surface of the IBC-SHJ solar cell.

5.4.2 Doped Layer Width Geometry

Three groups of simulations were performed to show how changing the individual finger widths would affect the basic JV parameters. First, the p-strip width was held constant at 1400 um while the n-strip width was varied from 50 um to 450 um. Next, the n-strip width was held constant at 250 um while the p-strip width was varied from 1000 um to 1600 um. The final group of experiments varied both p- and

n-strip widths, but keeping the ratio between the two the same. In decreasing the n-strip width, the device saw improved performance. While V_{oc} remained relatively constant, FF saw minor improvement, and I_{sc} increased more than 1 mA/cm^2 when the n-strip width was lowered to 50 μm. Conversely, when the p-strip width was allowed to vary, the device results showed little change throughout the entire range of widths.

The results from the third group of experiments best show the effect of changing the widths of the p- and n-strips. The combination of widths for these fingers is as follows (p(μm)-n(μm)): 560-100, 840-150, 1120-200, 1400-250, 1680-300. Table 5.3 gives the values for the basic JV parameters, and Figure 5.8 displays how the JV curves change with these different widths. Though the n-strip width was decreased to 100 um, the slimmer p-strip cause the J_{sc} to drop to 29.2 mA/cm2, and the V_{oc} fell to 612 mV. Thus, for smaller widths, the p-strip dominates the resulting JV parameters. Likewise, for the larger strip widths, even with the wider p-strip width benefiting the device, the larger n-strip width causes the FF, and thus the efficiency, to drop.

Table 5.3 JV parameters from changing both p- and n-strip widths. Ratios of the widths are held constant.

p- and n-widths (um)	I_{sc} (mA/cm^2)	V_{oc} (mV)	FF (%)	Efficiency (%)
560-100	29.2	612	71.8	12.9
840-150	32.1	628	72.2	14.5
1120-200	33.0	634	71.8	15.0
1400-250	32.9	629	70.0	14.5
1680-300	32.4	627	69.8	14.2

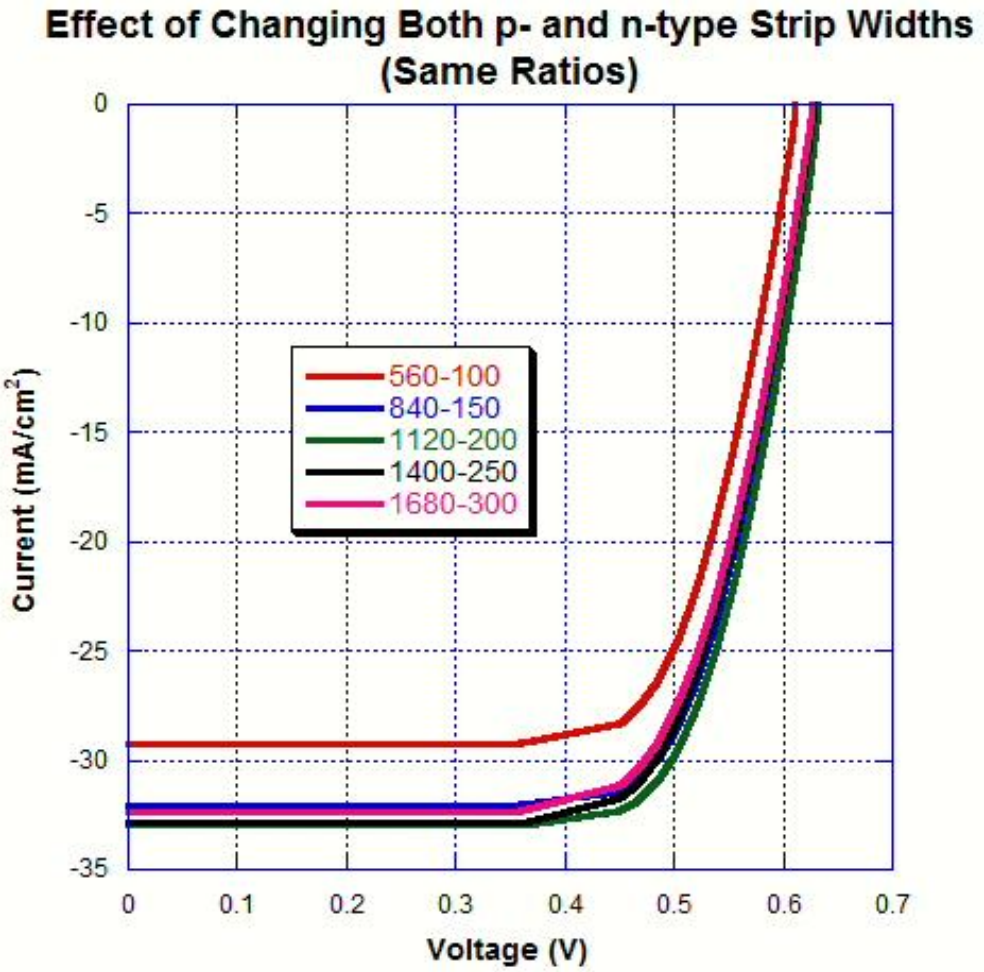

Figure 5.8 JV curves showing the effect of changing the doped layer finger widths, keeping the same p/n width ratio.

In simulating the effect of changing the gap-width between the p- and n-strips, little change was found in the results. Gaps having a width greater than 100 um started to show a decrease in device performance, but any width less than 100 um shows negligible difference in JV parameters. If the gaps are passivated well by the SiN_x, then the gap width does not seem to make a difference on IBC-SHJ solar cell results. Basic device physics suggests that the narrower the gaps, the better the results will be since they only represent potential recombination surfaces; current is

transported laterally near the Si/SiN_x heterojunction in the gap but does not cross the interface. There are physical limitations to this, however. Experimentally and from simulations, the best cell results come from narrower gaps and n-strips. A photomask alignment issue arises from decreasing these widths too much, though, and thus the geometry is limited by this factor.

5.5 Wafer Resistivity

Wafer resistivity plays a major role in device performance for IBC-SHJ solar cells. As was stated previously, the wafers currently used for device fabrication have a resistivity of about 2.5 Ωcm. Other SHJ and IBC groups have used wafers with resistivities ranging between 0.5-4 Ωcm [30]-[33]. Experiments were simulated to see how the JV parameters changed for different wafer resistivities. Physically, the wafer resistivity and electron/hole mobilities are related, and as such, both were changed together. Table 5.4 lists the values for the resistivities, the corresponding mobilities, and the values for the JV parameters. Though V_{oc} saw no change, J_{sc} and FF varied immensely. This would lead one to believe that the IBC portion of the device is the reason for the sensitivity to wafer resistivity. Higher fill factors were achieved with lower resistivity wafers, but the efficiency suffered because of the dramatically decreased current. Both the 2.50 Ωcm and 6.50 Ωcm wafers shared the same efficiency, and so the optimal wafer resistivity is believed to be within this range. Table 5.5 compares the maximum V_{oc} and efficiency achieved with wafers in SHJ solar cells having resistivities between the 0.5-4 Ωcm range for different companies. Since the model of IEC's SHJ cell matches with experimental results, and thus

compares with the devices in the table, we see that the 2.5 Ωcm resistivity currently used is sufficient for the IBC-SHJ device.

Table 5.4 JV results from changing wafer resistivies and carrier mobilities.

Wafer Resistivity (Ωcm)	Electron/Hole Mobility (cm^2/Vs)	J_{sc} (mA/cm^2)	V_{oc} (mV)	FF (%)	Efficiency (%)
0.11	806/342	18.9	673	78.7	10.0
0.29	1074/407	28.2	675	75.4	14.3
0.73	1228/438	32.2	674	73.8	16.0
2.50	1334/457	34.1	674	72.6	16.7
6.50	1373/464	34.7	673	71.5	16.7

Table 5.5 Comparison of different SHJ wafer resistivity results between companies. The simulation of IEC's SHJ cell matches with that of experiments, and thus compares to the devices in the table.

	Area (cm^2)	Best V_{oc} (V)	Best η (%)
Sanyo [2]	100	0.739	22.3
HZBME (HMI) [32]	1	0.660	19.8
NREL [33]	0.9	0.694	18.2
IEC [20]	0.56	0.694	18.4
Univ. of Neuchatel [12]		0.713	18.4
AIST [26]	0.21	0.610	15.8
CNR-IMM [11]	1	0.638	14

5.6 Wafer Lifetime and Thickness

Several simulations were created to analyze the effect of decreasing the lifetime of the c-Si wafer on device performance for varying thicknesses of the wafer. A range of lifetimes from 1 usec to 1000 usec and thicknesses from 25 um to 150 um was considered. The goal of this study was to verify a maximum peak in efficiency for some thickness within this range. The peak efficiency would of course be found for the wafer with the highest lifetime. These simulations were not meant to model IEC's device performance, but rather, to see the limit on efficiency that could be achieved with the wafers that were being used. A problem arose with this experiment, as the simulations were limited to wafers that were planar. At greater thicknesses, this was not too much of an issue. But for very thin planar wafers, there is no mechanism for light trapping, and the short-circuit current drops off dramatically. This issue was addressed by scaling the J_{sc} values to that of literature data incorporating textured wafers with superior light trapping abilities [34]. Due to the device being assumed as near-ideal, several parameters were altered to achieve a high level of performance. The defect levels in the doped amorphous silicon layers were reduced in the mid gap, and the characteristic energies of the band tail states were also reduced. The rear i-layer band gap was lowered to 1.66 eV, which is near the limit of where the growth of the layer does not yet become epitaxial. Surface recombination velocity was set to 1 cm/s for both the front and rear intrinsic a-Si/c-Si interfaces, and thus, D_{it} at these interfaces was decreased. These parameters can be considered slightly optimistic but not impossible to achieve.

Figure 5.9 shows the results of these simulations for the IBC-SHJ solar cell. They indicate that a wafer lifetime of around 300 μsec is required to exceed 20% at

any thickness. The data also shows that low quality wafers (<10 μsec) fail to yield acceptable performance even for very thin (<50 μm) devices no matter how ideal the processing is. Finally, this design is capable of exceeding 23% with optimistic parameters.

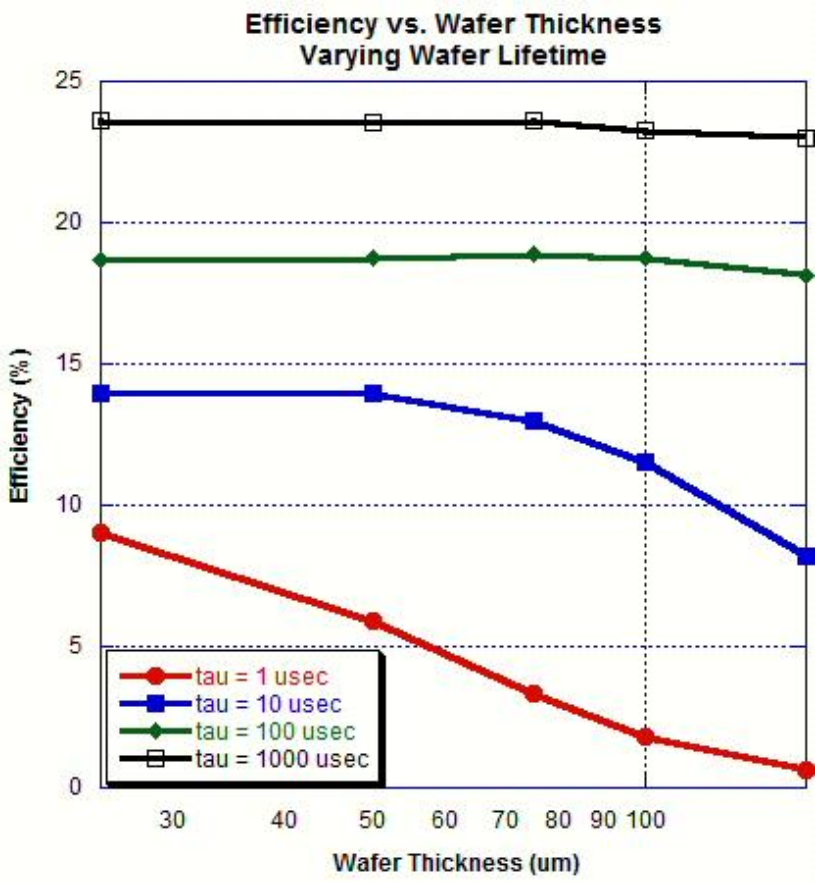

Figure 5.9 **Efficiency vs. wafer thickness for different lifetimes. The conversion from planar simulations to textured experimental devices was made using literature scaling factors. High-lifetime carriers see almost uniform collection regardless of wafer thickness, whereas short-lifetime carriers need thinner wafers for efficient collection.**

Chapter 6

CONCLUSION

This thesis has described the advantages that the novel IBC-SHJ solar cell has over standard diffused junctions on thick crystalline wafer and SHJ solar cells. After showing the processing steps in creating this device, characterization techniques used in the research have been discussed. An overview of Synopsys' TCAD software Sentaurus was presented with details about coding the simulations and the key parameters in the model which influence the device performance, especially the FF. Finally, the research results were shown in Chapter 5. The following sections summarize the findings, highlight some special aspects about this research, and discuss the application to future work.

6.1 Summary

The model has proven numerically and through literature to agree well with experimental results on IBC-SHJ solar cells. The main parameters used to model the devices were mid gap and band tail defect levels, interface defects in combination with surface recombination velocity, and rear i-layer band gaps. Research done on SHJ solar cells at IEC and other companies provided the physical parameters for the amorphous silicon layers.

Since the limiting factor on device performance is FF, methods of improving this were investigated. The mid gap defect levels in the emitter layer proved to only have some control over how high this parameter was. However, the band tail defect

levels governed the upper limit of the FF increase. The much more sensitive feature, the rear i-layer band gap, is more powerful in that low FF can occur easily within a few hundredths of an eV. Both the band gap and defect levels can be the cause of S-shaped JV curves, which is why these two features are being investigated currently in experimental devices.

Other simulations were used more to determine that some parameters in the device structure were already optimized. The number of interdigitated fingers on the rear surface were found to be sufficient, and adding more fingers does not increase efficiency further. Simulations of different ratios of the widths of the doped a-Si:H layers showed that the 1400-250 μm geometry was sufficient for good device performance. While V_{oc} was relatively unaffected, J_{sc} evenly decreased as the p-strip width decreased or the n-strip width increased. Simulations of variations in wafer resistivity showed the relationship between J_{sc} and FF. As wafer resistivity decreased, so did the J_{sc}, but FF increased, proving that 2.50 Ωcm wafers are suitable for device fabrication. Experiments on SHJ have shown that wafer resistivity is not a sensitive parameter, and so the IBC portion of the IBC-SHJ device is mainly affected by this feature. Lastly, wafer lifetime and thickness simulations, using ideal device parameters, showed where the future of silicon wafers is going to be. To achieve maximum efficiencies, wafers will have to be roughly 75 μm thick with lifetimes greater than 1 msec.

6.2 Improved IBC-SHJ Fabrication

Several characteristics of the two-cell IBC-SHJ devices made at IEC have hindered their results. The long diffusion length leads to collection of carriers outside

of the defined cell area so masks are used to block the incident light during JV testing. However, this presents a few problems. With the mask placed between the source of light and the solar cell, there is no way to see if the mask is aligned with the defined contact area on the rear side of the device. Also, because the silicon wafer is not always exactly 1" x 1", and the mask structure is, the quality of the alignment becomes even more difficult to discern, and J_{sc} is decreased. An even greater concern comes from the fact that the cell is not a perfect rectangle, and so different masks were made to allow illumination of different portions of the device. Where some masks had an area slightly larger than the entire cell, others had areas that allowed illumination of either more of the p-type or n-type fingers. This, of course, resulted in varying device performance. A strange phenomenon concerning V_{oc} when the mask is placed on the cell occurs. The V_{oc} decreases from what is assumed to be a dark-diode effect occurring when the entire cell is not illuminated. One solution that was investigated to solve this problem, along with the need for masking during JV testing, was to laser scribe around each cell for isolation from the rest of the wafer. This, however, caused roughly a 20 mV drop in V_{oc}.

A more advanced solution to this problem was to double the active area of the IBC-SHJ solar cell in hopes of minimizing these edge effects. Because the diffusion length is so long in these wafers (~2-3 mm), smaller cells will be more affected by the edge effects. The ratio of the cell perimeter to area decreases as the cell becomes larger, which explains why smaller cells are more affected. With excess carriers being generated outside of the cell area when no mask is used, the difference in the quasi-fermi potentials increases, and so does the V_{oc}. This is why the V_{oc} drops when the device is masked. In the new design, more interdigitated fingers are added, the shape

of the rear contacts becomes perfectly rectangular, and only one cell is fabricated on each substrate. The processing remains the same; a two-step photolithography procedure is used. Collection outside of the cell area still occurs, but is reduced due to the larger area. A new masking procedure has also been implemented. By using a self-aligning mask, the variability in testing has been drastically reduced. This mask is shown in Figure 6.1.

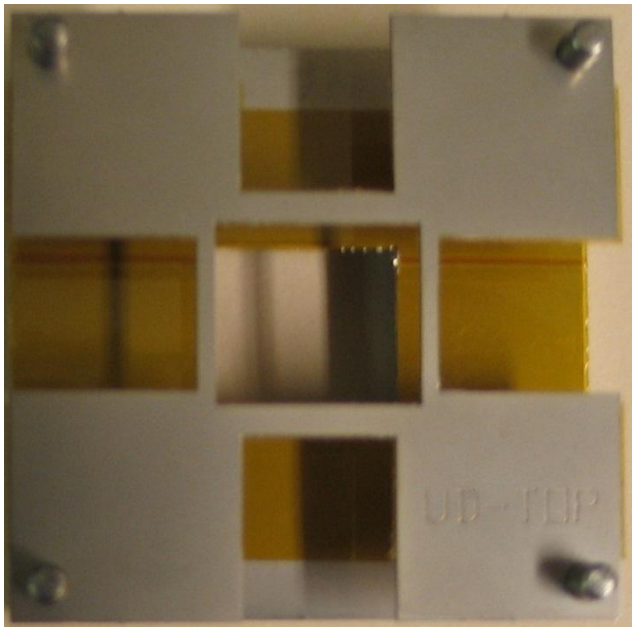

Figure 6.1 **Self-aligning IBC-SHJ mask used for JV testing. The solar cell, aluminum-side up, is placed on top of the base of the mask. The base has been covered with Kapton tape to insulate the mask from the cell. The "UD-TOP" patterned portion is then lowered over the cell. Using tweezers, the cell is positioned so that all of the Al contacts are visible. This aligns the incident light on the top surface of the cell with the defined area on the rear side. The four bolts in the corners keep the mask aligned with the base.**

Furthermore, a new one-step photolithography process is being studied in an attempt to increase device performance. The process involves depositing a p-type a-Si:H layer

on the entire rear side of the wafer immediately after the intrinsic a-Si:H layer deposition. Besides reducing the number of processing steps in different chambers of the silicon system, there is an added benefit in enabling this layer to be deposited at a higher temperature. As was stated in Chapter 5, increasing the temperature deposition from 200 °C to 250 °C will decrease the defect levels in the emitter layer, and thus improve FF. The standard photolithography, PECVD, and lift-off steps are then performed to deposit the n-strips. Also, the gap between the interdigitated fingers is reduced to roughly 5 nm wide, which is beneficial considering the presence and passivating quality of the SiN_x is questionable at this stage. For the two-cell IBC-SHJ cells, the gap was roughly 2% of the total area of the device, and for this new structure, the gap is only 1% of the total area.

Preliminary tests on both test structures have shown promising results. The two-step photolithography process has recently produced devices with increased V_{oc}, but they still suffer from a slight S-shaped JV curve. The one-step photolithography process is still under development, but early results show the removal of the S-shaped curve, which is believed to be from the p-type layer being deposited at 200 °C. However, all of the devices still suffered from low FF. After performing the dV/dJ analysis and correcting the JV curve for the resulting series resistance, the FF increased only from 55-58% to 63-66%. From this research, the prediction is that this FF will increase if the p-type layer is deposited at 250 °C.

6.3 Future Studies

The progress of simulating the IBC-SHJ device will continue with the development of this new solar cell structure. If the low FF problem is not completely solved by increasing the deposition temperature of the p-type layer, then other simulation studies will have to be investigated. An example of such a study would be to see if lowering the n-type contact 2 um into the wafer significantly changes device performance. This would correlate to the effect of the new etchant used in the deposition process of the n-type fingers in the one-step photolithography process, which removes roughly 2 um of the c-Si wafer.

The relation between advancements in IBC-SHJ solar cell technology and numerical simulation should be symbiotic. New device structures will require interpretation via modeling, and provide new data for model adjustments. Alternatively, new simulation studies will provide new directions and guidance for the design and fabrication of even better IBC-SHJ solar cells.

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